'97-'98

SEMICONDUCTOR DATABOOK

BIPOLAR IC

- AUDIO
- VIDEO
- COMMUNICATION
- OTHERS

JRC New Japan Radio Co., Ltd.

US SUBSIDIARY NJR CORPORATION, CALIFORNIA (U.S.A.)

SEMICONDUCTOR DATA BOOK

BIPOLAR IC

- AUDIO
- VIDEO
- COMMUNICATION
- OTHERS

New Japan Radio Co., Ltd.

[CAUTION]

1. NJRC strives to produce reliable and high quality semiconductors. NJRC's semiconductors are intended for specific applications and require proper maintenance and handling. To enhance the performance and service of NJRC's semiconductors, the devices, machinery or equipment into which they are integrated should undergo preventative maintenance and inspection at regularly scheduled intervals. Failure to properly maintain equipment and machinery incorporating these products can result in catastrophic system failures.

2. To ensure the highest levels of reliability, NJRC products must always be properly handled. The introduction of external contaminants (e.g. dust, oil or cosmetics) can result in failures of semiconductor products.

3. NJRC offers a variety of semiconductor products intended for particular applications. It is important that you select the proper component for your intended application. You may contact NJRC's Sale's Office if you are uncertain about the products listed in this catalog.

4. Special care is required in designing devices, machinery or equipment which demand high levels of reliability. This is particularly important when designing critical components or systems whose failure can foreseeably result in situations that could adversely affect health or safety. In designing such critical devices, equipment or machinery, careful consideration should be given to, amongst other things, their safety design, fail-safe design, back-up and redundancy systems, and diffusion design.

5. The products listed in the catalog may not be appropriate for use in certain equipment where reliability is critical or where the products may be subjected to extreme conditions. You should consult our sales office before using the products in any of the following types of equipment.

Aerospace Equipment
Equipment Used in the Deep sea
Power Generator Control Equipment (Nuclear, Steam, Hydraulic)
Life Maintenance Medical Equipment
Fire Alarm/Intruder Detector
Vehicle Control Equipment (automobile, airplane, railroad, ship, etc.)
Various Safety Equipment

6. NJRC's products have been designed and tested to function within controlled environmental conditions. Do not use products under conditions that deviate from methods or applications specified in this catalog. Failure to employ NJRC products in the proper applications can lead to deterioration, destruction or failure of the products. NJRC shall not be responsible for any bodily injury, fires or accidents, property damage or any consequential damages resulting from the misuse or misapplication of its products. PRODUCTS ARE SOLD WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

7. The product specifications and descriptions listed in this catalog are subject to change at any time, without notice.

JRC

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

INTRODUCTION

1

ORDERING INFORMATION

■ ORDERING INFORMATION

NJRC ICs are named by NJRC Naming Standard. Please order our ICs by their full names.

1. NJRC Naming Standard
   NJRC applies IC naming standard in the following.

(1) Integrated Circuit

① Bipolar Example : NJM 4558 D - A (T1)
1 2 3 4 5

Item 1 Classification of items
NJM -------Bipolar monolithic IC
NJW -------Bi-MOS IC

Item 2 Part Number
The name of product is shown by three-digit or four-digit number.
In case of substantial modification of circuit or masks, one capital alphabet is added to the name.
Example : NJM2233 → NJM2233B

Item 3 Classification of Package
The codes in [ ] are names defined in NJRC.

D	-------Dual-in-line plastic mold	[DIP]
E	-------Dual-in-line plastic mini-mold	[EMP]
F	--------Dual-in-line plastic mini-mold	[MTP-5]
	Quad flat plastic mold *QFP package is indicated by one capital alphabet (mold size) and one-digit number (lead length and forming) after F.	[QFP]
G	--------Dual-in-line plastic mini-mold	[SOP]
L	-------Shrunk dual-in-line plastic mold	[SDIP]
M	-------Dual-in-line plastic mini-mold	[DMP]
N	-------Dual-in-line plastic mold	[DIP]
V	-----Dual-in-line plastic shrunk mini-mold	[SSOP]
C	-------Chip	

Item 4 Characteristics Selection and Screening Option
Specially selected product or specially screened product are shown by within two capital alphabets after a hyphen.

Item 5 Taping Form
The taping form is shown by alphanumeric in parentheses.

② C-MOS Example : NJU 6408B FG1 - 00 , NJU 6391A E (T1)
1 2 3 4 1 2 3 5

Item 1 Classification of items
NJU--------MOS IC
NJW -------Bi-MOS IC

Item 2 Part Number
The name of product is shown by three-digit or four-digit number and one capital alphabet (series product only).
Example : NJU6391A/91B/91C

In case of substantial modification of circuit or masks, one capital alphabet is added to the name.
Example : NJU6408 → NJU6408B

Item 3 Classification of Package
The codes in [ ] are names defined in NJRC.

D -------Dual-in-line plastic mold	[DIP]
E -------Dual-in-line plastic mini-mold	[EMP]
F --------Quad flat plastic mold	[QFP]
Quad flat plastic mold *QFP package is indicated by one capital alphabet (mold size) and one-digit number (lead length and forming) after F.	
G--------Dual-in-line plastic mini-mold	[SOP]
L ------Shrunk dual-in-line plastic mold	[SDIP]
M -------Dual-in-line plastic mini-mold	[DMP]
N--------Dual-in-line plastic mold	[DIP]
V -------Dual-in-line plastic shrunk mini-mold	[SSOP]
C -------Chip	
H -------TCP (Tape Carrier Package)	

Item 4 ROM Code, Title and Screening Option

LCD Controller Driver	: Indicating ROM code by a alphanumeric after a hyphen.
Melody IC	: Indicating Title of the melody by capital alphabets after a hyphen.
Screening Product	: Indicating Screening level by one capital alphabet after a hyphen.

Item 5 Taping Form
The taping form is shown by alphanumeric in parentheses.

(2) Terminal Voltage Regulator

① 78/79 series

Example : NJM 78M 00 FA - B (T1)
1 2 3 4 5 6

Item 1 Classification of items
NJM -------Bipolar monolithic IC

Item 2 Part Number
The name of product is shown by two-digit number and one capital alphabet.

Item 3 Output Voltage
The output voltage is shown by two-digit number.

Item 4 · Classification of Package
The codes in [ ] are names defined in NJRC.

F	--------3 terminal plastic mold(Fully Covered)	[TO-220F]
U	--------3 terminal plastic mini-mold	[SOP]
No mark	---- 3 terminal plastic mold	[TO-92] (Note)

(Note) : NJM78L/79L only

·Output Voltage Accuracy
The output voltage accuracy is shown by one capital alphabet after package type mark.

Item 5 Characteristics Selection Option
Specially selected product is shown by within two capital alphabets after a hyphen.

Item 6 Taping form
The taping form is shown by alphanumeric in parentheses.

② C-MOS

Example: NJU 7201 L 00 (T1)
1 2 3 4 5

Item 1 Classification of items
NJU--------MOS IC

Item 2 Part Number
The name of product is shown by four-digit number and one capital alphabet.

Item 3 Classification of Package
The codes in [ ] are names defined in NJRC.

L	--------3 terminal plastic mold	[TO-92]
U	--------3 terminal plastic mini-mold	[SOT-89]

Item 4 Output Voltage
The Output voltage is shown by two-digit number.

Item 5 Taping form
The taping form is shown by alphanumeric in parentheses.

■ QUALITY ASSURANCE SYSTEM

1. Preface

In the present circumstance, it is not too much to say all electronic equipment is produced from the IC. The electronic equipment has been upgraded with its performance and plays important role in any industry. And the default of the equipment might cause a serious problem on the system. Thus the industry has required higher quality and reliability of IC year after year.

In compliance with this requirement, we New Japan Radio Co., Ltd. (hereinafter called we or NJRC) maintain the quality and reliability of the product by the following quality assurance system. To our customers we proffer the product which meet the customers requirement.

2. Policy on the Quality

Our fundamental policy on the quality is described below. With this policy, we are making the utmost effort to have the highest quality of the product. Not that quality is secured by a department but that quality is secured by the whole company.

Therefore we lead all worker to understand what quality is the most important.

3. Quality Assurance System

Fig. 1 shows NJRC's quality assurance system from the planning to the shipping.

(1) Quality Assurance during Development

① Design

We design the product to meet the customer's requirement by close communications.

For the quality of the design we check production technology, development data and quality information by Design Review (DR).

② Test Production

The test products are assessed the characteristic and the reliability.

The reliability evaluation method and condition shall be performed by ED-4741(EIAJ) specification.

③ Mass Production

The mass production is able to be started after consideration of process capability, yield result, reliability test result and customer's evaluation of ES (Engineering Sample).

(2) Quality Assurance during Mass Production

① Environment Control

The environment during IC production effect importantly the quality and the reliability.

We control properly the temperature, the humidity and the dust in fabrication. Especially we make the utmost effort to improve the cleanliness for the dust control is the most important factor.

② Quality Control of Raw Material

We make effort to improve the quality of the raw material by quality approval of the materials, the purchasing specification, incoming inspection and close communication with the vendors.

③ Process Control

We make effort to avoid scattering products by the standardization and automatic system.

We check the performance and the quality by the QC inspection. We feed back these results to the production department to maintain the stable process. Fig. 2 shows an example of process control.

④ Changing Control

We have the changing control system to avoid troubles by changing of the design, the process, the materials or the equipment. On this system, the changing of specification or characteristic is performed after customer's approval.

⑤ Supervision of Entrustment Productions

In case of entrusting production, we recognize the companies after evaluating their management attitude, technical ability , production record and quality information including the audit.

Process	Control Items
Wafer	
Wafer Process	
Wafer Test(100%)	Electrical characteristics
Visual inspection	Wafer visual
Silver Paste	
Dicing	Scribing Depth
Lead frame	
Qc inspection	Chip visual
Gold wire	
Die bonding	Temperature
Qc inspection	Visual, Die bonding strength
Wire bonding	Temperature, Ultra sonic power
Resin	
Qc inspection	Visual, Die bonding strength
Molding	Temperature, Pressure & Time
Qc inspection	Visual
Marking	
Electrical test	Electrical characteristics
Sampling inspection	Electrical characteristics, Visual
Stock	
Packing inspection	Product type, Quantity
Shipping	

Fig.2 QC Flow Chart

QUALITY ASSURANCE SYSTEM

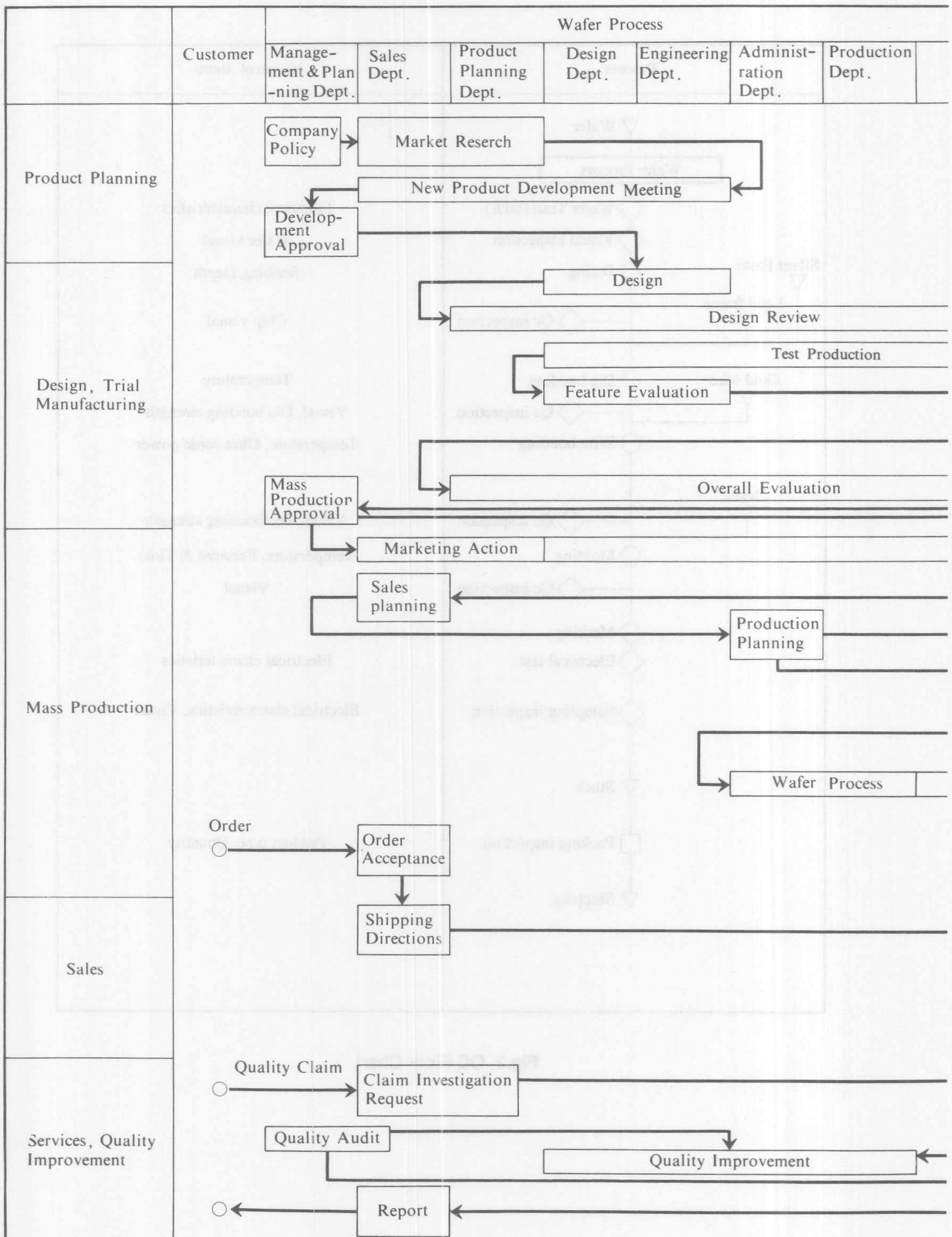
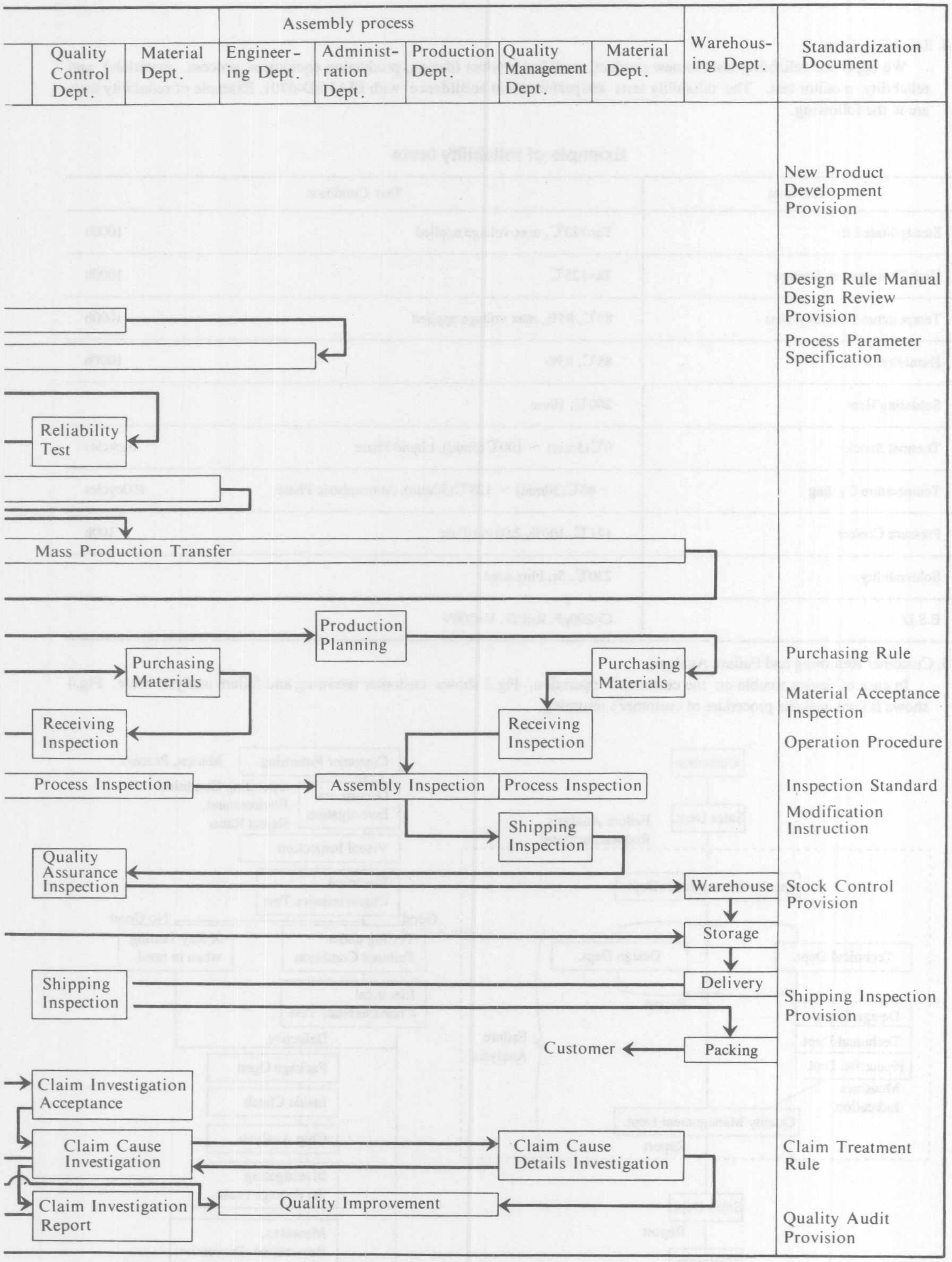


Fig. 1

QUALITY ASSURANCE SYSTEM



Qualithy Assurance System

4. Reliability Tests

We apply the reliability tests to new product, modified product (design, production equipment, process, materials) and reliability monitor test. The reliability tests are performed in accordance with EIAJ ED-4701. Example of reliability tests are in the following.

Example of reliability tests

Test Item	Test Condition	
Steady State Life	Ta=125℃, max voltage applied	1000h
High Temperature Storage	Ta=125℃	1000h
Temperature Humidity-Bias	85℃, 85%, max voltage applied	1000h
Humidity	85℃, 85%	1000h
Soldering Heat	260℃, 10sec	
Thermal Shock	0℃(5min) ~ 100℃(5min), Liquid Phase	10cycles
Temperature Cycling	−40℃(30min) ~ 125℃(30min), Atmospheric Phase	100cycles
Pressure Cooker	121℃, 100%, 2.03×10^5Pa	100h
Solderability	230℃, 5s, Flux used	
E.S.D	C=200pF, R=0Ω, V=200V	

5. Customer Returning and Failure Analysis

In case of device trouble on the customer's operation, Fig.3 shows customer returning and failure analysis route. Fig.4 shows failure analysis procedure of customer's returning.

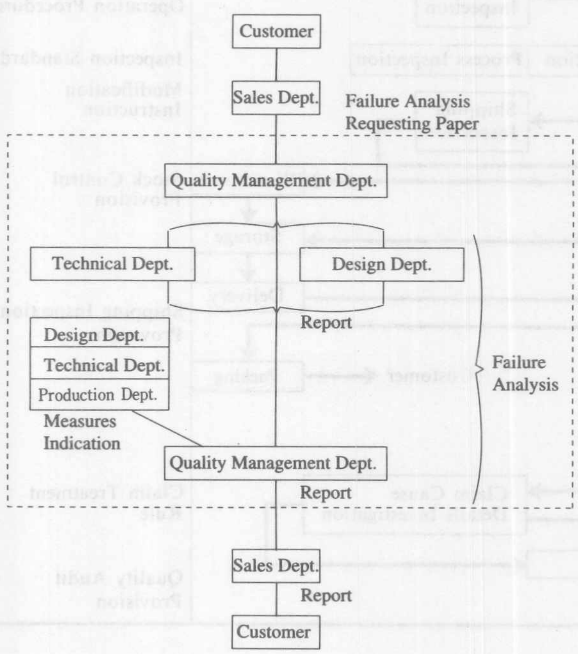


Fig.3 Customer Returning and Failure Analysis Route

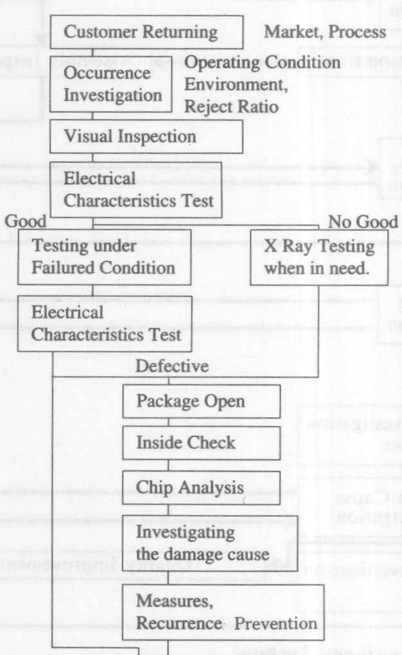


Fig.4 Failure Analysis Procedure

■ RECOMMENDED MOUNTING METHOD

1.Soldering Methods

The recommended soldering methods for each package are shown in the following table.

(1) Recommended Soldering Methods Table

Through-Hole mounted device type package

PKG	REFLOW	FLOW	IRON	PKG	REFLOW	FLOW	IRON
TO-92	○	○	○	SDIP22	○	○	○
TO-220F	○	○	○	SDIP24	○	○	○
DIP8	○	○	○	SDIP28	○	○	○
DIP14	○	○	○	SDIP30	○	○	○
DIP16	○	○	○	SDIP42	○	○	○
DIP18	○	○	○	SDIP56	○	○	○
DIP20	○	○	○	SIP8	○	○	○
DIP22	○	○	○	ZIP16	○	○	○
DIP28	○	○	○				
DIP40	○	○	○				

Surface mount device type package

PKG	REFLOW	FLOW	IRON	PKG	REFLOW	FLOW	IRON
SOT-89	○ *1	×	○	SSOP8	○	×	○
MTP-5	○ *1	×	○	SSOP14	○	×	○
DMP8	○ *2	○ *3	○	SSOP16	○	×	○
DMP14	○	○	○	SSOP20	○	×	○
DMP16	○	○	○	SSOP24	○	○	○
DMP20	○	×	○	QFP44-A1	○	×	○
DMP24	○	○	○	QFP44-B1	○	×	○
SDMP30	○	○	○	QFP56-A1	○	×	○
EMP8	○	○	○	QFP64-B2	○	×	○
EMP14	○	○	○	QFP64-B3	○	×	○
SOP8	○	○	○	QFP64-C1	○	×	○
SOP18	○	○	○	QFP64-C2	○	×	○
SOP20	○	○	○	QFP64-D1	○	×	○
SOP22	○	○	○	QFP64-E1	○	×	○
SOP28	○	○	○	QFP80-C1	○	×	○
SOP40	○	○	○	QFP80-C2	○	×	○
				QFP100-C1	○	×	○
				QFP100-C2	○	×	○
				QFP64-G1	○	○ *4	○
				QFP80-G1	○	○ *4	○
				QFP100-G1	○	○ *4	○

○ : Twice soldering is allowed.

*1:Once soldering only.

*2:NJM2073M,NJMOP-07M and NJM5532M once soldering only.

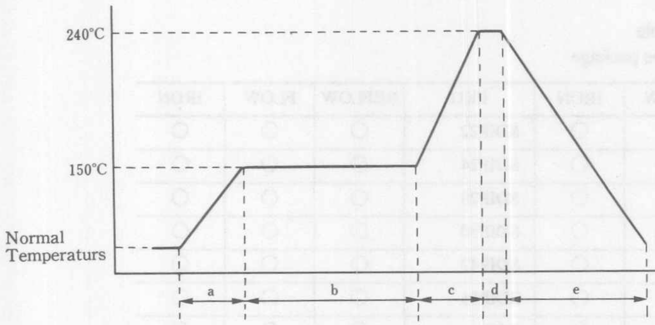
*3:Expect NJM2073M,NJMOP-07M,NJM5532M.

*4:Some of devices are allowed only once.

× : Don't apply.

(2) Soldering Temperature Profile of Reflow

Recommended reflow soldering temperature profile is in the following.

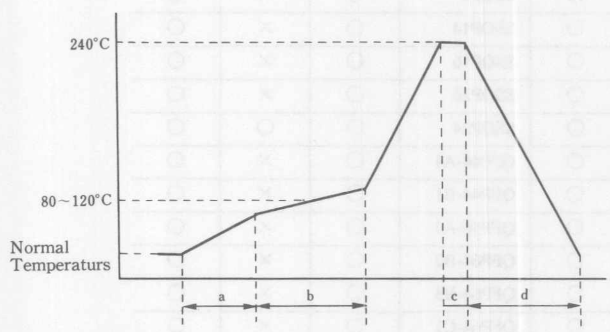


a : Temperature ramping rate		1℃～7℃/sec
b : Pre-heating	Temperature	150℃
	Time	60～120sec
c : Temperature ramping rate		1℃～7℃/sec
d : Main heating	Temperature	240℃ max
	Time	within 10sec
e : Ramping rate		7℃/sec max

Note : The temperature mentioned are measured on the surface of mold resin.

(3) Soldering Temperature Profile of Flow

Recommended flow soldering temperature profile is in the following.



a : Temperature ramping rate		1℃～7℃/sec
b : Pre-heating	Temperature	150℃
	Time	60～120sec
c : Main heating	Temperature	240℃ max
	Time	within 10sec
d : Ramping rate		7℃/sec max

Note : The temperature mentioned are measured on the surface of mold resin.

(4) Soldering Temperature Profile of Iron

Recommended iron soldering temperature profile is in the following.

At 1 lead Temperature : within 300～340℃
Time : within 3sec

(5) Note

It is not good for IC's reliability to keep IC High temperature for long time within limit of recommended ranges.
Please finish soldering as soon as possible within limit of recommended ranges.

RECOMMENDED MOUNTING METHOD

2. Recommended Soldering Method for Moisture-Proof Packing

(1) Mounting

Be sure to use within 7days after opening and to apply 2nd soldering within 3days.

Be sure to apply soldering within twice.

(2) Storage

It is better to keep ICs at following condition.

Temperature : 5～40℃, Humidity : 40～60%

(3) Baking

In case of keeping except above condition, be sure to apply baking.

Baking Method : Ta=125℃, over 16h

3. Flux Cleaning

Please clean flux,because halogen compound in flux is badly affected to products. The example of flux cleaning is in the following.

Frequency	: 28kHz
Power	: 20W/l
Temperature	: 40℃
Time	: between 30～40sec

CAUTION : Don't brush ink marking face while cleaning.

To take care the products resonation and touch directly to the vibrator.

4.Recommended Solder Pads for Surface Mount Package

Recommended solder pads for each package are shown as follows.

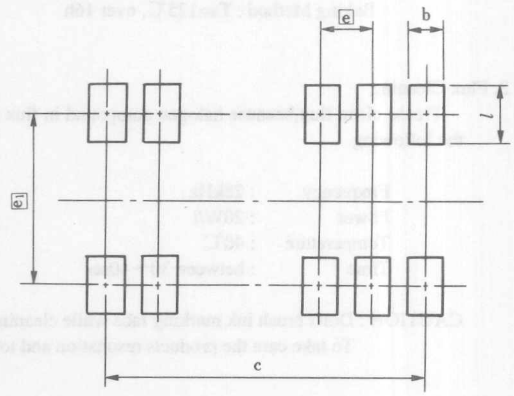
Please take easiness of mounting, reliability of bonding, prevention of solder bridge, margin of pattern area into consideration when designing the solder pads.

(1) Example of Solder Pads Dimensions

DMP/SOP/EMP/SSOP

PKG	b	l	e	e1	e
DMP8	0.72	1.27	3.81	6.10	1.27
DMP14	0.72	1.27	7.62	6.10	1.27
DMP16	0.72	1.27	8.89	6.10	1.27
DMP20	0.72	1.27	8.55	6.10	0.95
DMP24	0.72	1.27	13.97	9.53	1.27
SDMP30	0.60	1.27	14.00	9.53	1.00
SOP8	0.76	1.27	3.81	4.00	1.27
SOP18	0.76	1.27	10.16	4.90	1.27
SOP20	0.76	1.27	11.43	4.90	1.27
SOP22	0.76	1.27	12.70	4.90	1.27
SOP28	0.76	1.27	16.51	7.00	1.27
SOP40	0.76	1.27	24.13	8.90	1.27
EMP8	0.72	1.27	3.81	5.72	1.27
EMP14	0.72	1.27	7.62	5.72	1.27
SSOP8	0.35	1.00	1.95	5.90	0.65
SSOP14	0.35	1.00	3.90	5.90	0.65
SSOP16	0.35	1.00	4.55	5.90	0.65
SSOP20	0.35	1.00	5.85	5.90	0.65
SSOP24	0.45	1.00	8.80	7.30	0.80

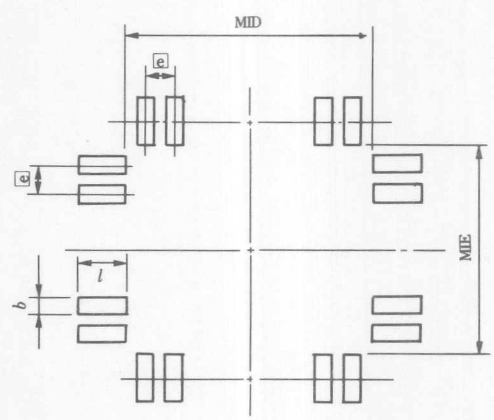
Unit:mm



QFP

PKG	MOLD SIZE	b	l	e	MID	MIE
QFP44-A1	10 X 10	0.50	1.20	0.80	10.4	10.4
QFP44-B1	14 X 14	0.70	1.80	1.00	14.4	14.4
QFP56-A1	10 X 10	0.35	1.20	0.65	10.4	10.4
QFP64-B2	14 X 14	0.50	1.60	0.80	14.4	14.4
QFP64-B3	14 X 14	0.50	1.40	0.80	14.4	14.4
QFP64-C1	20 X 14	0.70	2.80	1.00	20.4	14.4
QFP64-C2	20 X 14	0.70	2.00	1.00	20.4	14.4
QFP64-D1	10 X 10	0.20	1.00	0.50	10.4	10.4
QFP64-E1	14 X 14	0.50	1.30	0.80	14.4	14.4
QFP80-C1	20 X 14	0.50	2.80	0.80	20.4	14.4
QFP80-C1	20 X 14	0.50	2.80	0.80	20.4	14.4
QFP80-C2	20 X 14	0.50	2.00	0.80	20.4	14.4
QFP100-C1	20 X 14	0.35	2.80	0.65	20.4	14.4
QFP100-C1	20 X 14	0.35	2.80	0.65	20.4	14.4
QFP100-C2	20 X 14	0.35	2.00	0.65	20.4	14.4
QFP64-G1	14 X 14	0.50	1.00	0.80	14.4	14.4
QFP80-G1	14 X 14	0.35	1.00	0.65	14.4	14.4
QFP100-G1	14 X 14	0.20	1.00	0.50	14.4	14.4

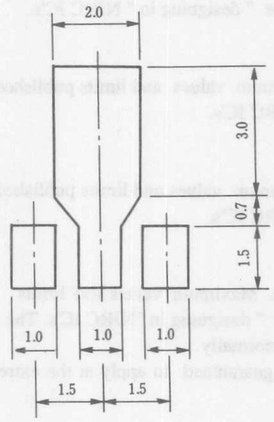
Unit:mm



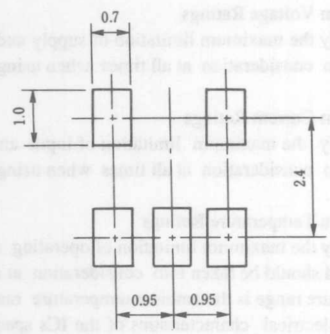
Note : These solder pads dimensions are just examples.

When designing PCB, please estimate the pattern carefully.

SOT-89



MTP5



Unit:mm

■ ABSOLUTE MAXIMUM RATINGS

1. Definition of Absolute Maximum Rating (Ta = 25℃)

NJRC defines maximum ratings as the values of voltage, current, temperature,power dissipation etc, which should not be exceeded at any time, otherwise deterioration or destruction of the IC may take place. Maximum values and limits published should be taken into consideration at all times when using or " designing in " NJRC IC's.

(1) Maximum Voltage Ratings

Specify the maximum limitation of supply and input voltages. Maximum values and limits published should be taken into consideration at all times when using or " designing in " NJRC IC's.

(2) Maximum Current Ratings

Specify the maximum limitation of input and output current. Maximum values and limits published should be taken into consideration at all times when using or " designing in " NJRC IC's.

(3) Maximum Temperature Ratings

Specify the maximum limitation of operating and storage temperature. Maximum values and limits published should be taken into consideration at all times when using or " designing in "NJRC IC's. The operating temperature range is the ambient temperature range that IC operates just normally.

The electrical characteristics of the ICs specified at 25°C are not guaranteed to apply at the extremes of the operating temperature range.

(4) Maximum Power Dissipation Rating

Specify the maximum limitation of power dissipation. Maximum values and limits published should be taken into consideration at all times when using or " designing in " NJRC IC's.

The power dissipation is mentioned following formula.

$P_D = (Tj - Ta) / \theta ja$ Where

P_D	: Power Dissipation	(w)
Tj	: Junction Temperature	(℃)
Ta	: Ambient Temperature	(℃)
θ ja	: Thermal Resistance	(w/℃)

As Tj is normally constant, the maximum power dissipation at a particular ambient temperature is determined by the thermal resistance of the package, which is in turn determined by it's dimensions and materials used in it's manufacture.

As a rule the smaller the package, the lower it's maximum power dissipation.

Note : Exceeding any of the maximum ratings, even briefly lead to deterioration in IC performance or even destruction.

PACKAGE 2

■ PACKAGE OUTLINE TABLE

	Suffix	3Pin	5Pin	8Pin	9Pin	14Pin	16Pin	18Pin	20Pin	22Pin
TO-92	L*1	○	—	—	—	—	—	—	—	—
TO-220F	F	○	—	—	—	—	—	—	—	—
SOT-89	U	○	—	—	—	—	—	—	—	—
MTP-5	F	—	○	—	—	—	—	—	—	—
DIP	D／N	—	—	○	—	○	○	○	○	○
SDIP	L	—	—	—	—	—	—	—	—	○
DMP	M	—	—	○	—	○	○	—	○*2	—
SOP	G	—	—	○	—	—	—	○	○	○
EMP	E	—	—	○	—	○	—	—	—	—
SSOP	V	—	—	○	—	○	○	—	○	—
SIP	S／L	—	—	○	○	—	—	—	—	—
ZIP	S	—	—	—	—	—	○	—	—	—
QFP	F	—	—	—	—	—	—	—	—	—

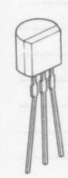
	Suffix	24Pin	28Pin	30Pin	40Pin	42Pin	44Pin	56Pin	64Pin	80Pin	100Pin
DIP	D／N	○*3	—	—	○	—	—	—	—	—	—
SDIP	L	○	○	○	—	○	—	○	—	—	—
DMP	M	○	—	○*4	—	○	—	—	—	—	—
SOP	G	○*3	○	—	○	—	—	—	—	—	—
EMP	E	—	—	—	—	—	—	—	—	—	—
SSOP	V	○	—	—	—	—	—	—	—	—	—
SIP	S／L	—	—	—	—	—	—	—	—	—	—
ZIP	S	—	—	—	—	—	—	—	—	—	—
QFP	F	—	—	—	—	—	○	○	○	○	○

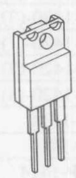
*1) Except NJM78L,NJM79LSeries

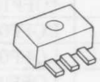
*2) Lead pitch: 0.95mm

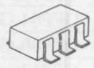
*3) These two packages are applied to only NJU9702.

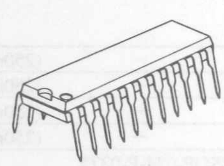
*4) Lead pitch: 1.0mm(SDMP-30)

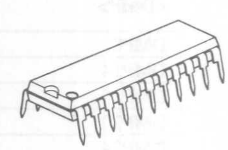

TO-92

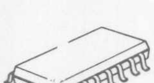

TO-220F

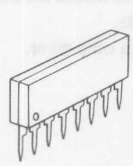

SOT-89

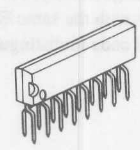

MTP-5

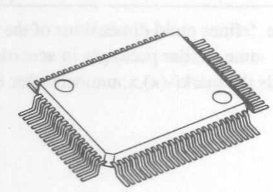

DIP


SDIP


DMP


SIP


ZIP


QFP

■ PACKAGE CODE TABLE(NJRC vs. EIAJ CODE)

The package codes using in this Data Book are NJRC codes defined by NJRC.
EIAJ codes which correspond to NJRC codes are shown as follows.

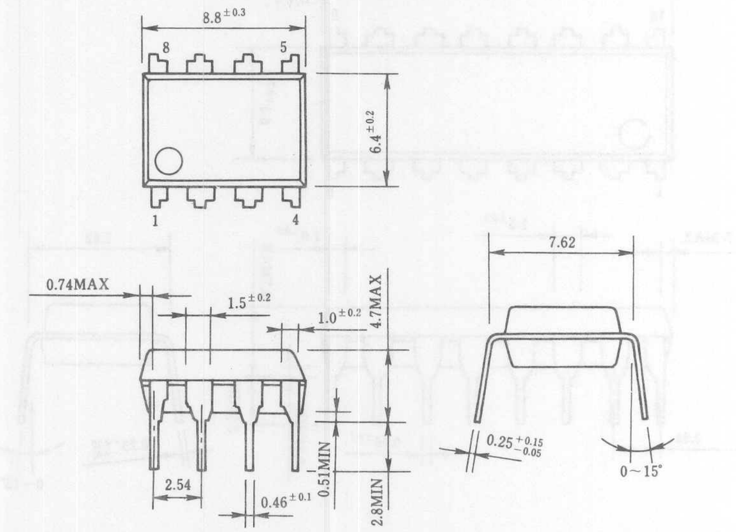
NJRC CODE	EIAJ CODE
<DIP>	
DIP8	*DIP008-P-0300
DIP14	*DIP014-P-0300
DIP16	*DIP016-P-0300
DIP18	*DIP018-P-0300
DIP20	*DIP020-P-0300
DIP22	*DIP022-P-0400
DIP24	*DIP024-P-0600
DIP40	*DIP040-P-0600
<SDIP>	
SDIP22	SDIP022-P-0300
SDIP24	SDIP024-P-0300
SDIP28	SDIP028-P-0400(Similar)
SDIP30	SDIP030-P-0400
SDIP42	SDIP042-P-0600
SDIP56	SDIP056-P-0600
<SIP/ZIP>	
SIP8	*SIP008-P-0000
SIP9	*SIP009-P-0000(Similar)
SIP9※	*SIP009-P-0000
ZIP16	*ZIP016-P-0325
<TO>	
TO-92(Viny Bag)	SC-43A
TO-92(Taping)	SC-43A
TO-220F	SC-67
<MTP/SOT>	
SOT-89	SC-62
MTP-5	SC-74A
<DMP>	
DMP8	– (250mil)
DMP14	– (250mil)
DMP16	– (250mil)
DMP20	– (250mil)
DMP24	*SOP-024-P-0375
SDMP30	SSOP030-P-0375
DMP42	– (450mil)

NJRC CODE	EIAJ CODE
<SOP>	
SOP8	*SOP008-P-0225
SOP18	*SOP018-P-0300
SOP20	*SOP020-P-0300
SOP22	*SOP022-P-0300
SOP24	*SOP024-P-0450
SOP28	*SOP028-P-0375
SOP40	*SOP040-P-0450
<EMP>	
EMP8	*SOL008-P-0150
EMP14	*SOL014-P-0150
<SSOP>	
SSOP8	SSOP008-P-0225
SSOP14	SSOP014-P-0225
SSOP16	SSOP016-P-0225
SSOP20	SSOP020-P-0225
SSOP24	SSOP024-P-0300
<QFP>	
QFP44-A1	*QFP044-P-1010
QFP44-B1	*QFP044-P-1414
QFP56-A1	*QFP056-P-1010
QFP64-B2	*QFP064-P-1414-(1) Note
QFP64-B3	*QFP064-P-1414-(2) Note
QFP64-E1	*QFP064-P-1414-(3) Note
QFP64-C1	*QFP064-P-1420-(1) Note
QFP64-C2	*QFP064-P-1420-(2) Note
QFP64-D1	*QFP064-P-1010
QFP80-C1	*QFP080-P-1420-(1) Note
QFP80-C1	*QFP080-P-1420-(2) Note
QFP80-C2	*QFP080-P-1420-(3) Note
QFP100-C1	*QFP100-P-1420-(1) Note
QFP100-C1	*QFP100-P-1420-(2) Note
QFP100-C2	*QFP100-P-1420-(3) Note
QFP64-G1	LQFP064-P-1414
QFP80-G1	LQFP080-P-1414
QFP100-G1	LQFP0100-P-1414

Note : EIAJ code defines mold dimensions of the package exactly, but lead dimensions are defined loosely.
There are some similar packages in accordance with the same EIAJ code.
NJRC adds the mark(-(x),x:number) after EIAJ code to distinguish them each other.

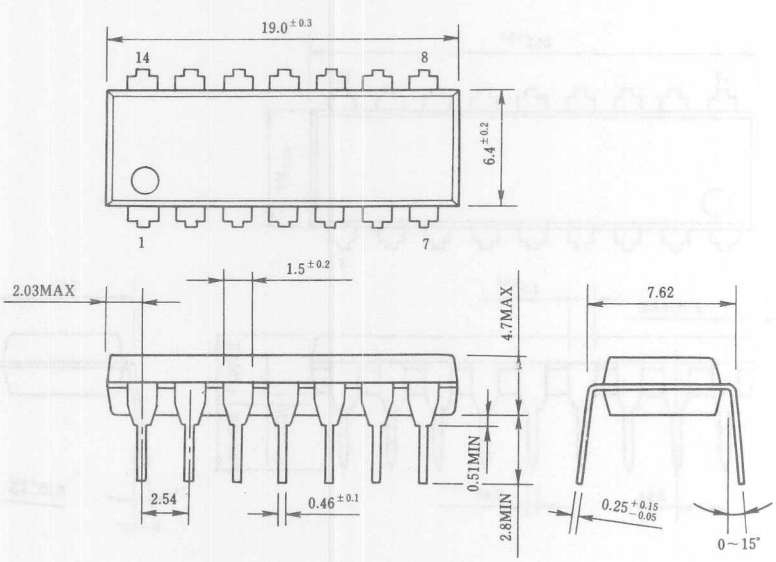
■ PACKAGE DIMENSIONS

DIP8



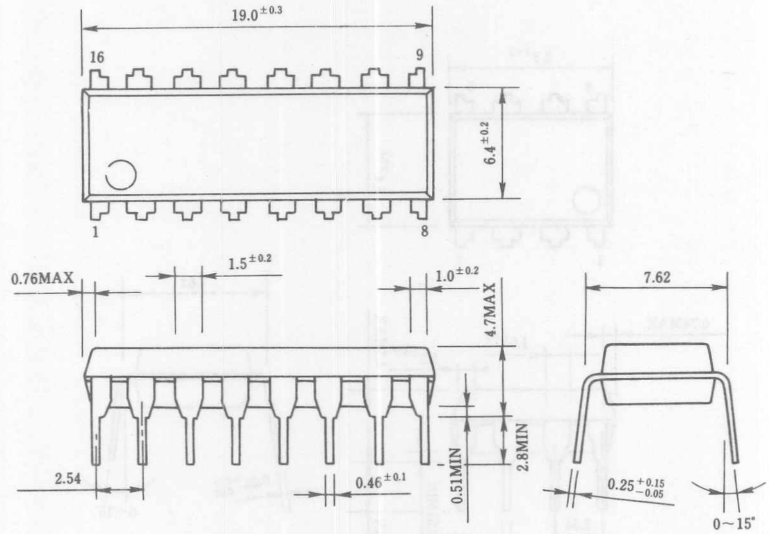
Unit:mm

DIP14



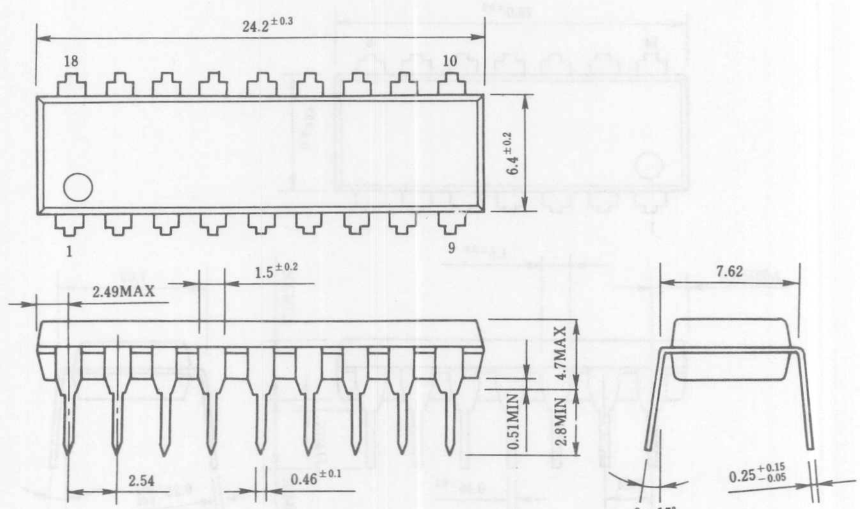
Unit:mm

DIP16



Unit:mm

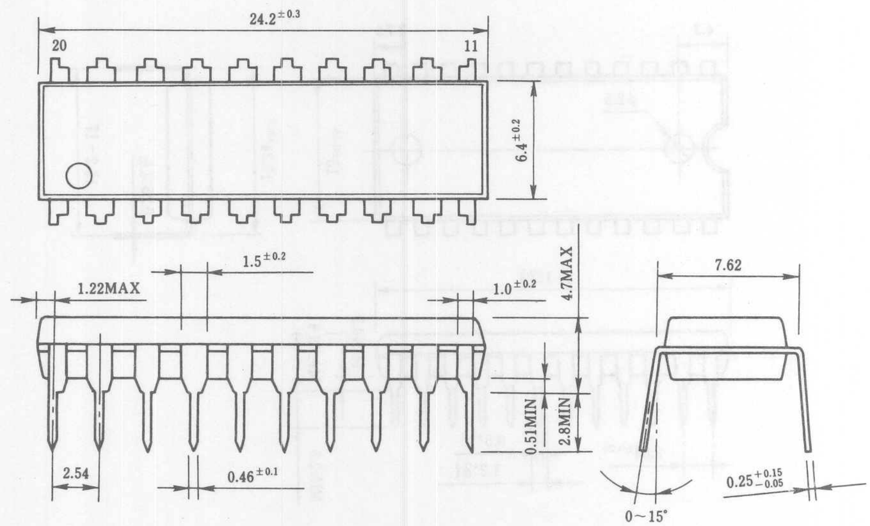
DIP18



Unit:mm

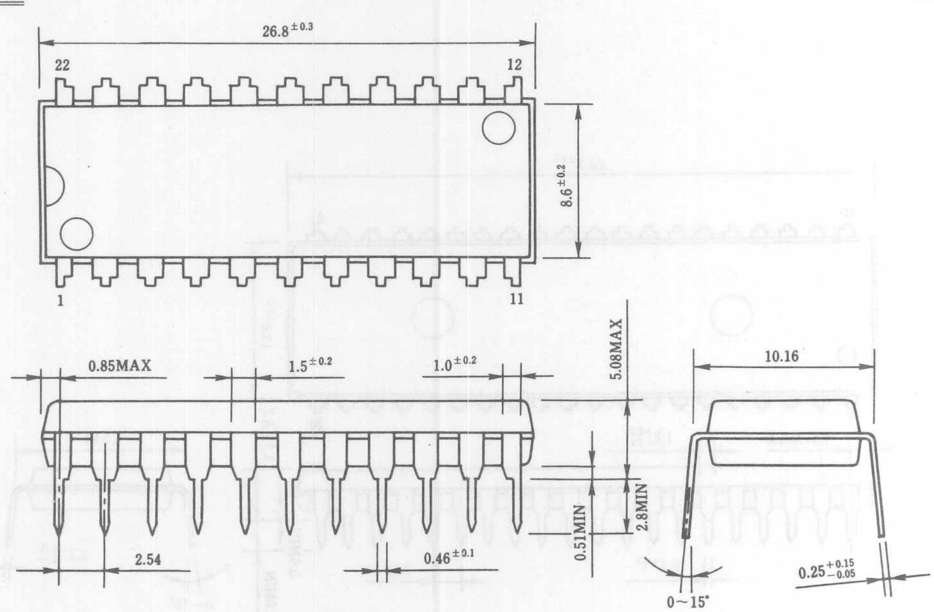
PACKAGE DIMENSIONS

DIP20



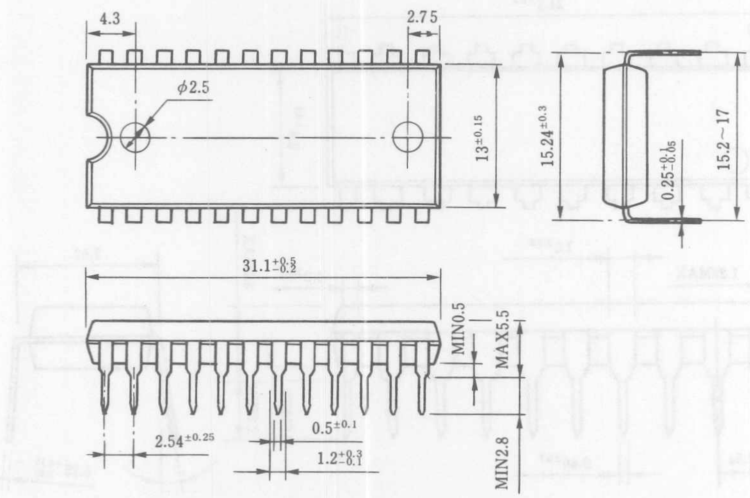
Unit:mm

DIP22



Unit:mm

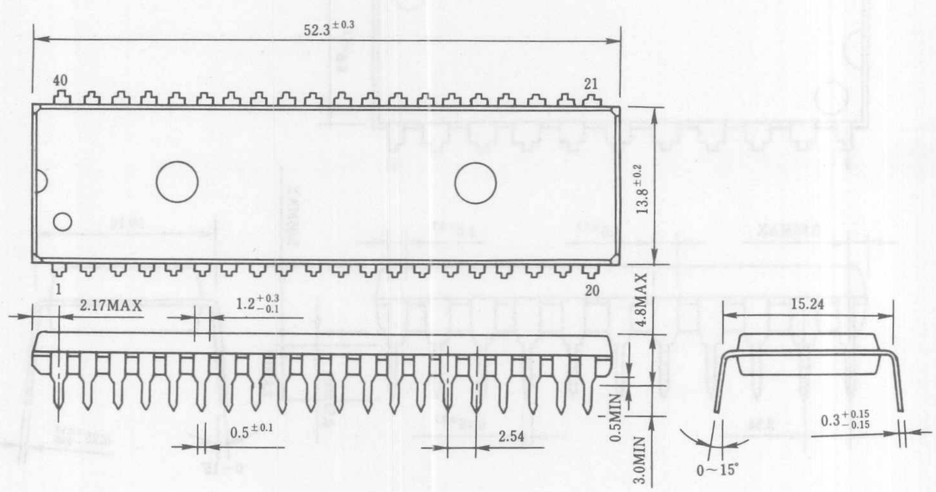
DIP24



* This package is applied to only NJU9702.

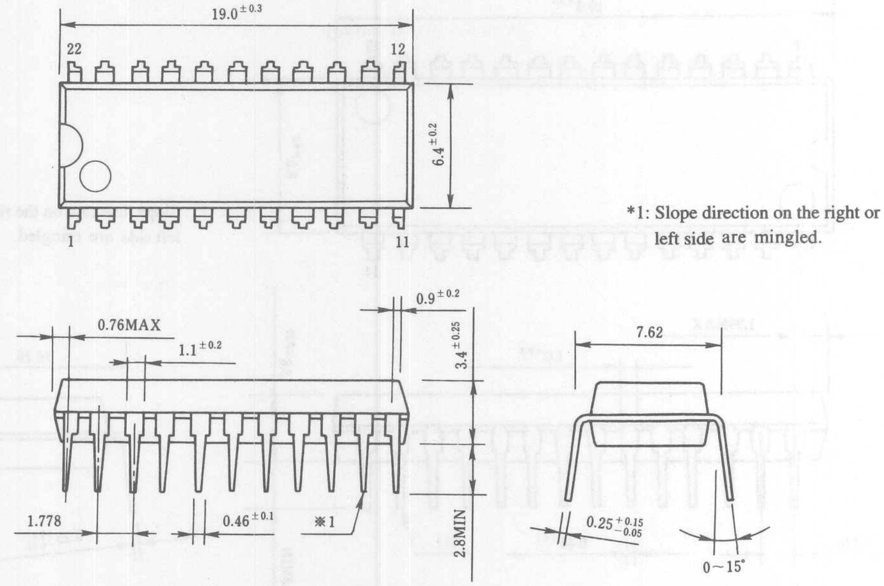
Unit:mm

DIP40



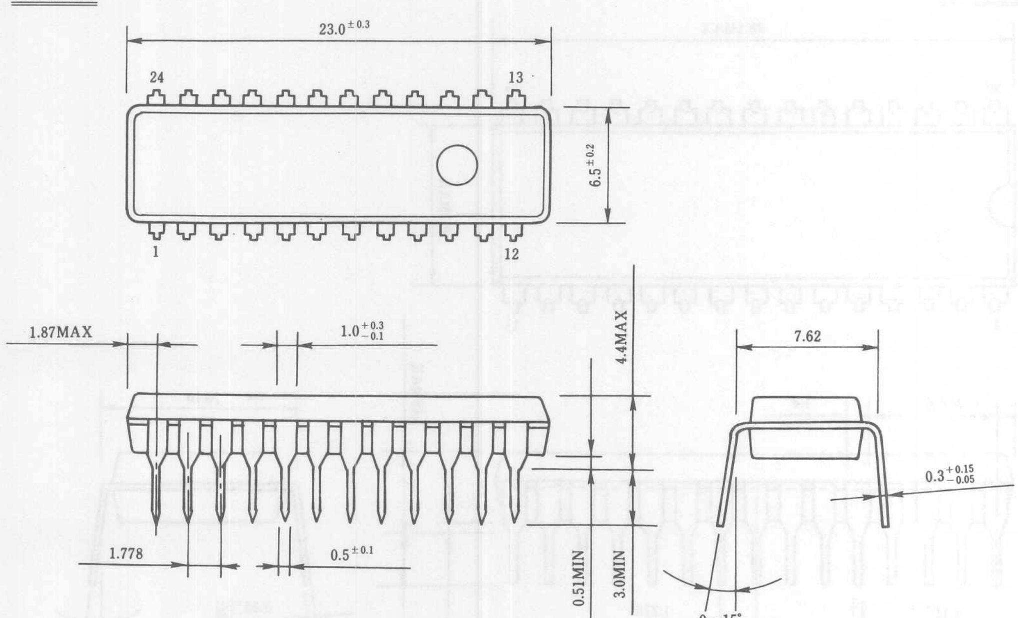
Unit:mm

SDIP22



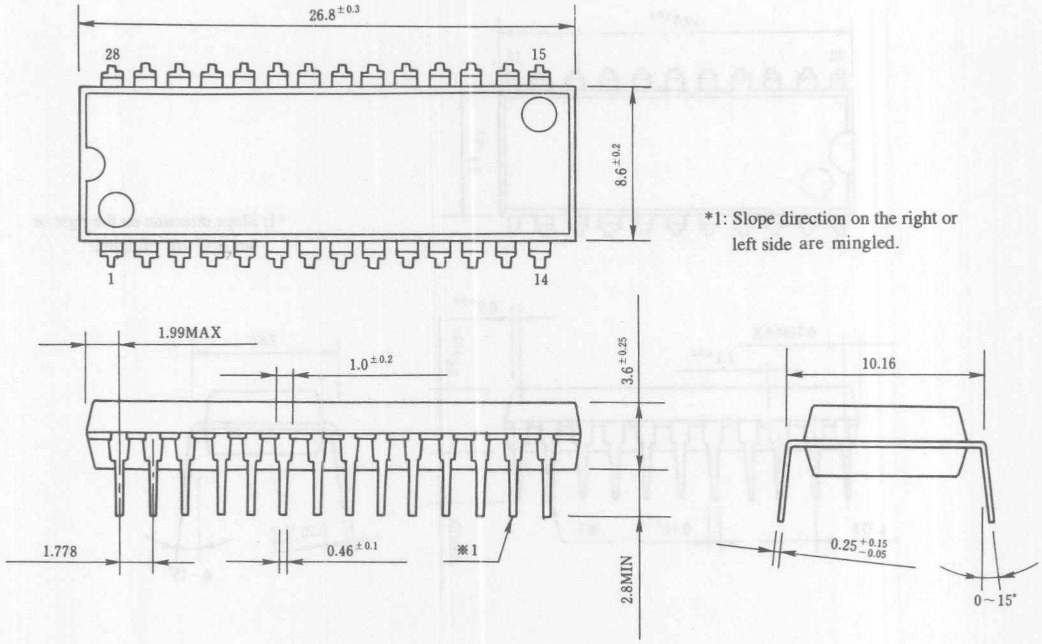
Unit:mm

SDIP24



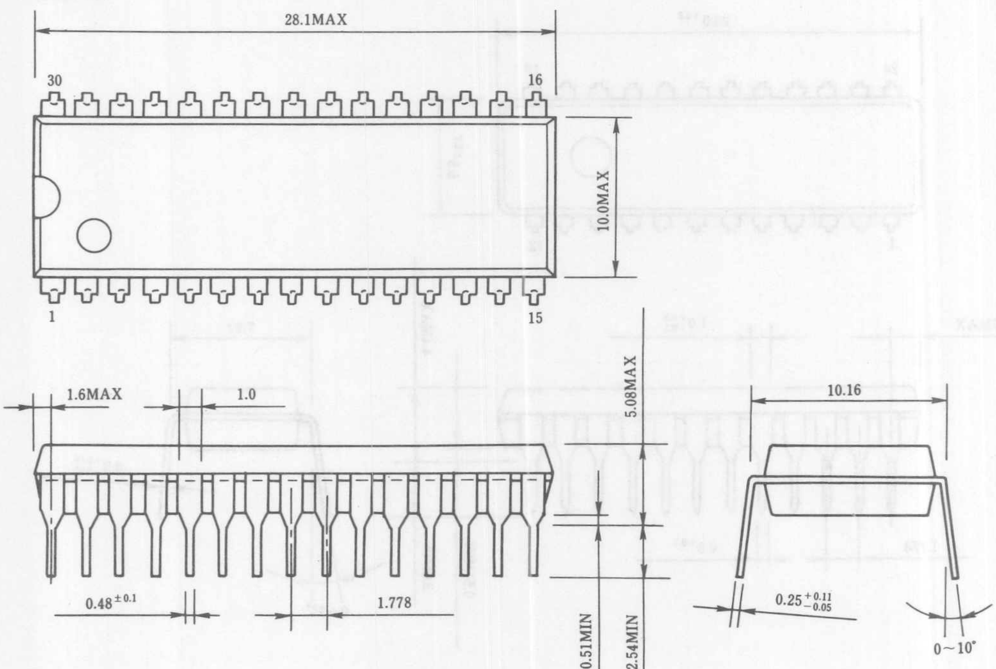
Unit:mm

SDIP28



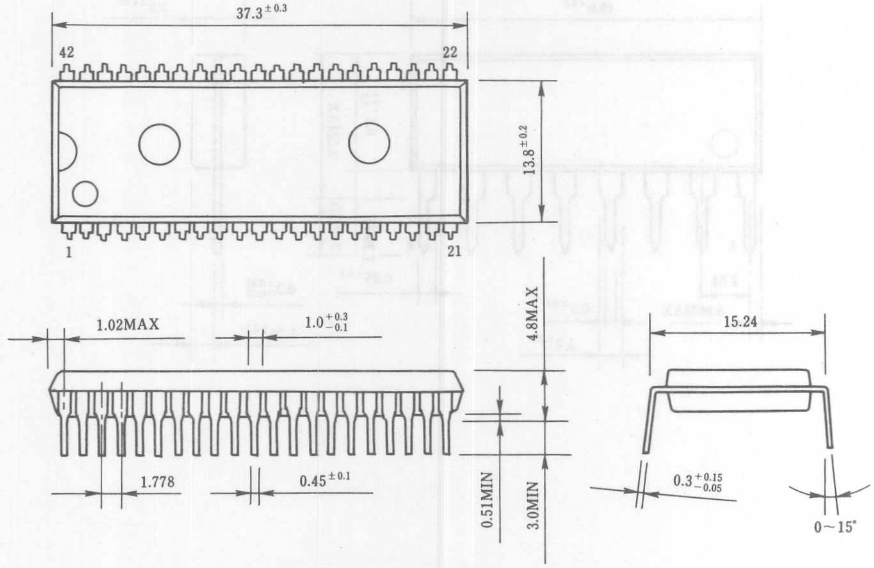
Unit:mm

SDIP30



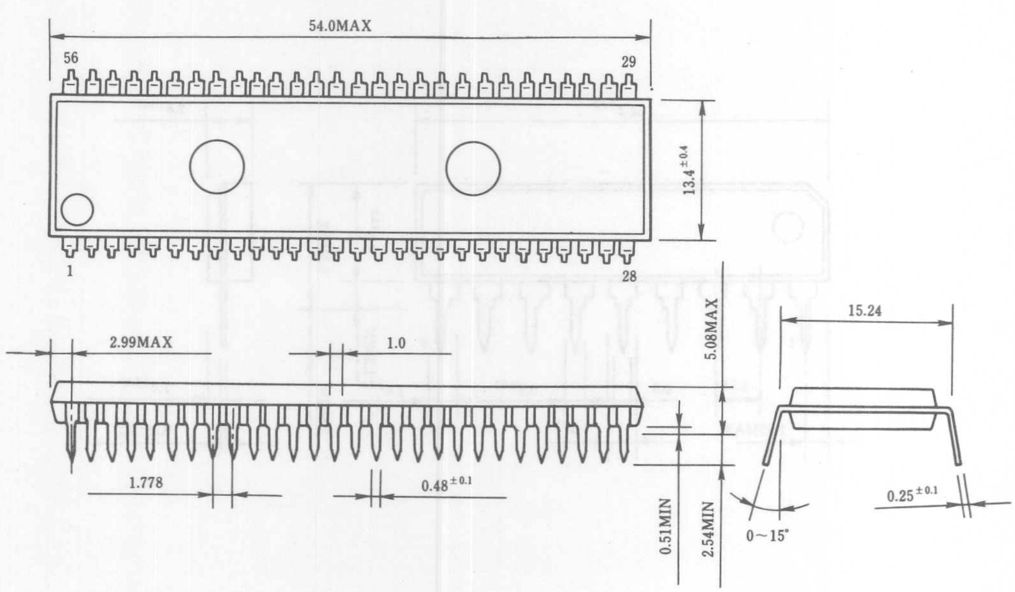
Unit:mm

SDIP42



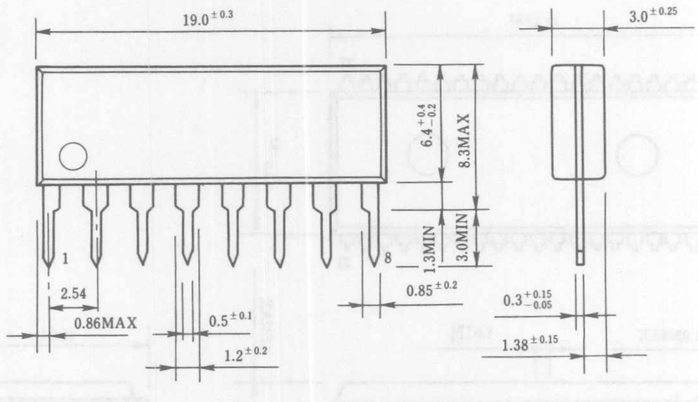
Unit:mm

SDIP56



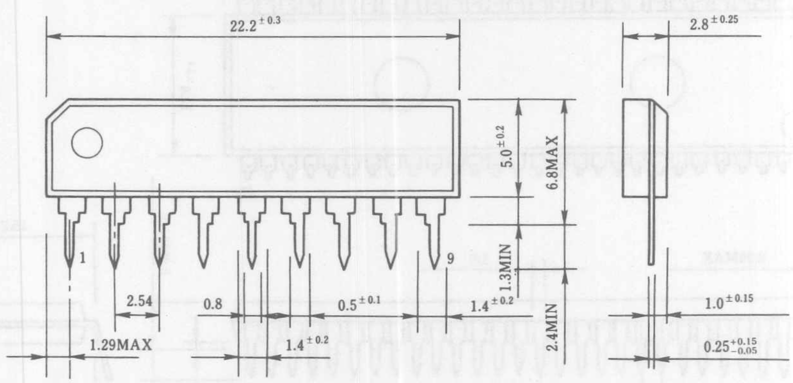
Unit:mm

SIP8



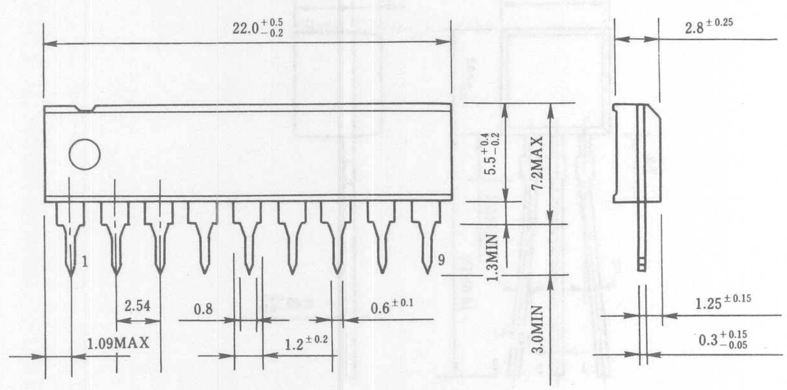
Unit:mm

SIP9



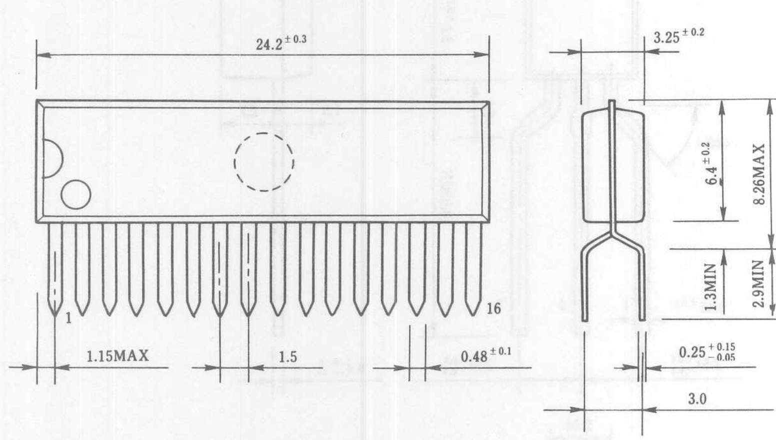
Unit:mm

SIP9＊



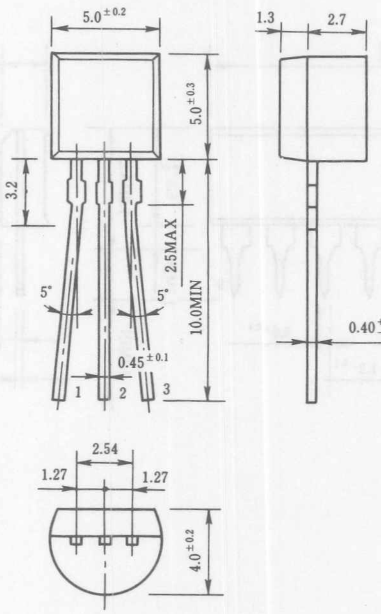
Unit:mm

ZIP16



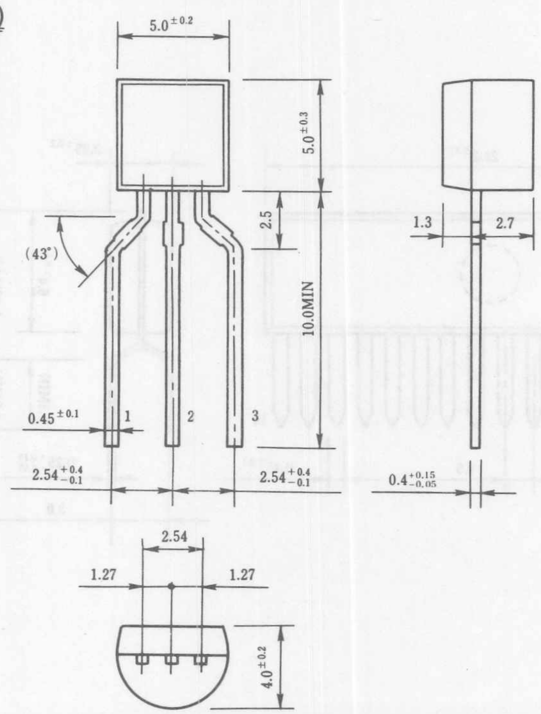
Unit:mm

TO-92(Vinyl Bag)



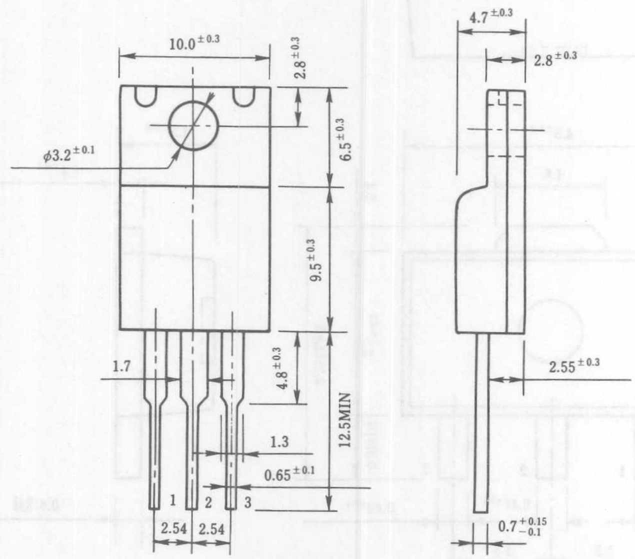
Unit:mm

TO-92(Taping)



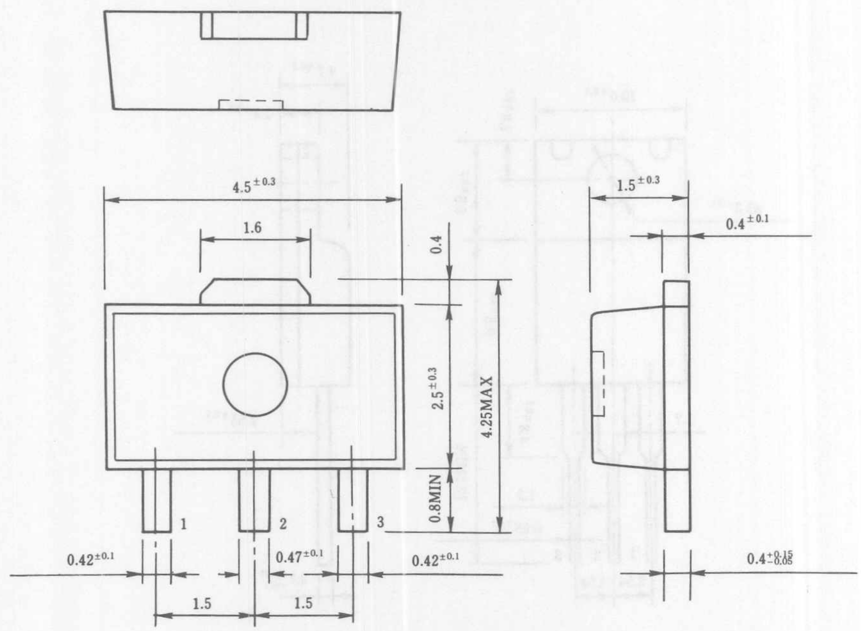
Unit:mm

TO-220F



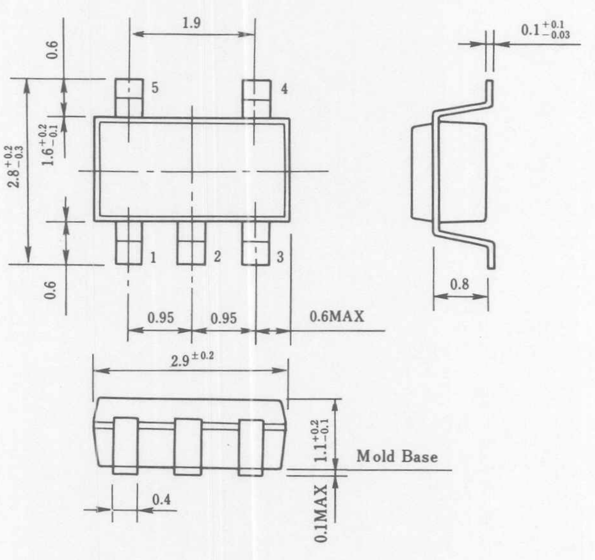
Unit:mm

SOT-89



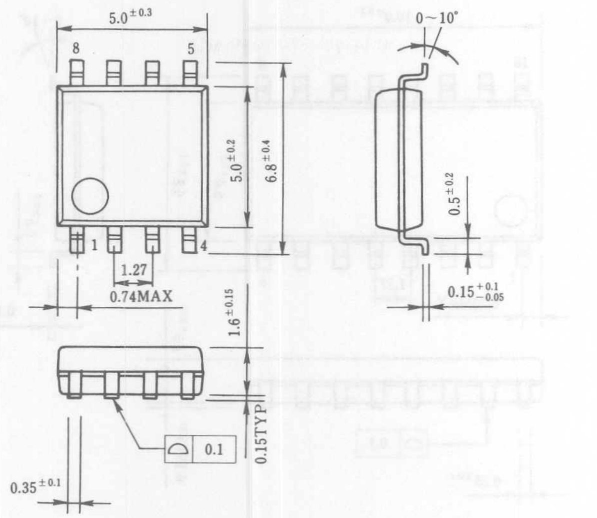
Unit:mm

MTP5



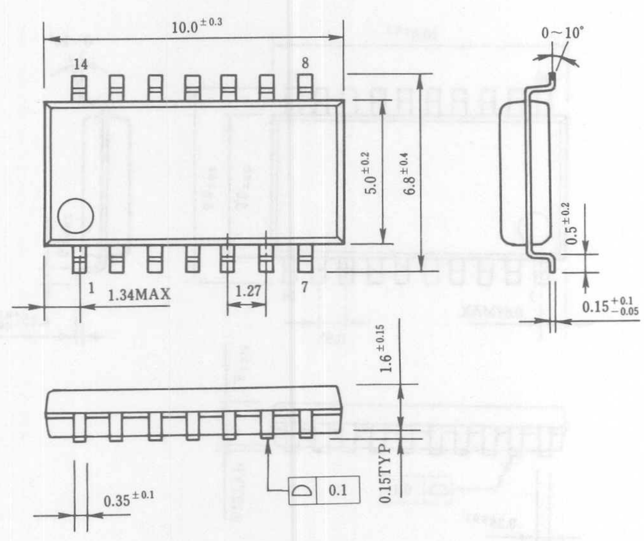
Unit:mm

DMP8



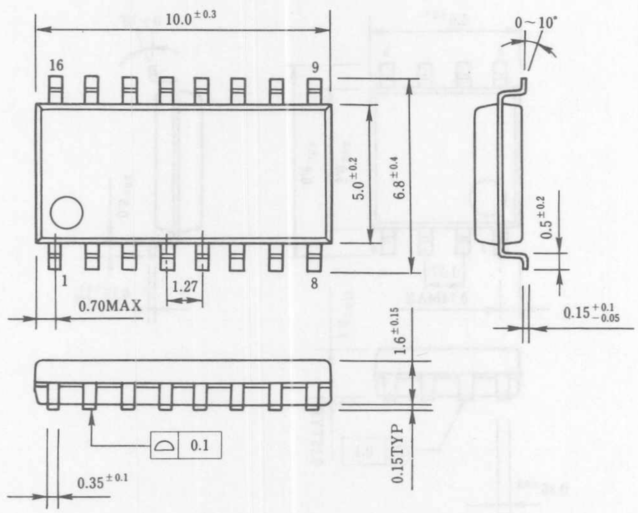
Unit:mm

DMP14



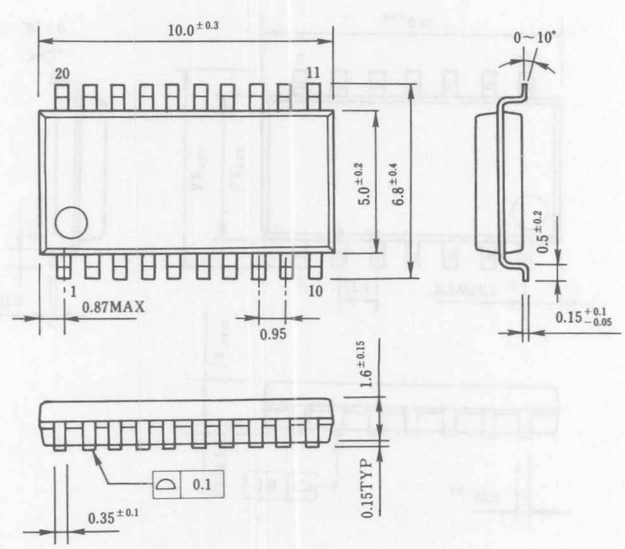
Unit:mm

DMP16



Unit:mm

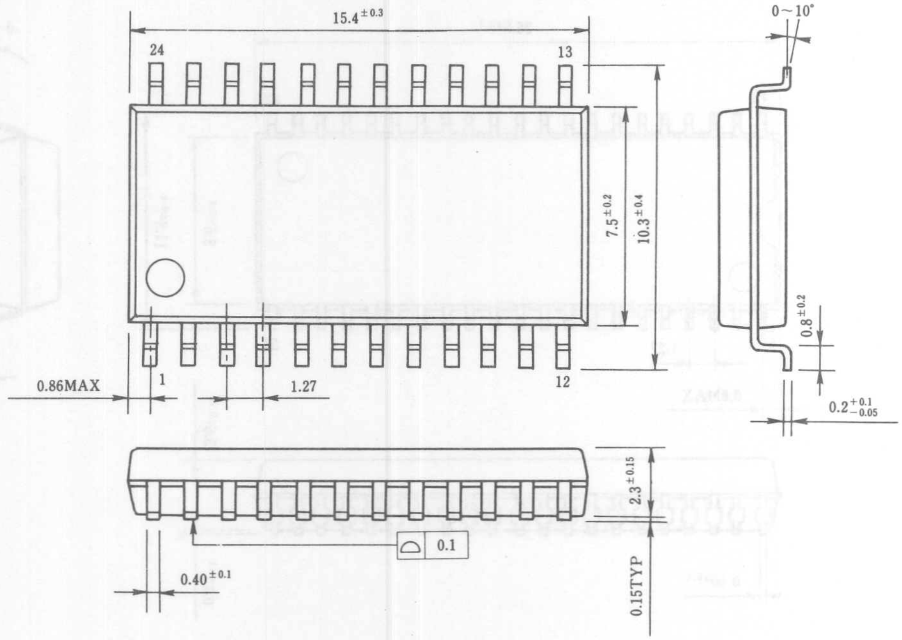
DMP20



Unit:mm

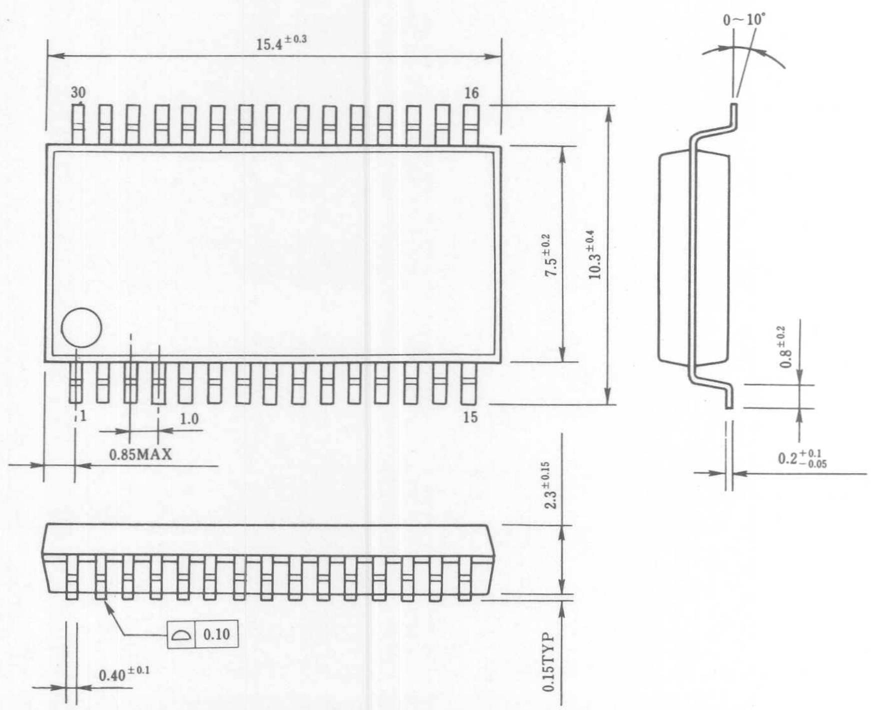
PACKAGE DIMENSIONS

DMP24



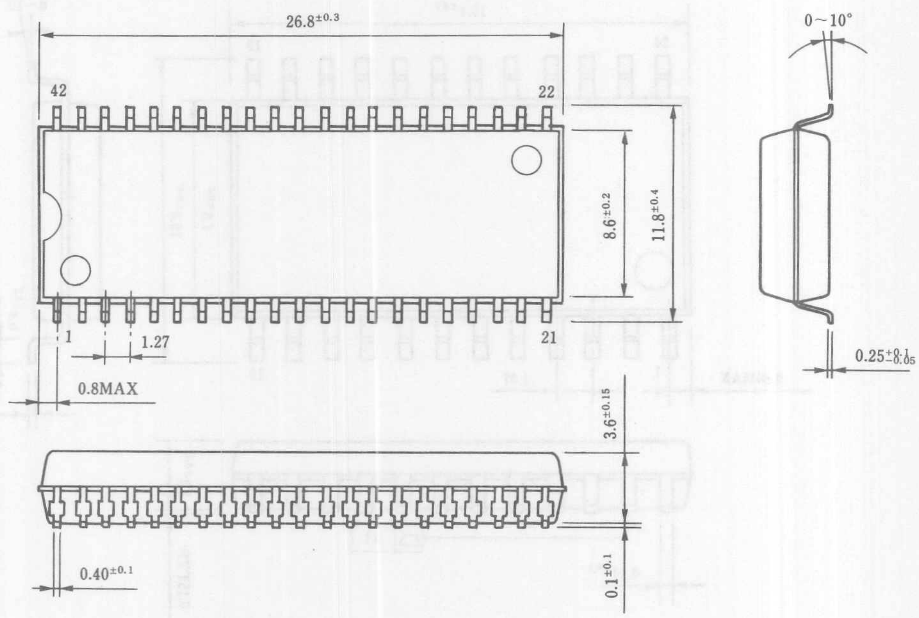
Unit:mm

SDMP30



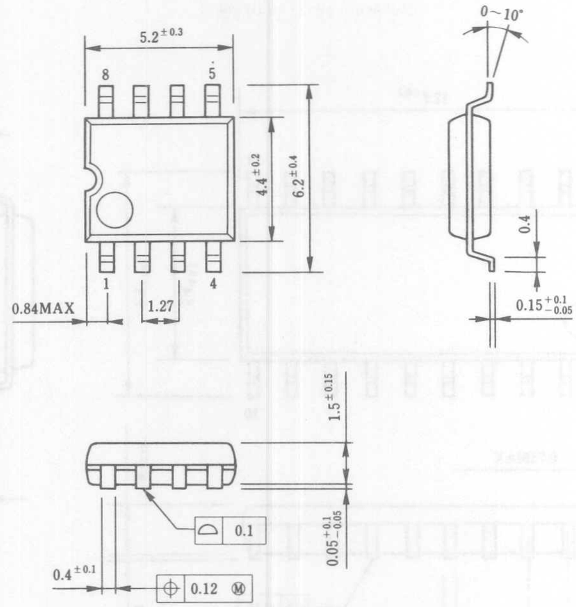
Unit:mm

DMP42



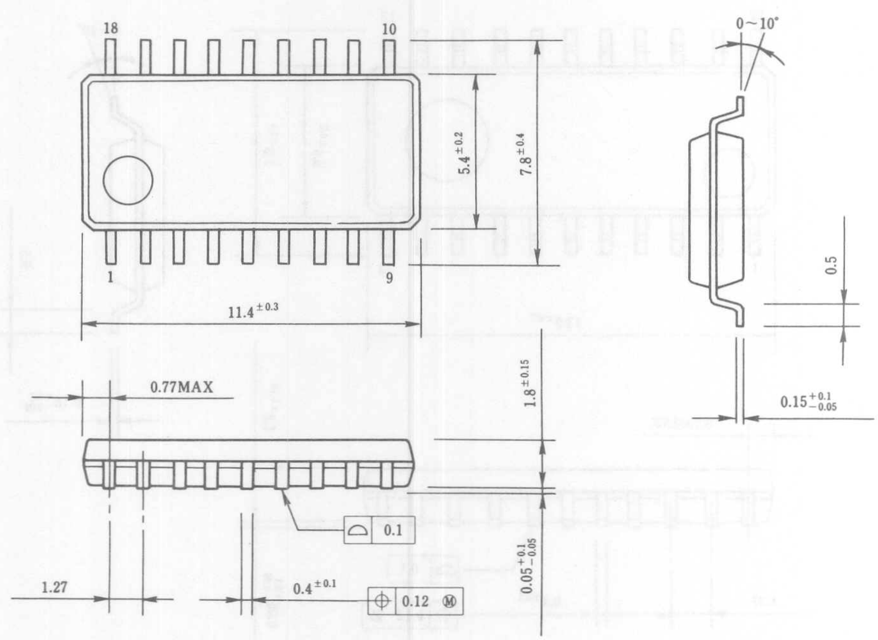
Unit:mm

SOP8



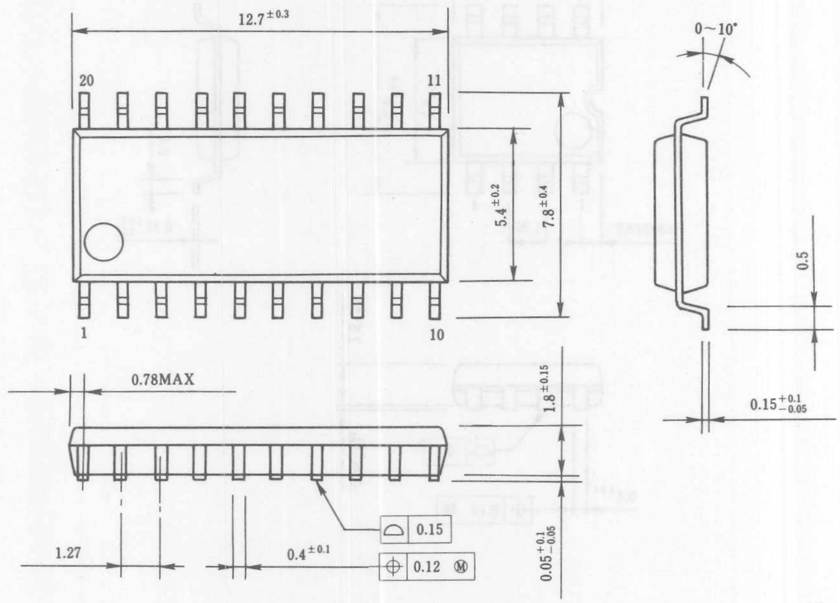
Unit:mm

SOP18



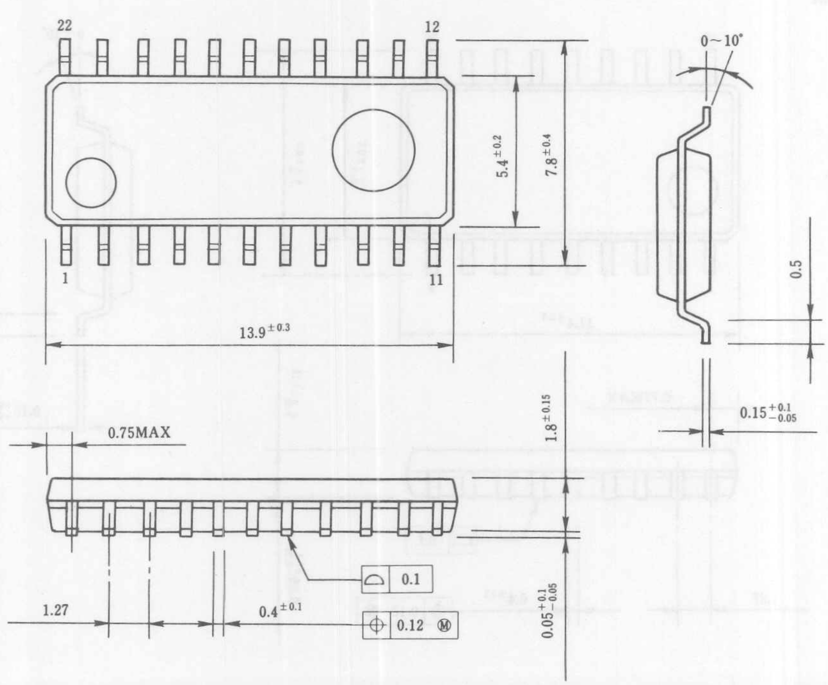
Unit:mm

SOP20



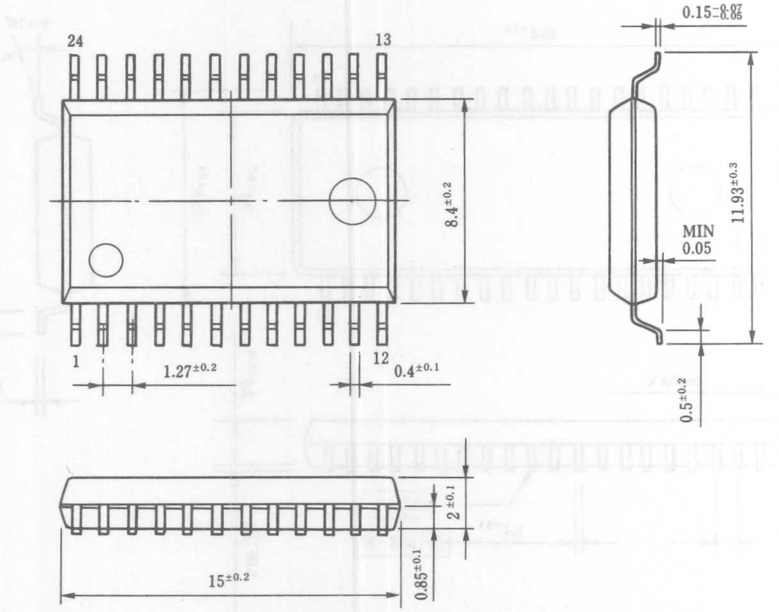
Unit:mm

SOP22



Unit:mm

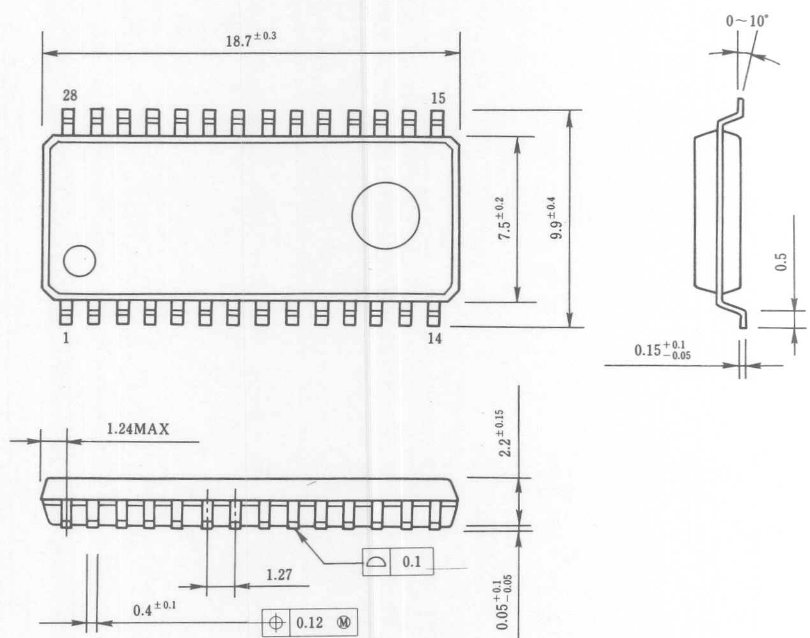
SOP24



Unit:mm

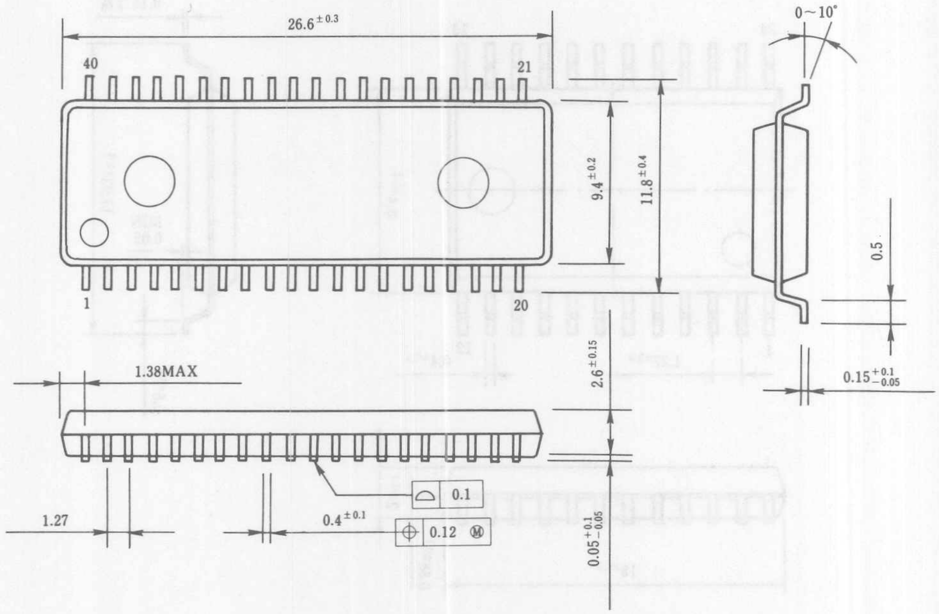
∗This package is applied to only NJU9702.

SOP28



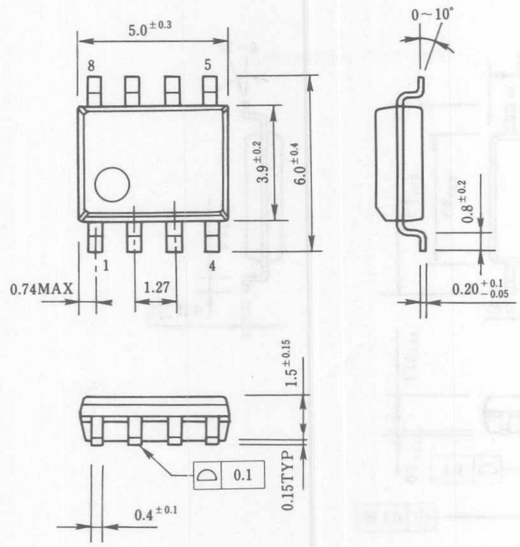
Unit:mm

SOP40



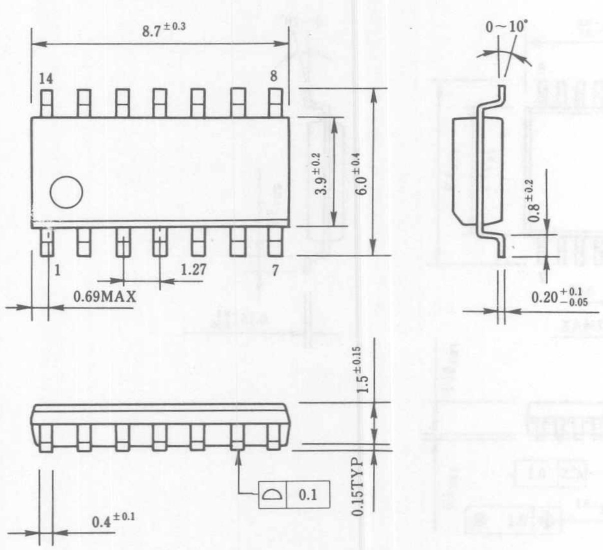
Unit:mm

EMP8



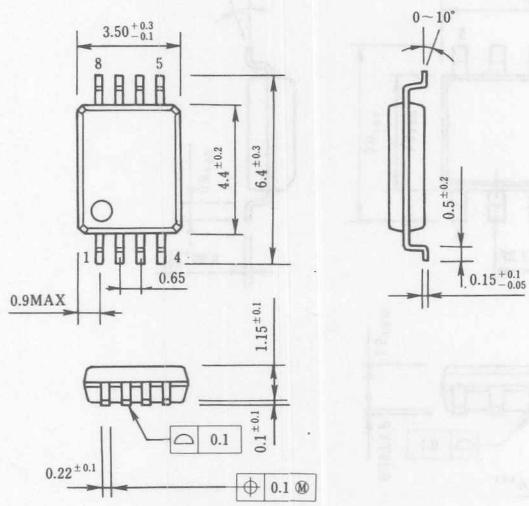
Unit:mm

EMP14



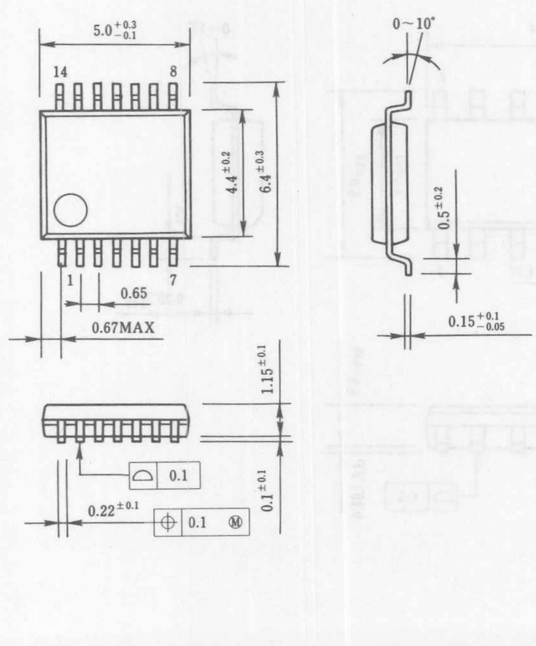
Unit:mm

SSOP8



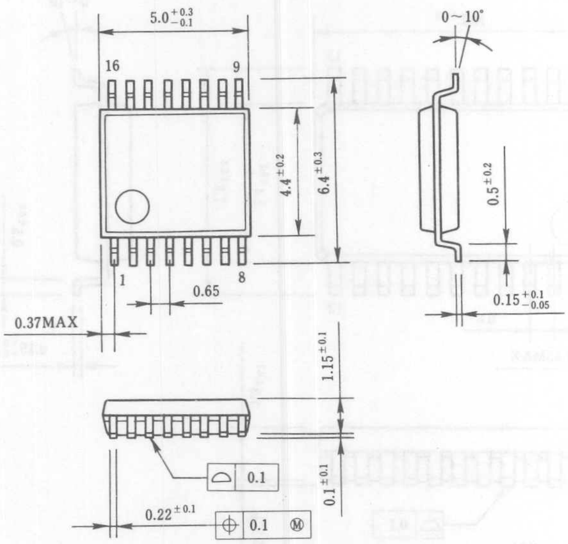
Unit:mm

SSOP14



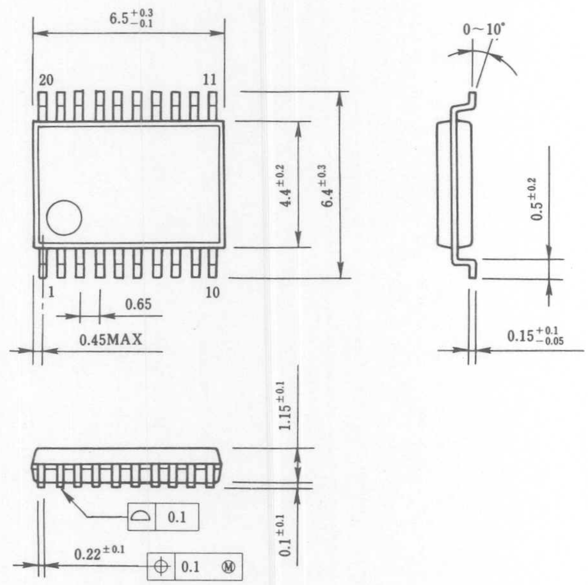
Unit:mm

SSOP16



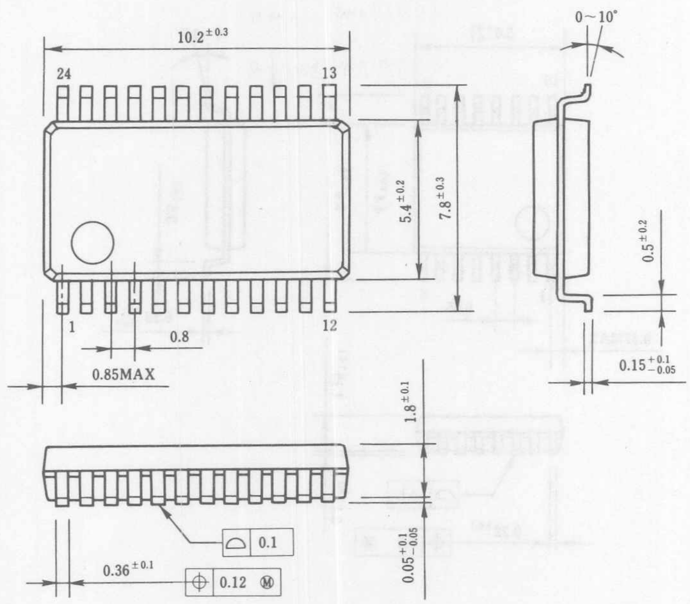
Unit:mm

SSOP20



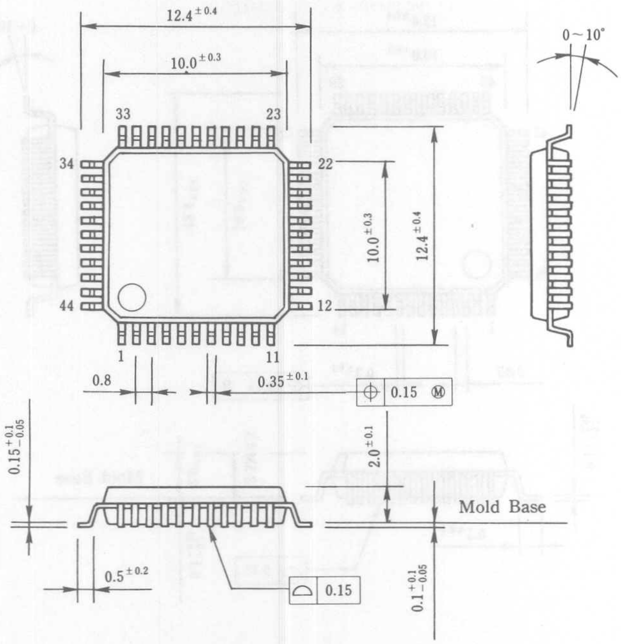
Unit:mm

SSOP24



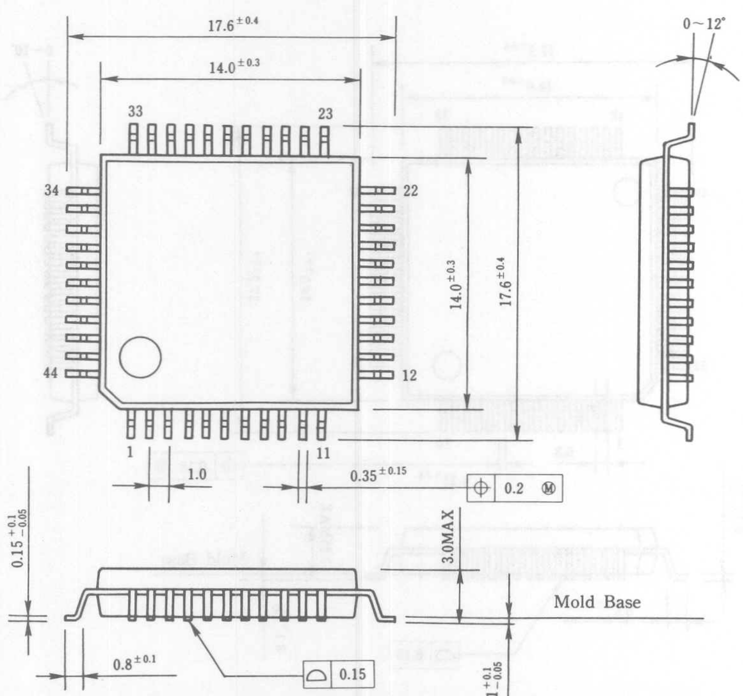
Unit:mm

QFP44-A1



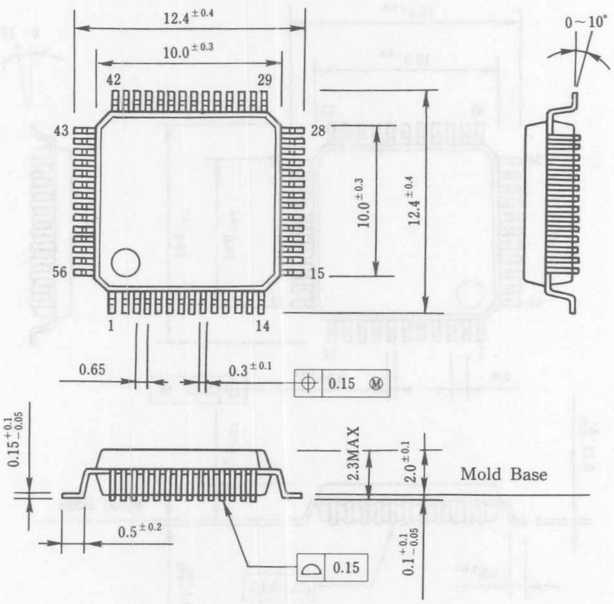
Unit:mm

QFP44-B1



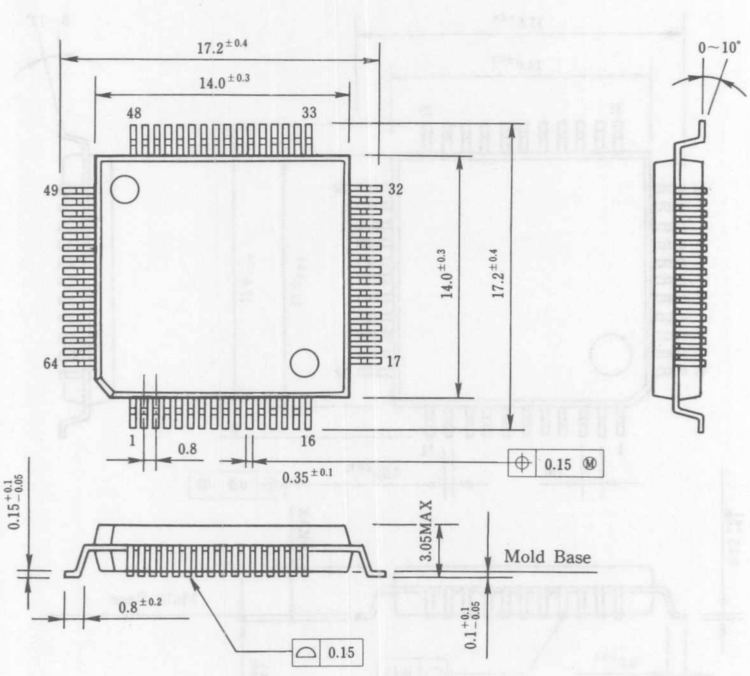
Unit:mm

QFP56-A1



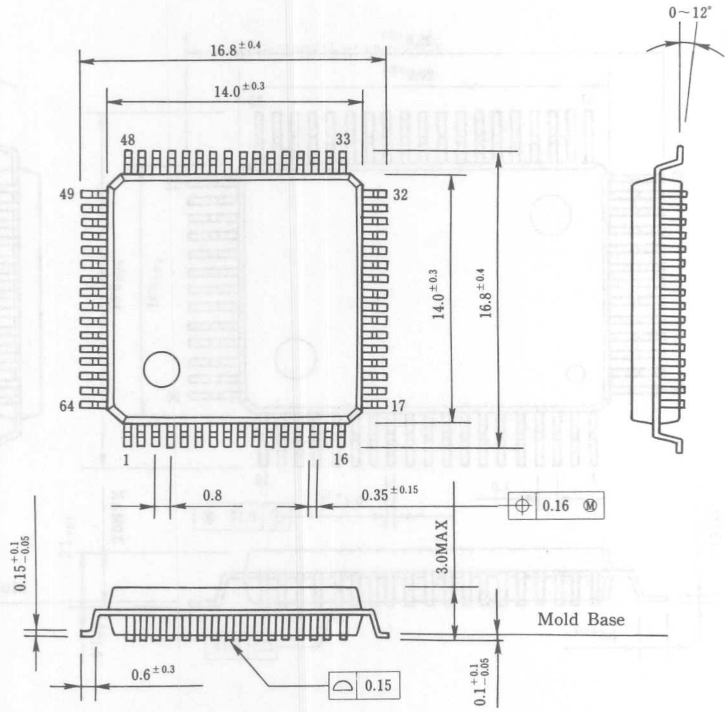
Unit:mm

QFP64-B2



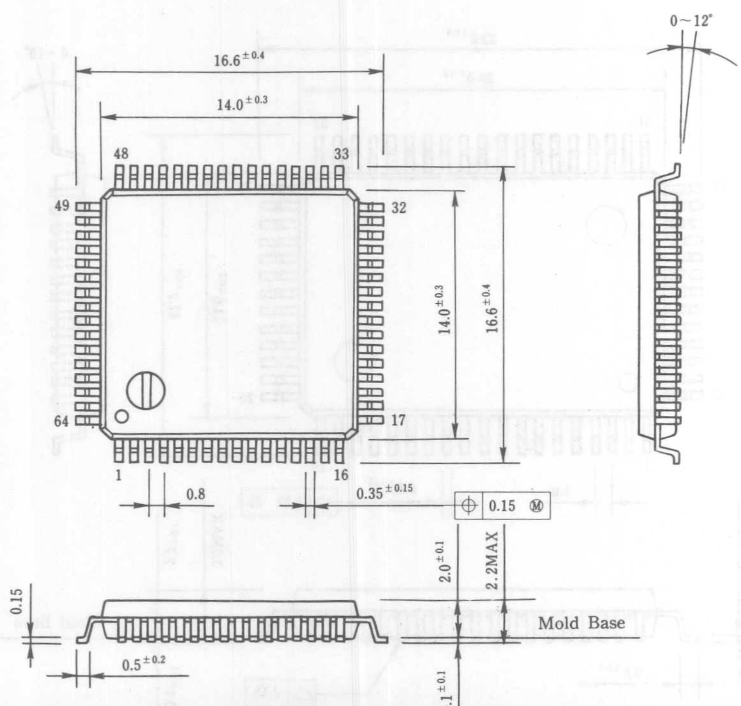
Unit:mm

QFP64-B3



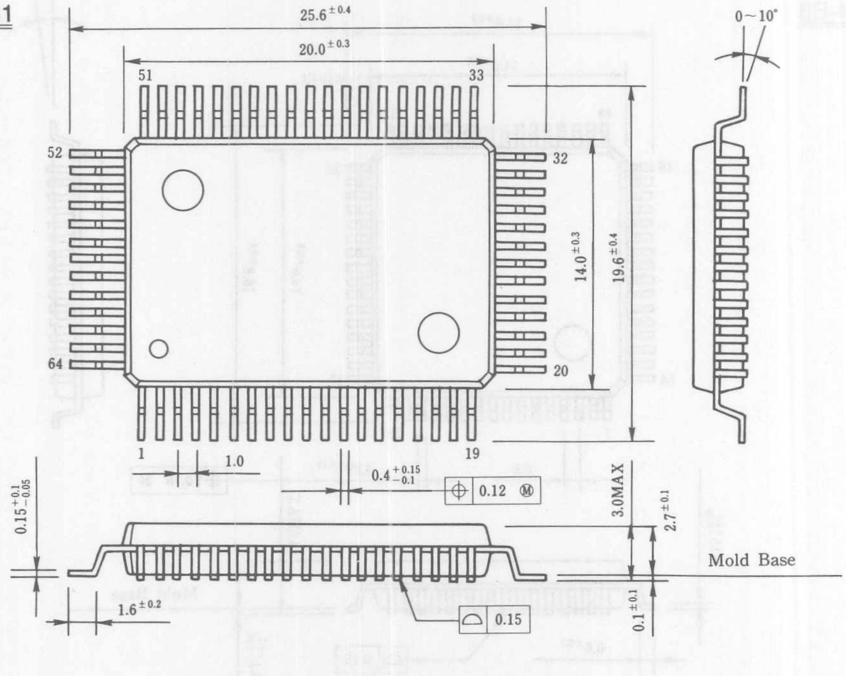
Unit:mm

QFP64-E1



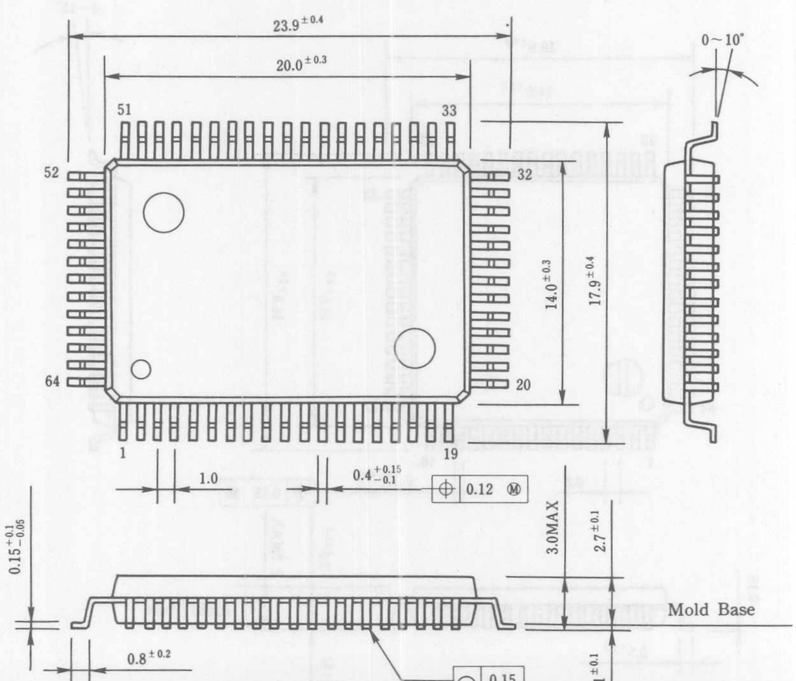
Unit:mm

QFP64-C1



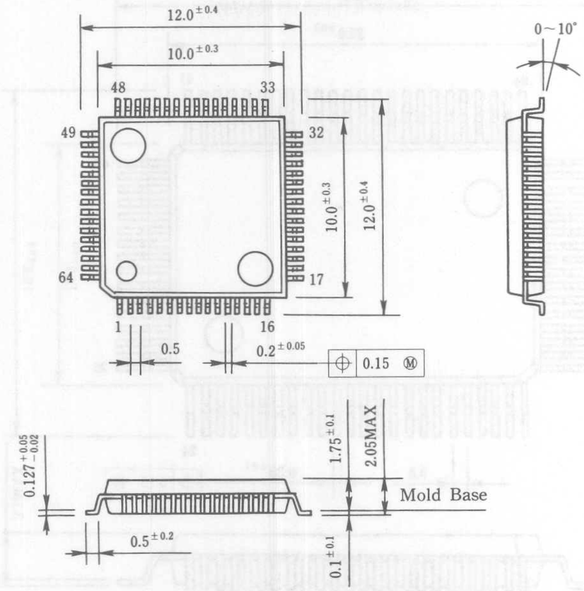
Unit:mm

QFP64-C2



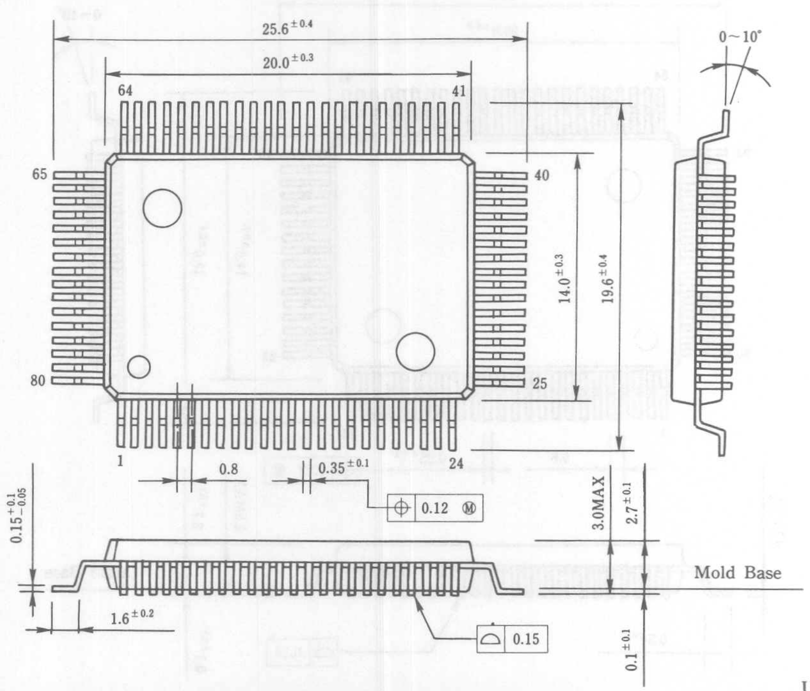
Unit:mm

QFP64-D1



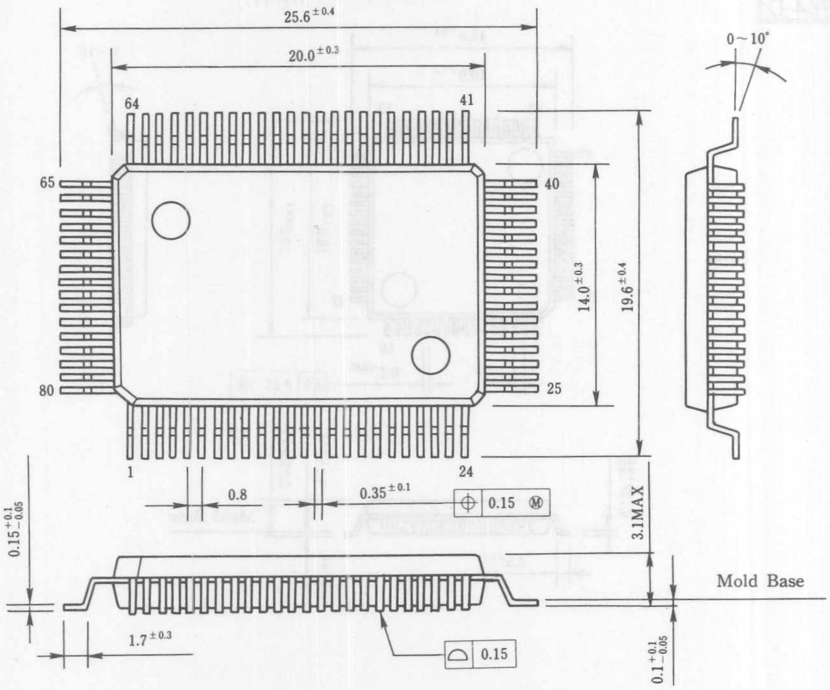
Unit:mm

QFP80-C1(1)



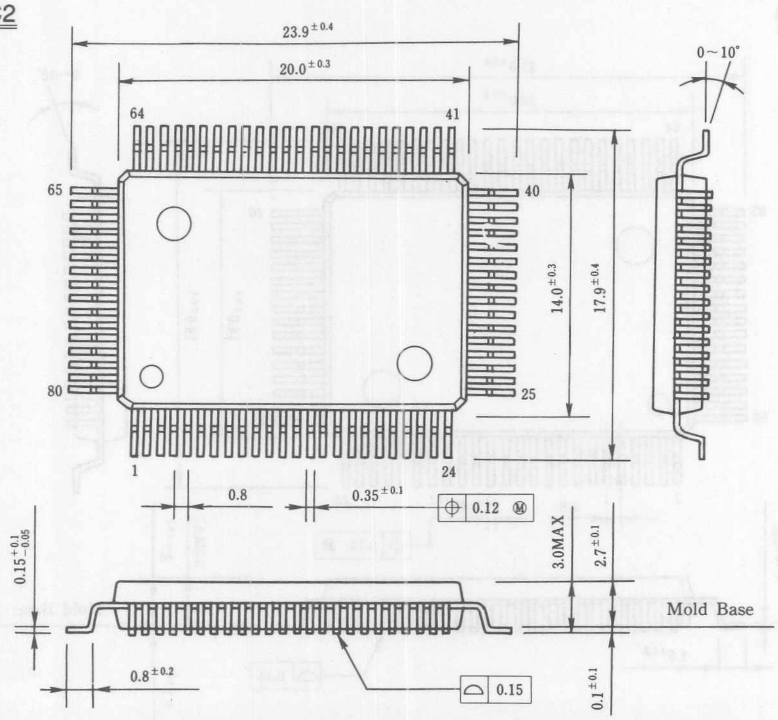
Unit:mm

QFP80-C1(2)



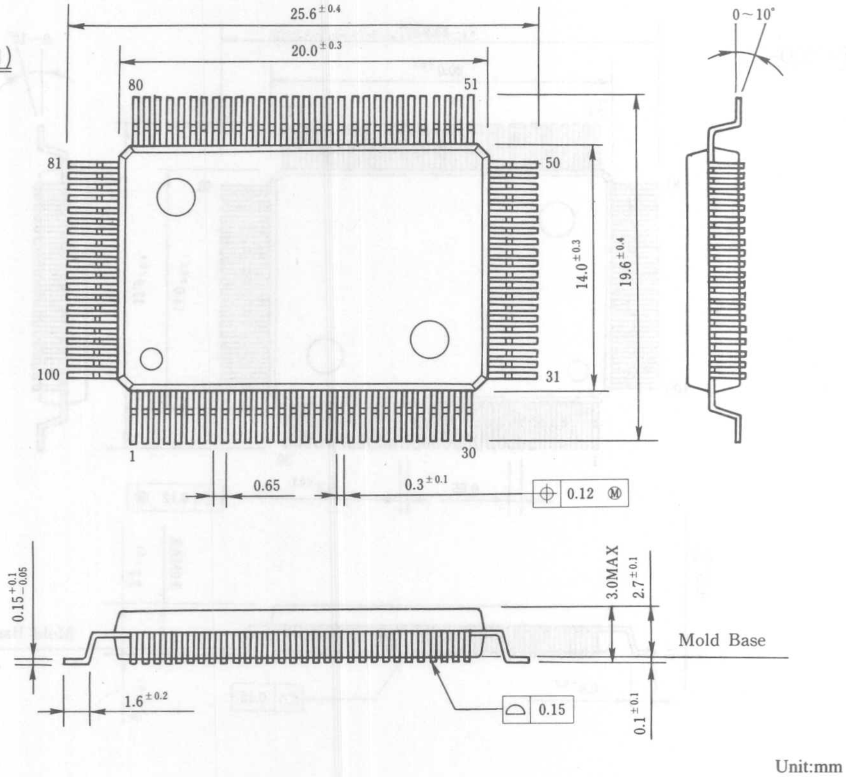
Unit:mm

QFP80-C2

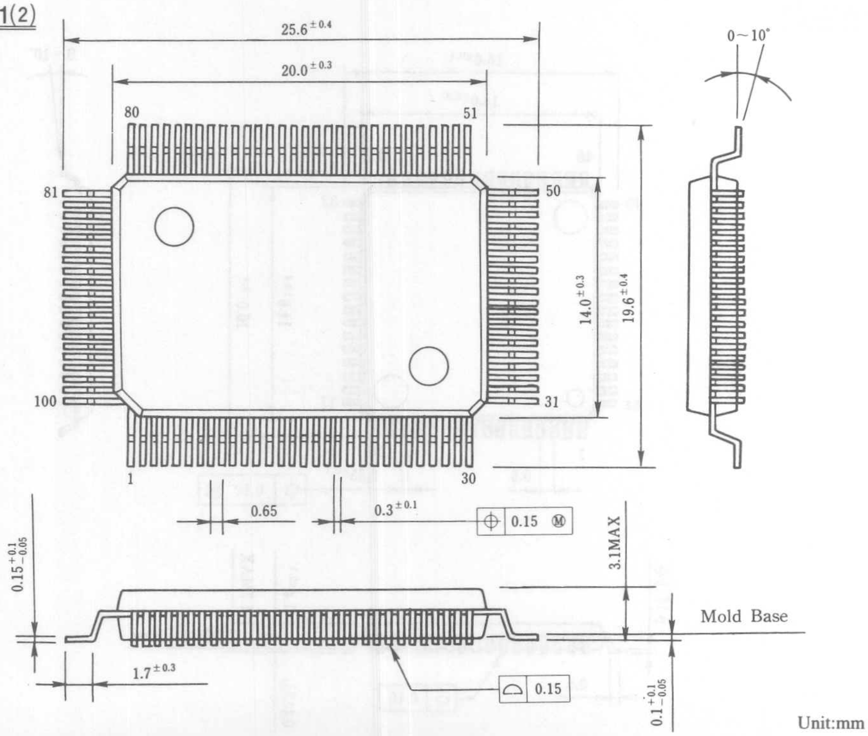


Unit:mm

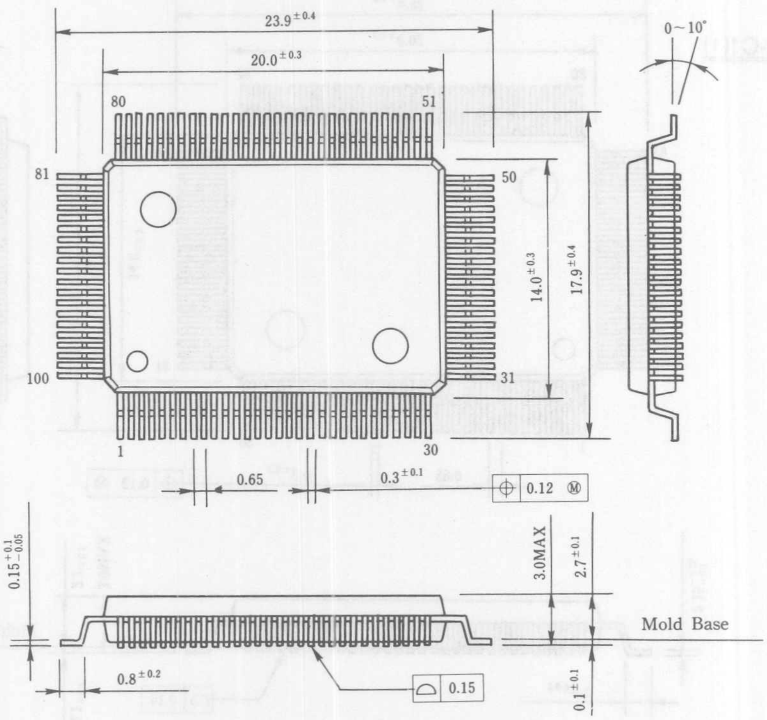
QFP100-C1(1)



QFP100-C1(2)

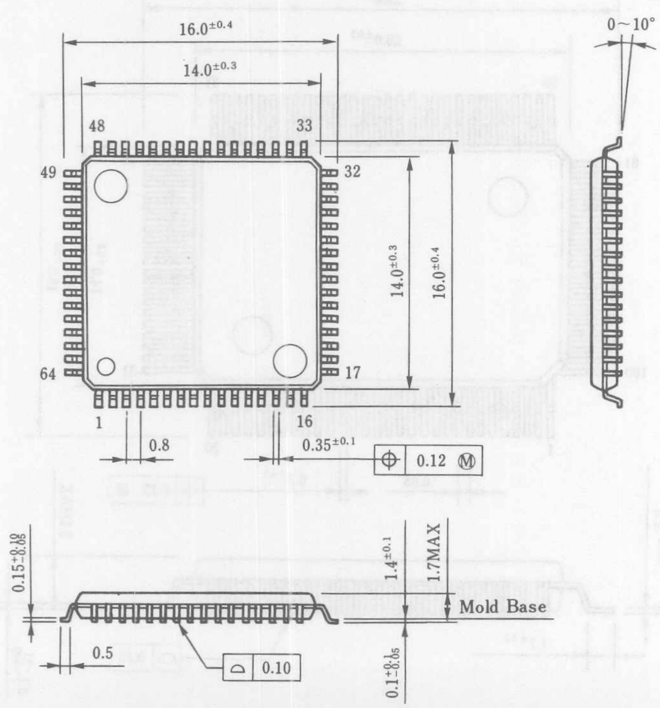


QFP100-C2



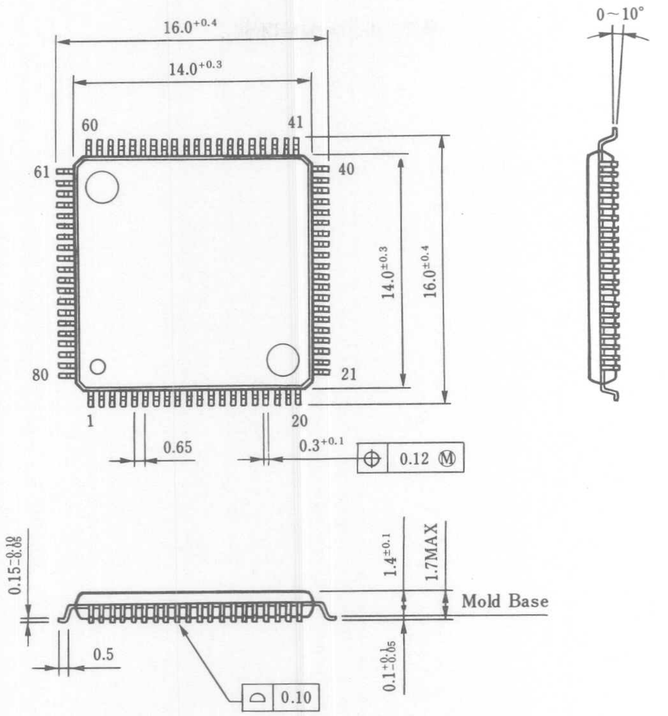
Unit:mm

QFP64-G1



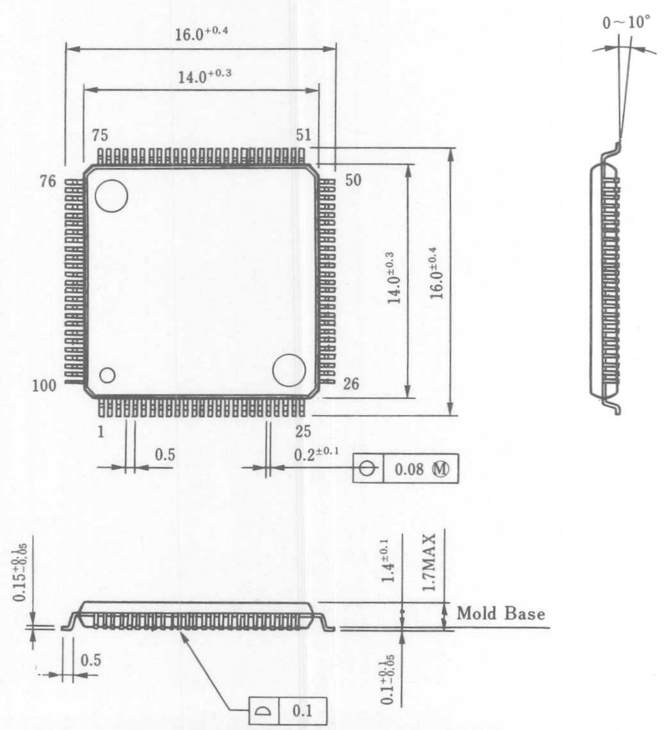
Unit:mm

QFP80-G1



Unit:mm

QFP100-G1



Unit:mm

PACKING 3

GENERAL DESCRIPTION/PACKING SPECIFICATION

■ GENERAL DESCRIPTION

NJRC delivers ICs in 4 methods of plastic tube container, two kind of Taping, tray and vinyl bag packing.

Except adhesive tape treated anti electorostatic and contain carbon are using as the ESD (Electrostatic Discharge Damage) protection.

■ PACKING SPECIFICATION TABLE

PKG	Packing Type				
	Plastic tube	Taping		Tray	Vinyl Bag
		Adhesive	Emboss		
<DIP>					
DIP8	○ 50pcs/tube	—	—	—	—
DIP14	○ 25pcs/tube	—	—	—	—
DIP16	○ 25pcs/tube	—	—	—	—
DIP18	○ 20pcs/tube	—	—	—	—
DIP20	○ 20pcs/tube	—	—	—	—
DIP22	○ 20pcs/tube	—	—	—	—
DIP40	○ 10pcs/tube	—	—	—	—
<SDIP>					
SDIP22	○ 25pcs/tube	—	—	—	—
SDIP24	○ 20pcs/tube	—	—	—	—
SDIP28	○ 20pcs/tube	—	—	—	—
SDIP30	○ 20pcs/tube	—	—	—	—
SDIP42	○ 14pcs/tube	—	—	—	—
SDIP56	○ 10pcs/tube	—	—	—	—
<SIP>					
SIP8	○ 25pcs/tube	—	—	—	—
SIP9	○ 25pcs/tube	—	—	—	—
SIP9 *	○ 20pcs/tube	—	—	—	—
ZIP16	○ 20pcs/tube	—	—	—	—
<TO>					
TO-92	—	○ 2,000pcs/reel 2,000pcs/box	—	—	○ 500pcs/bag
TO-220F	—	—	—	—	○ 100pcs/bag
<SOT / MTP>					
SOT-89	○ 25pcs/tube	—	○ 1,000pcs/reel	—	—
MTP-5	—	—	○ 3,000pcs/reel	—	—

■ Packing Specification Table

PKG	Packing Type				
	Plastic tube	Taping		Tray	Vinyl Bag
		Adhesive	Emboss		
<DMP>					
DMP8	○ 100pcs/tube	○ 2,000pcs/reel	○ 2,000pcs/reel	—	—
DMP14	○ 50pcs/tube	○ 2,000pcs/reel	○ 2,000pcs/reel	—	—
DMP16	○ 50pcs/tube	○ 2,000pcs/reel	○ 2,000pcs/reel	—	—
DMP20	○ 50pcs/tube	○ 2,000pcs/reel	○ 2,000pcs/reel	—	—
DMP24	○ 25pcs/tube	○ 1,500pcs/reel	—	—	—
SDMP30	○ 25pcs/tube	○ 1,500pcs/reel	—	—	—
DMP42	○ 20pcs/tube	—	—	—	—
<SOP>					
SOP8	○ 50pcs/tube	○ 2,000pcs/reel	○ 3,000pcs/reel	—	—
SOP18	○ 25pcs/tube	○ 2,000pcs/reel	○ 2,000pcs/reel	—	—
SOP20	○ 25pcs/tube	○ 2,000pcs/reel	Note ○	—	—
SOP22	○ 25pcs/tube	Note ○	○ 2,000pcs/reel	—	—
SOP28	Note ○	Note ○	○ 2,000pcs/reel	—	—
SOP40	○ 15pcs/tube	—	—	—	—
<EMP>					
EMP8	○ 100pcs/tube	○ 2,000pcs/reel	○ 2,000pcs/reel	—	—
EMP14	○ 50pcs/tube	○ 2,000pcs/reel	○ 2,000pcs/reel	—	—
<SSOP>					
SSOP8	—	—	○ 2,000pcs/reel	—	—
SSOP14	—	—	○ 2,000pcs/reel	—	—
SSOP16	—	—	○ 2,000pcs/reel	—	—
SSOP20	—	—	○ 2,000pcs/reel	—	—
SSOP24	—	Note ○	○ 2,000pcs/reel	—	—

Note ○ : Examination for customer's request

■ Packing Specification Table

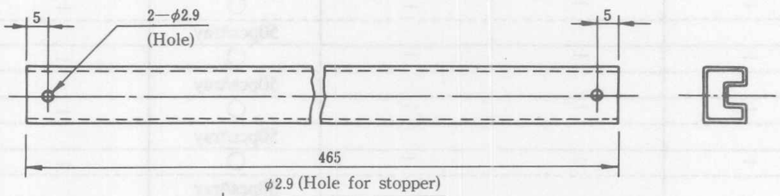
PKG	Packing Type				
	·Plastic tube	Taping		Tray	Vinyl Bag
		Adhesive	Emboss		
<QFP>					
QFP44 －＊＊	–	–	–	○ 50pcs/tray	–
QFP56 －＊＊	–	–	–	○ 50pcs/tray	–
QFP64 －＊＊	–	–	–	○ 50pcs/tray	–
QFP80 －＊＊	–	–	–	○ 50pcs/tray	–
QFP100 －＊＊	–	–	–	○ 50pcs/tray	–
<TAB>	Q'ty depends on product type (Reel or Tray).				
<CHIP>	Q'ty depends on product type (Tray only).				
<WAFER>	Q'ty depends on product type .				

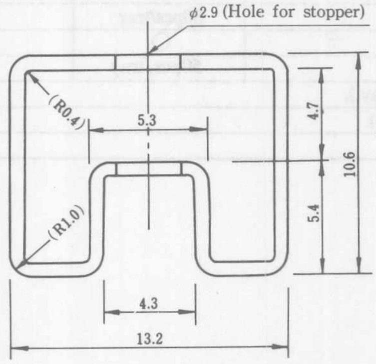
■ Plastic Tube Container Dimensions

DIP, SDIP, SIP, ZIP, DMP, SDMP, SOP, EMP, SOT packages can pack in the plastic tube container the dimensions are mentioned as follows.

1.Plastic Tube Container for dual-in-line plastic mold

(1) Plastic Tube Container dimensions for DIP8

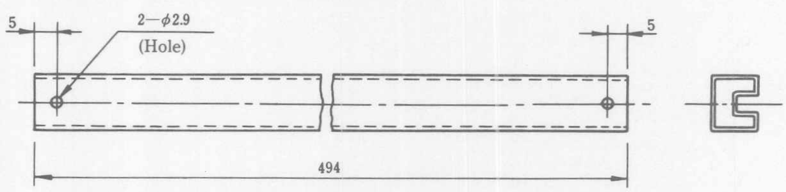


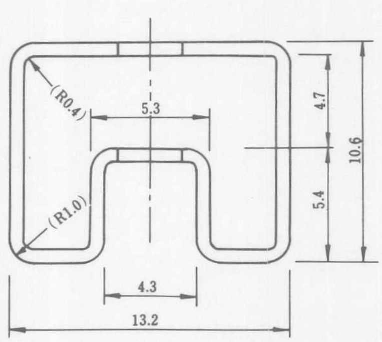


1.Thickness 0.5
2.Material PVC
3.Stopper Stick Pin
4.Contents DIP8-50pcs/tube

Unit:mm

(2) Plastic Tube Container dimensions for DIP14/16

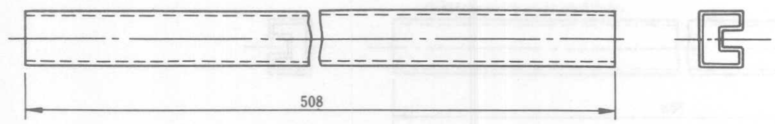


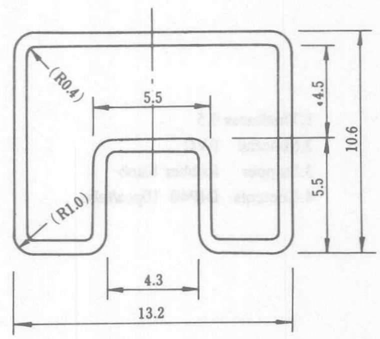


1.Thickness 0.5
2.Material PVC
3.Stopper Stick Pin
4.Contents DIP14-25pcs/tube
DIP16-25pcs/tube

Unit:mm

(3) Plastic Tube Container dimensions for DIP18/20

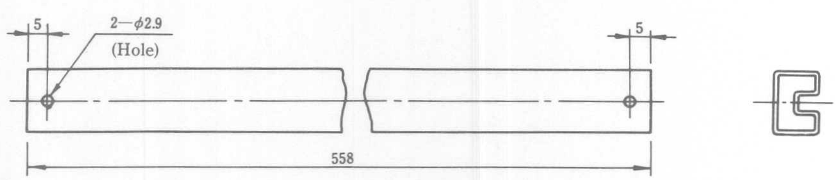


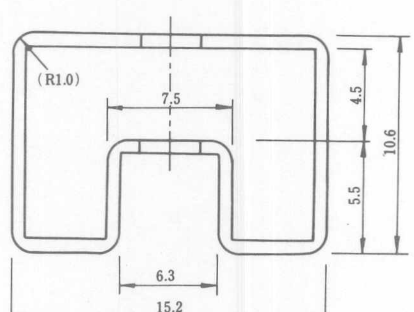


1.Thickness 0.6
2.Material PVC
3.Stopper Rubber Knob
4.Contents DIP20-20pcs/tube

Unit:mm

(4) Plastic Tube Container dimensions for DIP22/DMP42

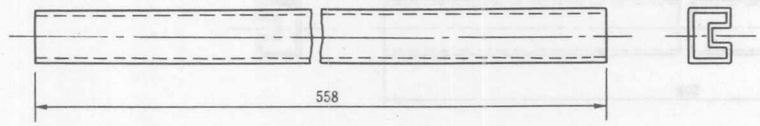


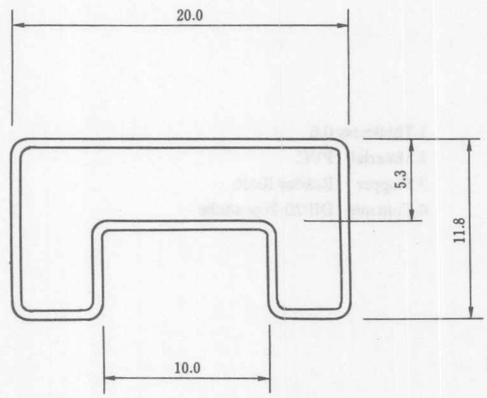


1.Thickness 0.6
2.Material PVC
3.Stopper Stick Pin
4.Contents DIP22-20pcs/tube

Unit:mm

(5) Plastic Tube Container dimensions for DIP40



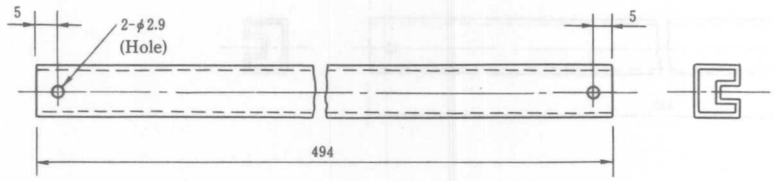


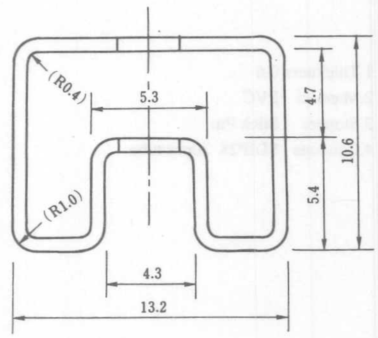
1.Thickness 0.5
2.Material PVC
3.Stopper Rubber Knob
4.Contents DIP40 10pcs/tube

Unit:mm

2.Plastic Tube Container for shrunk dual-in-line plastic mold

(1) Plastic Tube Container dimensions for SDIP22

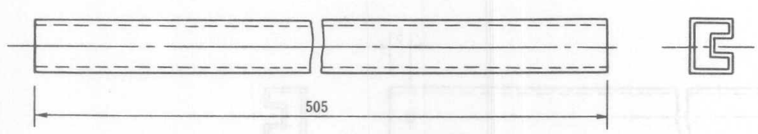


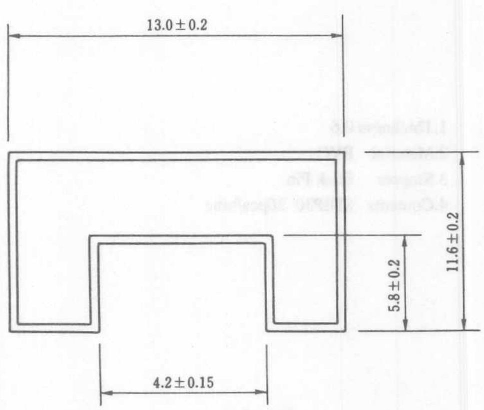


1.Thickness 0.5
2.Material PVC
3.Stopper Stick Pin
4.Contents SDIP22-25pcs/tube

Unit:mm

(2) Plastic Tube Container dimensions for SDIP24

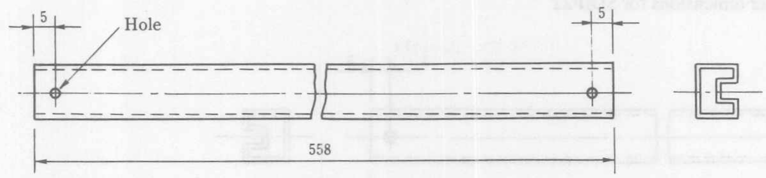


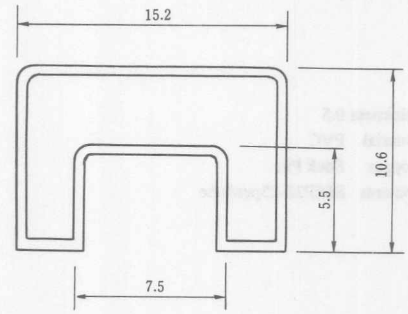


1.Thickness 0.5
2.Material PVC
3.Stopper Rubber Knob
4.Contents SDIP24 20pcs/tube

Unit:mm

(3) Plastic Tube Container dimensions for SDIP28

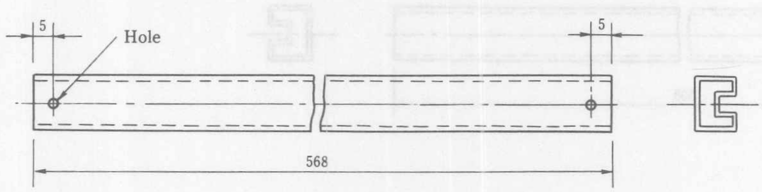


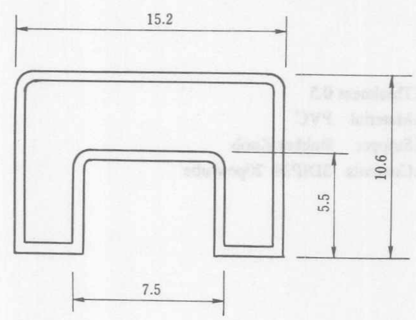


1.Thickness 0.6
2.Material PVC
3.Stopper Stick Pin
4.Contents SDIP28 20pcs/tube

Unit:mm

(4) Plastic Tube Container dimensions for SDIP30

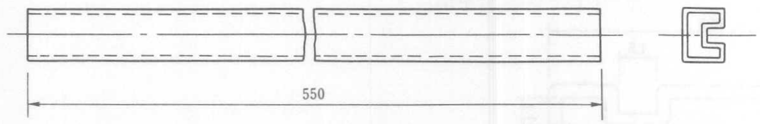


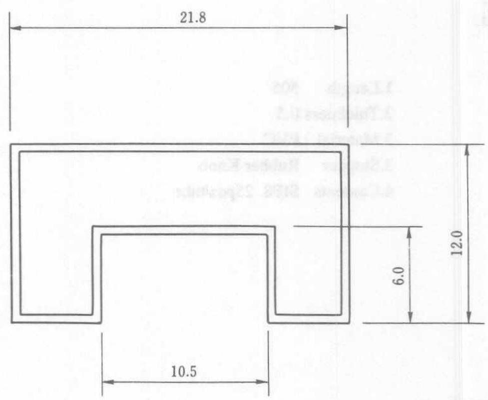


1.Thickness 0.6
2.Material PVC
3.Stopper Stick Pin
4.Contents SDIP30 20pcs/tube

Unit:mm

(5) Plastic Tube Container dimensions for SDIP42

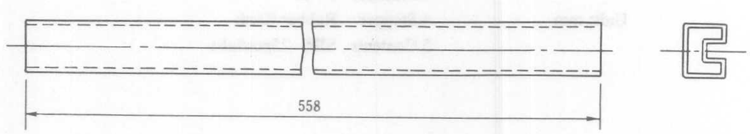


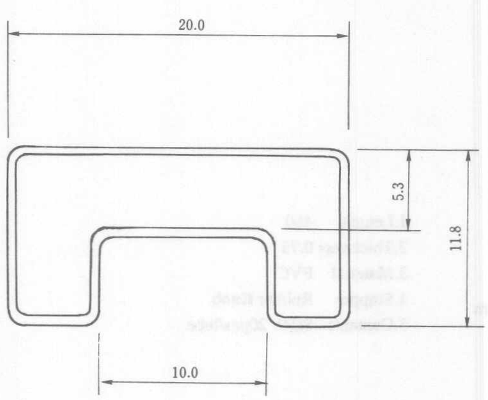


1.Thickness 0.5
2.Material PVC
3.Stopper Rubber Knob
4.Contents SDIP42 14pcs/tube

Unit:mm

(6) Plastic Tube Container dimensions for SDIP56



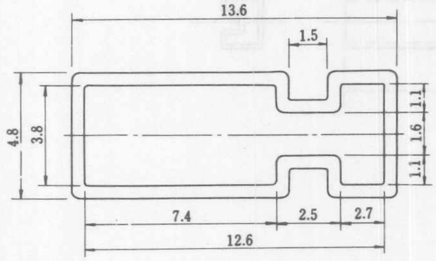


1.Thickness 0.5
2.Material PVC
3.Stopper Rubber Knob
4.Contents SDIP56 10pcs/tube

Unit:mm

3.Plastic Tube Container for single-in-line plastic mold

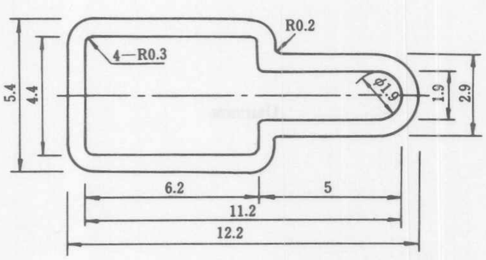
(1) Plastic Tube Container dimensions for SIP8



Unit: mm

1.Length 505
2.Thickness 0.5
3.Material PVC
3.Stopper Rubber Knob
4.Contents SIP8 25pcs/tube

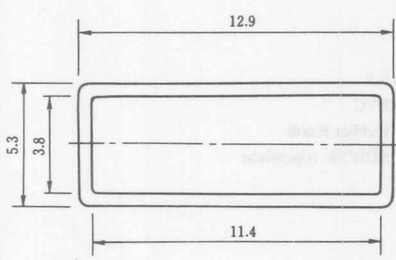
(2) Plastic Tube Container dimensions for SIP9



Unit: mm

1.Length 580±2
2.Thickness 0.5
3.Material PVC
4.Stopper Rubber Knob
5.Contents SIP9 25pcs/tube

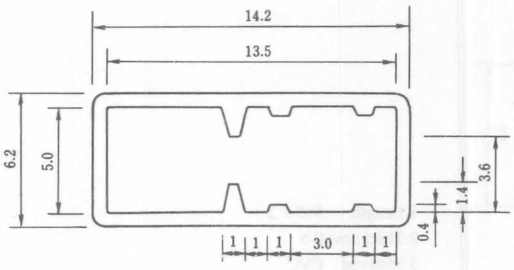
(3) Plastic Tube Container dimensions for SIP9※



Unit: mm

1.Length 460
2.Thickness 0.75
3.Material PVC
4.Stopper Rubber Knob
5.Contents SIP9 20pcs/tube

(4) Plastic Tube Container dimensions for ZIP16

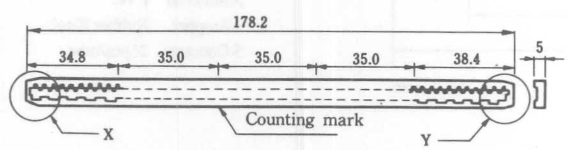


1.Length 513
2.Thickness 0.6
3.Material PVC
4.Stopper Rubber Knob
5.Contents ZIP16 20pcs/tube

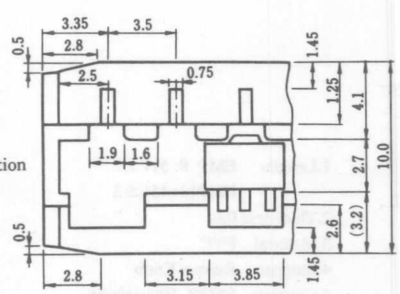
Unit: mm

4.Plastic Tube Container for Three terminal plastic mini mold

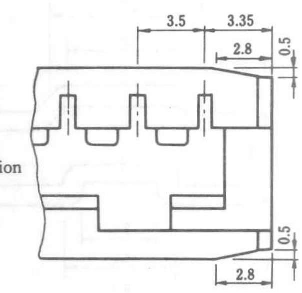
(1) Plastic Tube Container dimensions for SOT89



Magnification of X-part



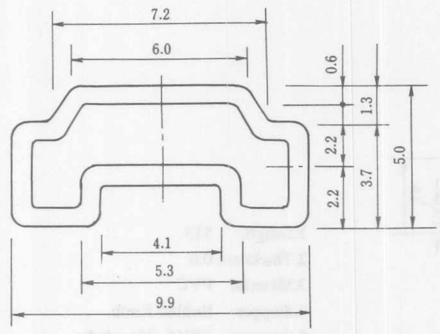
Magnification of Y-part



Unit: mm

5.Plastic Tube Container for dual-in-line plastic mini mold

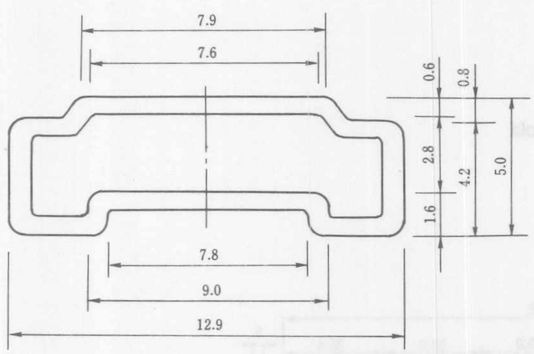
(1) Plastic Tube Container dimensions for DMP8/14/16/20



Unit: mm

1.Length 515±2
2.Thickness 0.6
3.Material PVC
4.Stopper Rubber Knob
5.Contents DMP8 100pcs/tube
DMP14/16/20 50pcs/tube

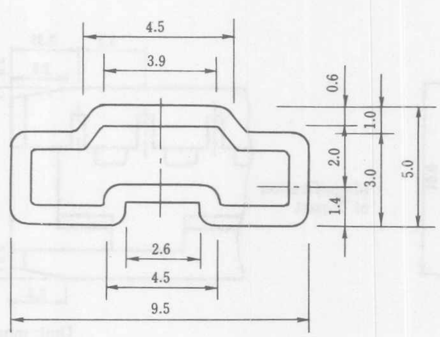
(2) Plastic Tube Container dimensions for DMP24/SDMP30



Unit: mm

1.Length 410±2
2.Thickness 0.6
3.Material PVC
4.Stopper Rubber Knob
5.Contents 25pcs/tube

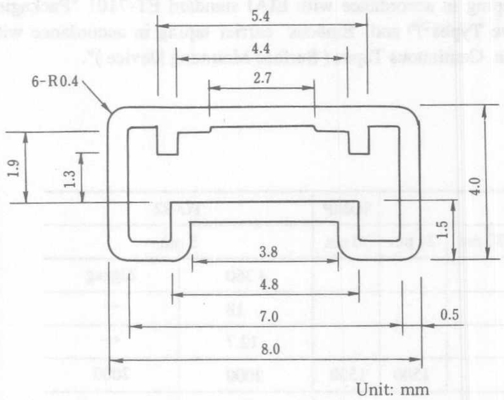
(3) Plastic Tube Container dimensions for EMP8/14



Unit: mm

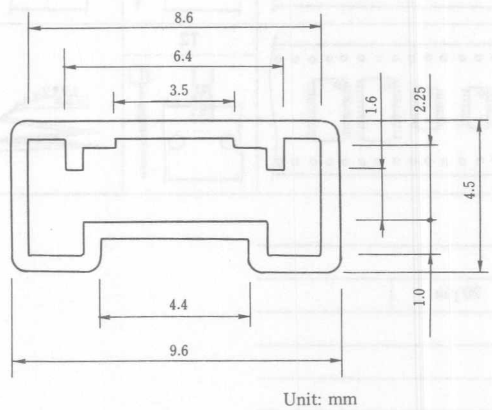
1.Length EMP 8: 517±2
EMP14: 454±2
2.Thickness 0.6
3.Material PVC
4.Stopper Rubber Knob
5.Contents EMP8 100pcs/tube
EMP14 50pcs/tube

(4) Plastic Tube Container dimensions for SOP8



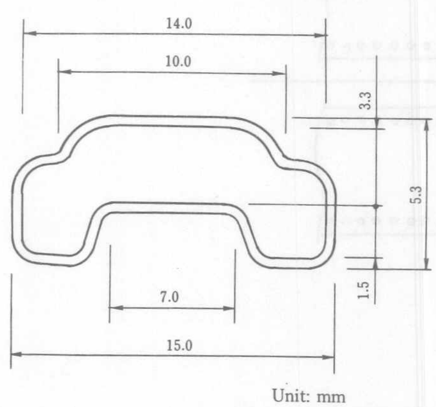
1.Length 280.5
2.Thickness 0.5
3.Material PVC
4.Stopper Rubber Knob
5.Contents SOP8 50pcs/tube

(5) Plastic Tube Container dimensions for SOP18/20/22



1.Length 400
2.Thickness 0.5
3.Material PVC
4.Stopper Rubber Knob
5.Contents SOP18 25pcs/tube
SOP20 25pcs/tube
SOP22 25pcs/tube

(6) Plastic Tube Container dimensions for SOP40

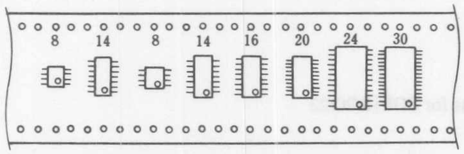
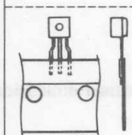
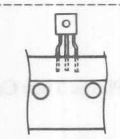
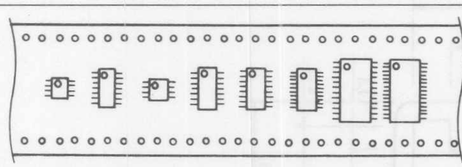
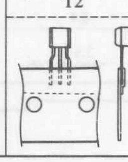
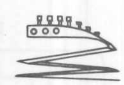


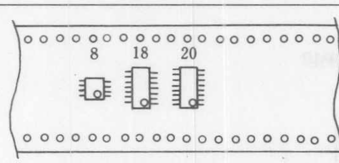
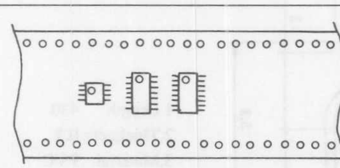
1.Length 430
2.Thickness 0.5
3.Material PVC
4.Stopper Rubber Knob
5.Contents SOP40 15pcs/tube

■ Taping Dimensions

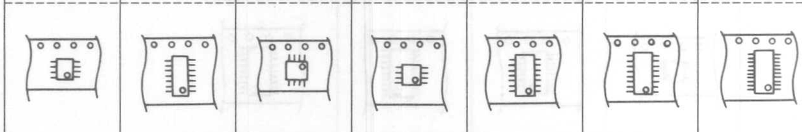
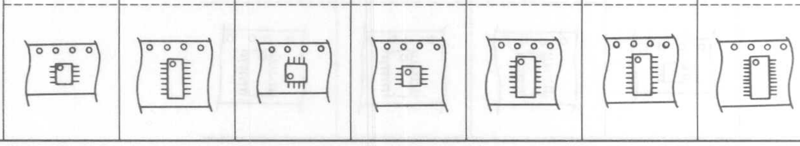
There are two types of taping packing, Adhesive Taping in accordance with EIAJ standard ET-7101 "Packaging of Electronic Components on Continuous Tapes (Adhesive Types)" and Emboss carrier taping in accordance with JIS standard C-0806 "Packaging of Electronic Components on Continuous Tapes (Surface Mounting Device)".

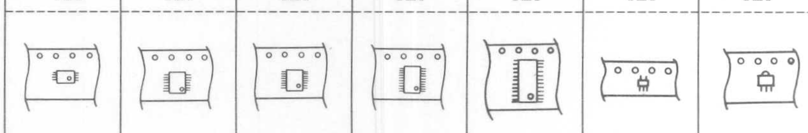
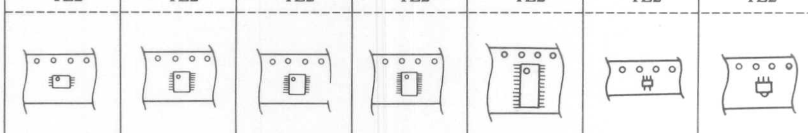
1.Adhesive Taping Table

PKG / Item		EMP		DMP					SDMP	TO-92	
		8 pin	14 pin	8 pin	14 pin	16 pin	20 pin	24 pin	30 pin	3 pin	
Reel Diameter (mm)		ϕ 300								ϕ 360	Zigzag
Tape Width (mm)		32								18	←
Pich (mm)		12								12.7	←
Contents (pcs)		2000						1500	1500	2000	2000
Pull-out Direction ⟹	T1									T1 	T3 
	T2									T2 	

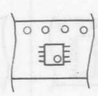
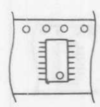
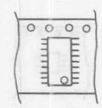
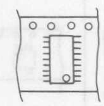
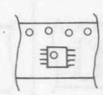
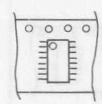
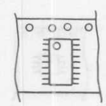
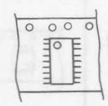
PKG / Item		SOP		
		8 pin	18 pin	20 pin
Reel Diameter (mm)		ϕ 300		
Tape Width (mm)		32		
Pitch (mm)		12		
Contents (psc)		2000		
Pull-out Direction ⟹	T1			
	T2			

2.Emboss Taping Table

PKG / Item	EMP		DMP				
	8 pin	14 pin	8 pin	8 pin	14 pin	16 pin	20 pin
Reel Diameter (mm)	ϕ 330	←	←	←	←	←	←
Tape Width (mm)	12	16	12	16	←	←	←
Pich (mm)	8	←	←	12	←	←	←
Contents (pcs)	2000	←	←	←	←	←	←
Pull-out Direction ⇨	TE1	TE1	TE3	TE1	TE1	TE1	TE1
							
	TE2	TE2	TE4	TE2	TE2	TE2	TE2
							

PKG / Item	SSOP					MTP	SOT-89
	8 pin	14 pin	16 pin	20 pin	24 pin	5 pin	3 pin
Reel Diameter (mm)	ϕ 255	←	←	←	ϕ 300	ϕ 178	←
Tape Width(mm)	12	←	←	←	16	8	12
Pitch (mm)	8	←	←	←	12	4	8
Contents (pcs)	2000	←	←	←	←	3000	1000
Pull-out Direction ⇨	TE1	TE1	TE1	TE1	TE1	TE1	TE1
							
	TE2	TE2	TE2	TE2	TE2	TE2	TE2
							

Emboss Taping Table

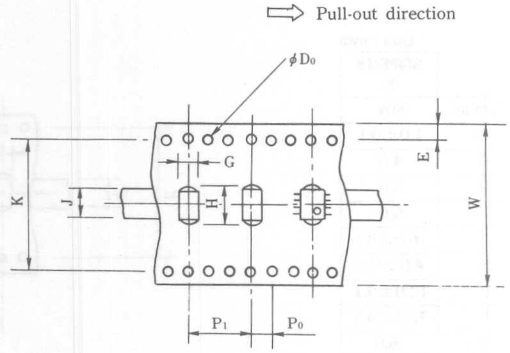
PKG / Item	SOP			
	8 pin	18 pin	22 pin	28 pin
Reel Diameter (mm)	330	←	←	←
Tape Width (mm)	12	24	←	←
Pich (mm)	8	12	←	←
Contents (pcs)	3000	2000	←	←
	TE1	TE1	TE1	TE1
Pull-out Direction ⇨				
	TE2	TE2	TE2	TE2
				

3.Adhesive Taping Dimensions

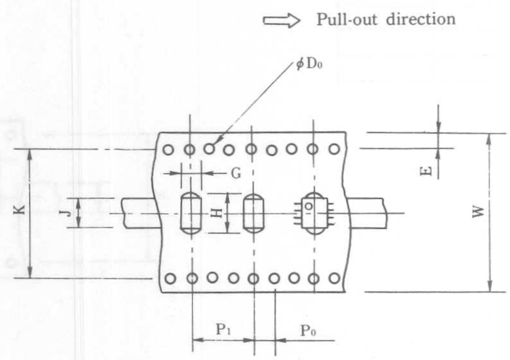
(1) Adhesive Taping Dimensions for DMP/EMP

Unit : mm

Symbol	DMP8/14/16/20/24 SDMP30,EMP8/14 Size
D_0	$1.0^{+0.1}_{0}$
E	3.0±0.1
G	4.0
H	8.0
J	6.0
K	26.0±0.1
P_0	4.0±0.1
P_1	12.0±0.1
W	32.0±0.3



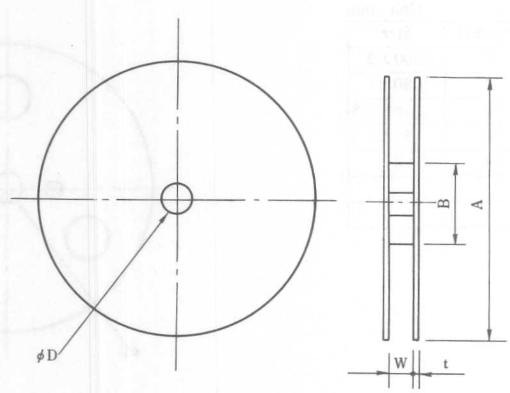
T1



T2

Unit : mm

Symbol	Size
A	ϕ300±2
B	ϕ80±1
D	ϕ16±0.8
W	34±1
t	2

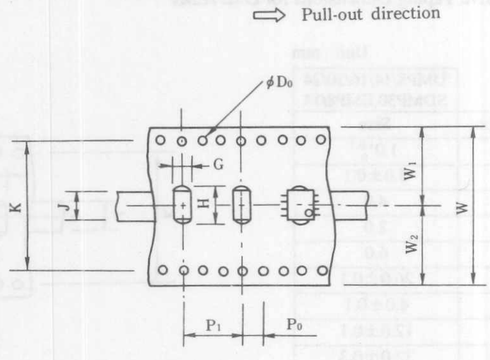


Pull-out beginning : Empty part 80～100cm+Adhesive Tape 20cm
Pull-out end: Empty part 80～100cm

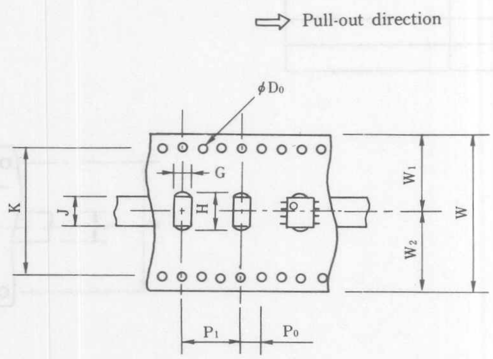
(2) Adhesive Taping Dimensions for SOP

Unit : mm

Symbol	SOP8/18 20 Size
D_0	1.0±0.1
G	4.0
H	8.0
J	6.0
K	26.0±0.1
P_0	4.0±0.1
P_1	12.0±0.1
W	32.0±0.3
W_1	16.0
W_2	16.0



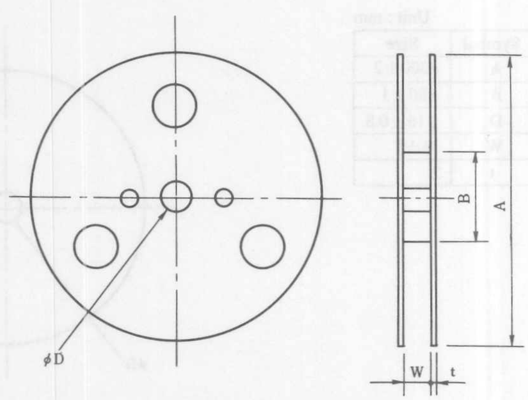
T1



T2

Unit : mm

Symbol	Size
A	ϕ 300±2
B	ϕ 80±1
D	ϕ 16±0.5
W	34±1
t	2

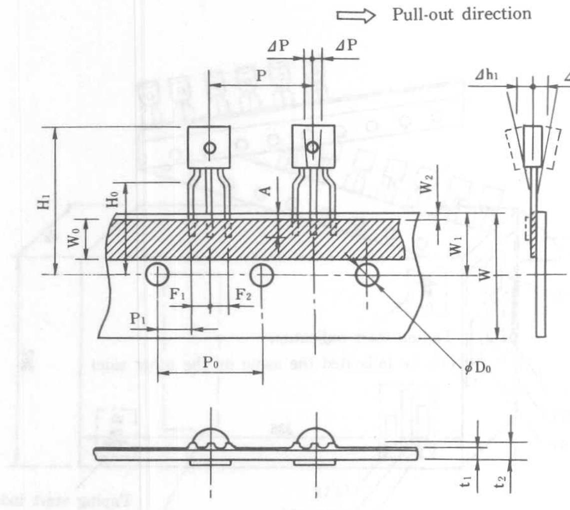


Pull-out beginning : Empty part more than 90cm+Adhesive Tape 20cm
Pull-out end: Empty part more than 80cm

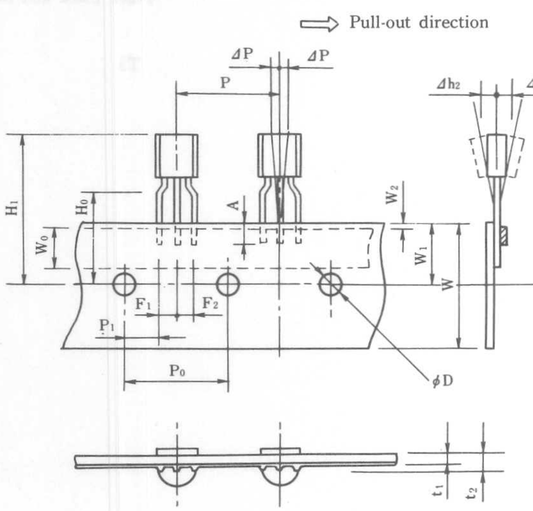
(3) Adhesive Taping Dimensions for TO-92

Unit : mm

Symbol	Size
P	12.7±0.1
P_0	12.7±0.3
P_1	3.85±0.7
F_1, F_2	$2.5^{+0.4}_{-0.1}$
W	$18.0^{+1.0}_{-0.5}$
W_0	6.0
W_1	9.5±0.5
W_2	0.5
H_0	16.0±0.5
H_1	24.7MAX
ϕD_0	ϕ4.0±0.2
$\triangle h_1$, $\triangle h_2$	2.0MAX
$\triangle P$	1.0
t_1	0.6±0.3
t_2	1.5MAX
A	2.5



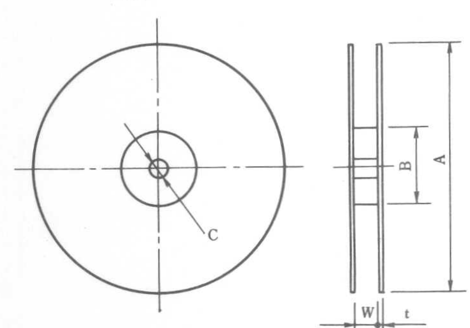
T1



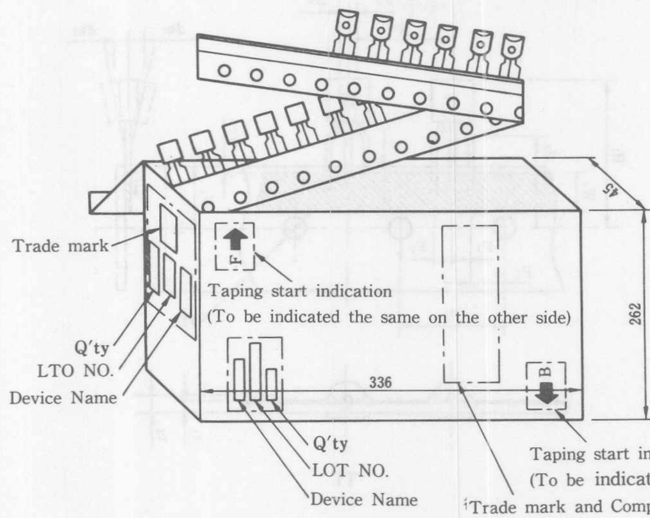
T2

Unit : mm

Symbol	Size
A	ϕ 360
B	ϕ 89
D	ϕ 30
W	43.0
t	3.0



Pull-out beginning : Empty part more than 5 devices+Layer paper more than 1000mm
Pull-out end: Empty part more than 5 devices+layer paper more than 1000mm



Zigzag type
(25 devices winding)
Tape size is the same as T1/T2 type

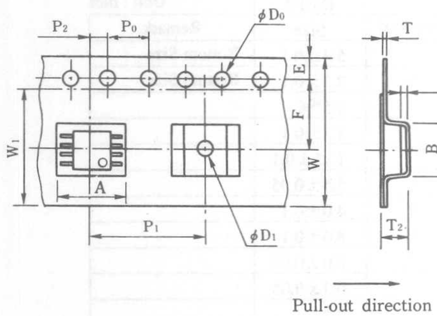
T3

4.Emboss Carrier Taping Dimensions

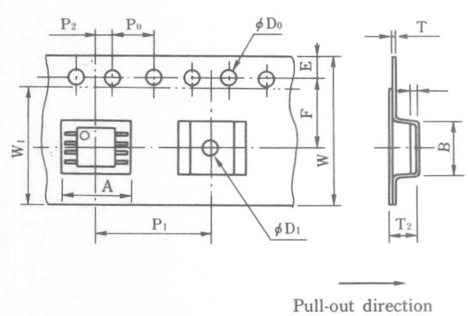
(1) Emboss Carrier Taping Dimensions for DMP8

Unit : mm

Symbol	DMP8 Size	Remark
A	7.1±0.1	Bottom Size
B	5.4±0.1	Bottom Size
D_0	1.55±0.05	
D_1	2.05±0.1	
E	1.75±0.1	
F	7.5±0.1	
P_0	4.0±0.1	
P_1	12.0±0.1	
P_2	2.0±0.1	
T	0.3±0.05	
T_2	2.3	
W	16.0±0.3	
W_1	13.5	Thickness 0.1MAX



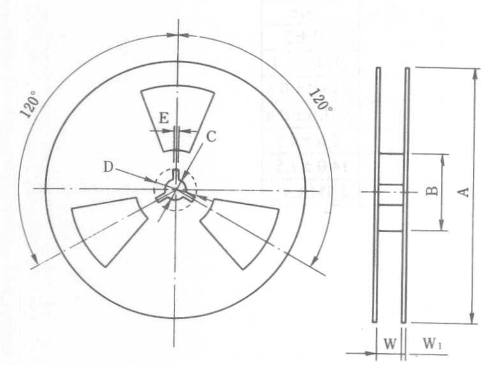
TE1



TE2

Unit : mm

Symbol	Size
A	ϕ 330±2
B	ϕ 80±1
C	ϕ 13±0.5
D	ϕ 21±0.8
E	2±0.5
W	$17.5^{+2.0}_{0}$
W_1	2.5MAX

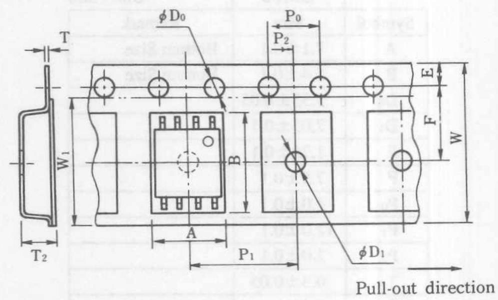


Pull-out beginning : Empty part more than 20 embosses+Cover tape more than one around reel
Pull-out end: Empty part more than 20 embosses

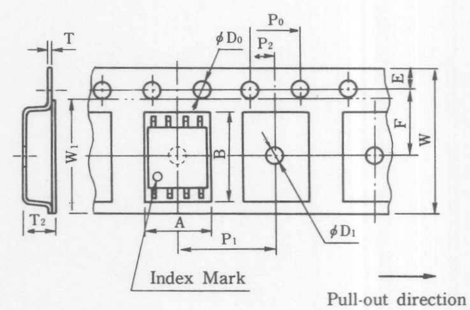
Emboss Carrier Taping Dimensions for DMP8

Unit : mm

Symbol	DMP8 Size	Remark
A	5.4±0.1	Bottom Size
B	7.3±0.1	Bottom Size
D_0	$1.5^{+0.1}_{-0}$	
D_1	1.7±0.1	
E	1.75±0.1	
F	5.5±0.05	
P_0	4.0±0.1	
P_1	8.0±0.1	
P_2	2.0±0.05	
T	0.3±0.05	
T_2	2.4	
W	12.0±0.3	
W_1	9.5	Thickness 0.1MAX



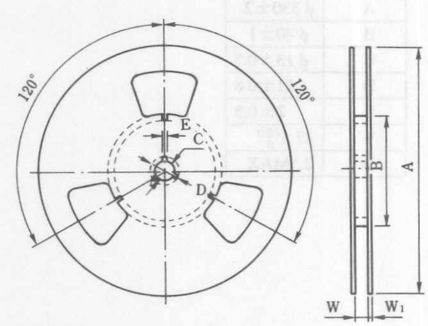
TE3



TE4

Unit : mm

Symbol	Size
A	φ 330±2
B	φ 80.0±1
C	φ 13.0±0.5
D	φ 21.0±0.8
E	2.0±0.5
W	14.0±1.5
W_1	2.5MAX

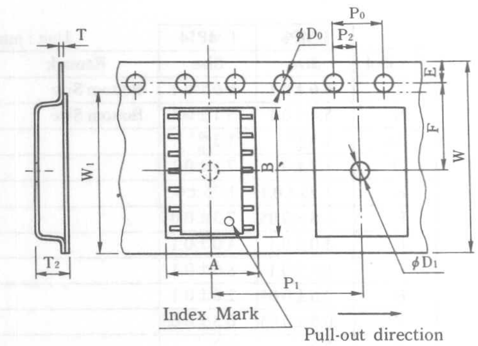


Pull-out beginning : Empty part more than 20 embosses+Cover tape more than one around reel
Pull-out end: Empty part more than 20 embosses

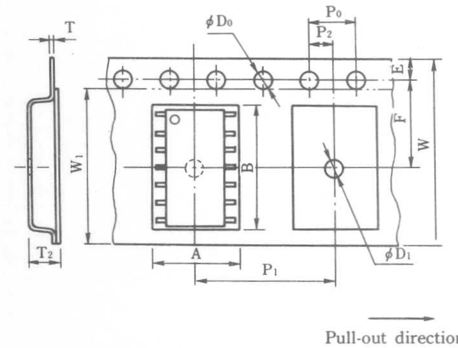
(2) Emboss Carrier Taping Dimensions for DMP14/16/20

Unit : mm

Symbol	DMP14/16/20 Size	Remark
A	7.4±0.1	Bottom Size
B	10.4±0.1	Bottom Size
D_0	$1.5^{+0.1}_{-0}$	
D_1	1.7±0.1	
E	1.75±0.1	
F	7.5±0.1	
P_0	4.0±0.1	
P_1	12.0±0.1	
P_2	2.0±0.1	
T	0.3±0.05	
T_1	—	
T_2	2.3	
W	16.0±0.3	
W_1	13.5	Thickness 0.1MAX



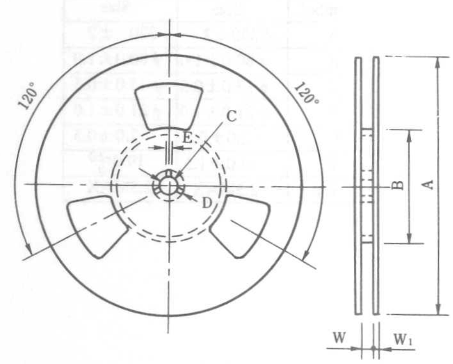
TE1



TE2

Unit : mm

Symbol	Size
A	ϕ 330±2
B	ϕ 80±1
C	ϕ 13.0±0.5
D	ϕ 21.0±0.8
E	2.0±0.5
W	$19.0^{+2.0}_{-0}$
W_1	2.5MAX

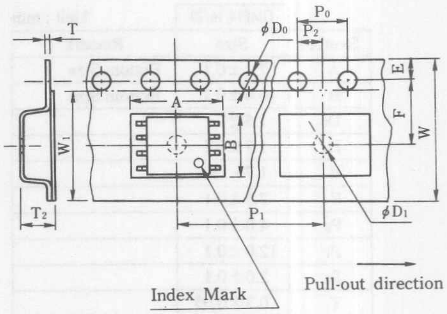


Pull-out beginning : Empty part more than 20 embosses+Cover tape more than one around reel
Pull-out end: Empty part more than 20 embosses

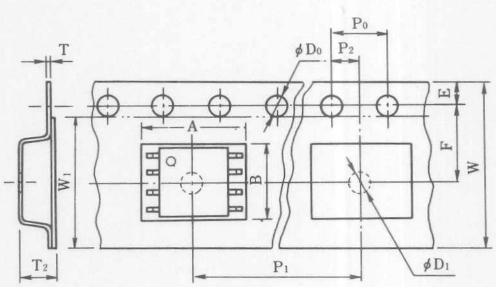
(3) Emboss Carrier Taping Dimensions for EMP8/14

Unit : mm

	EMP8	EMP14	
Symbol	Size	Size	Remark
A	6.6±0.1	6.6±0.1	Bottom Size
B	5.4±0.1	9.1±0.1	Bottom Size
D_0	$1.5^{+0.1}_{-0}$	$1.5^{+0.1}_{-0}$	
D_1	1.7±0.1	7.1±0.1	
E	1.75±0.1	1.75±0.1	
F	5.5±0.05	7.5±0.05	
P_0	4.0±0.1	4.0±0.1	
P_1	8.0±0.1	8.0±0.1	
P_2	2.0±0.05	2.0±0.1	
T	0.3±0.05	0.3±0.05	
T_2	2.2	2.2	
W	12.0±0.3	16.0±0.3	
W_1	9.5	13.5	Thickness 0.1MAX



TE1

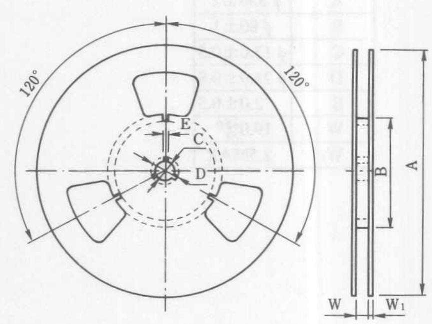


TE2

Pull-out direction

Unit:mm

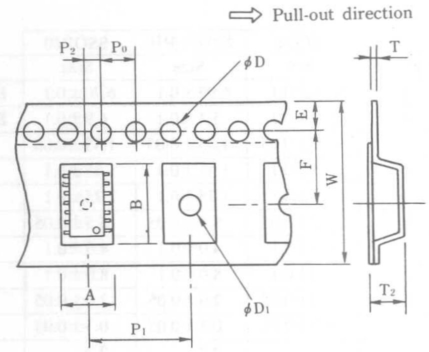
	EMP8	EMP14
Symbol	Size	Size
A	ϕ330±2	ϕ330 ±2
B	ϕ80.0±1.0	ϕ80.0±1.0
C	ϕ13.0±0.5	ϕ13.0±0.5
D	ϕ21.0±1.0	ϕ21.0±1.0
E	2.0±0.5	2.0±0.5
W	14.0±1.5	$19.0^{+2.0}_{-0}$
W_1	2.5MAX	2.5MAX



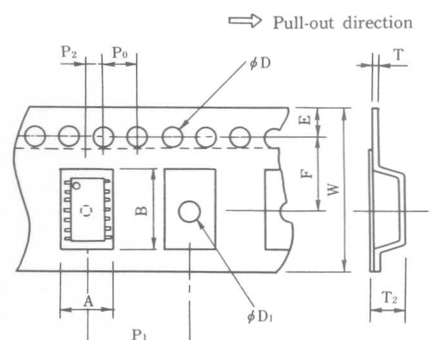
Pull-out beginning : Empty part more than 20 embosses+Cover tape more than one around reel
Pull-out end: Empty part more than 20 embosses

(4) Emboss Carrier Taping Dimensions for SOP8/18/22/28

	SOP8	SOP18	SOP22	SOP28	Unit : mm
Symbol	Size	Size	Size	Size	Remark
A	6.7	8.4	8.4	10.8	
B	5.5	12.0	14.5	19.2	
D	1.55	1.55	1.55	1.55	
D_1	2.0	2.05	2.05	2.05	
E	1.75	1.75	1.75	1.75	
F	5.5	11.5	11.5	11.5	
P_0	4.0	4.0	4.0	4.0	
P_1	8.0	12.0	12.0	12.0	
P_2	2.0	2.0	2.0	2.0	
T	0.3	0.3	0.3	0.3	
T_2	2.51	2.86	2.86	3.36	
W	12.0	24.0	24.0	24.0	



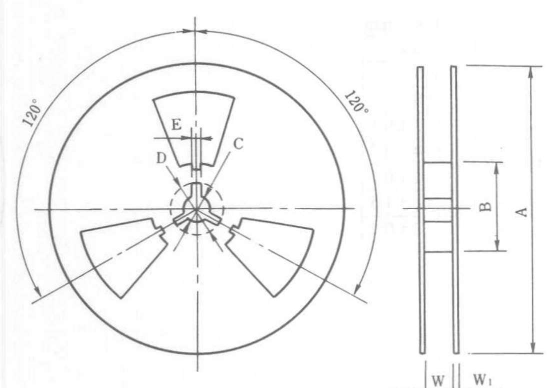
TE1



TE2

Unit : mm

	SOP8	SOP18/22/28
Symbol	Size	Size
A	ϕ 330±2	ϕ 330±2
B	ϕ 80±1	ϕ 80±1
C	ϕ 13±0.5	ϕ 13±0.5
D	ϕ 21±0.5	ϕ 21±0.5
E	2±0.5	2±0.5
W	14±1.5	24.4±2.0
t	2±0.5	2±0.5

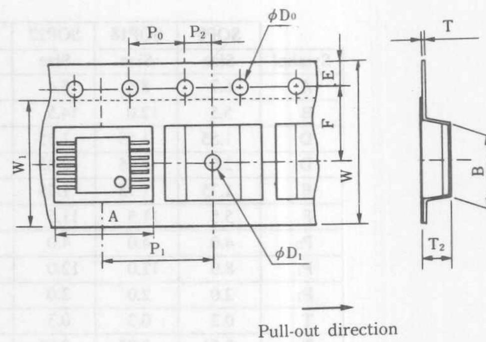


Pull-out beginning : Empty part more than 500mm+Cover tape more than 400mm
Pull-out end: Empty part more than 500mm+Cover tape more than 400mm

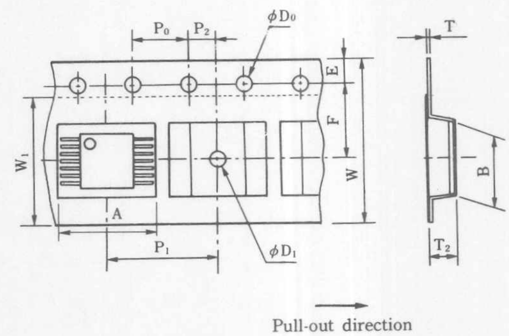
(5) Emboss Carrier Taping Dimensions for SSOP8/14/16/20

Unit : mm

	SSOP8	SSOP14/16	SSOP20	
Symbol	Size	Size	Size	Remark
A	6.70±0.1	6.95±0.1	6.70±0.1	Bottom+0.3mm
B	3.9±0.1	5.4±0.1	6.9±0.1	Bottom+0.3mm
D_0	1.55±0.05	1.55±0.05	1.55±0.05	
D_1	1.55±0.1	1.55±0.1	1.55±0.1	
E	1.75±0.1	1.75±0.1	1.75±0.1	
F	5.5±0.05	5.5±0.05	5.5±0.05	
P_0	4.0±0.1	4.0±0.1	4.0±0.1	
P_1	8.0±0.1	8.0±0.1	8.0±0.1	
P_2	2.0±0.05	2.0±0.05	2.0±0.05	
T	0.3±0.05	0.3±0.05	0.3±0.05	
T_2	2.2	2.2	2.2	
W	12.0±0.3	12.0±0.3	12.0±0.3	
W_1	9.5	9.5	9.5	Thickness 0.1 MAX



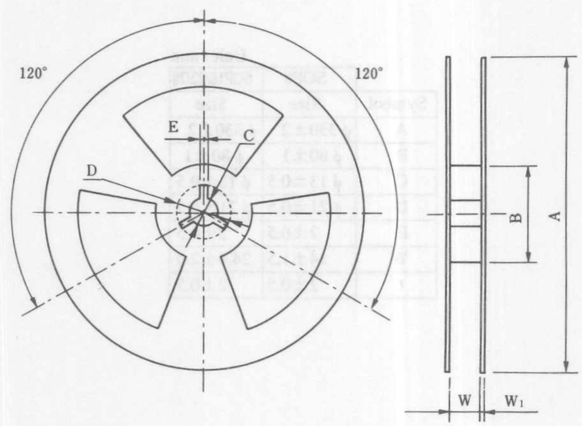
TE1



TE2

Unit : mm

Symbol	Size
A	ϕ 255±1
B	ϕ 80±1
C	ϕ 13±0.2
D	ϕ 24±0.5
E	2±0.5
W	14±1.5
W_1	2±0.2

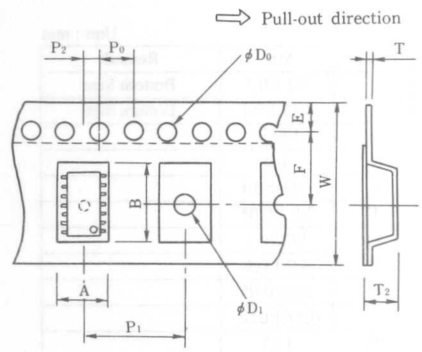


Pull-out beginning : Empty part more than 20 embosses+Cover tape more than one around reel
Pull-out end: Empty part more than 20 embosses

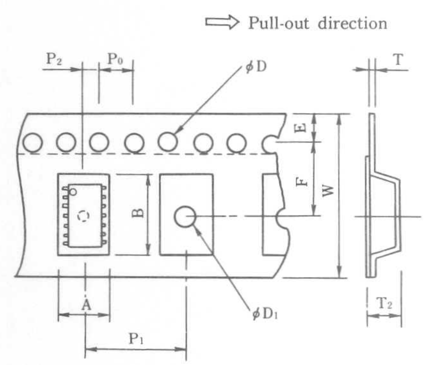
(6) Emboss Carrier Taping Dimensions for SSOP24

Unit : mm

Symbol	SSOP24 Size
A	8.3
B	10.5
D_0	1.55
D_1	2.05
E	1.75
F	7.5
P_0	4.0
P_1	12.0
P_2	2.0
T	0.3
T_2	2.86
W	16.0



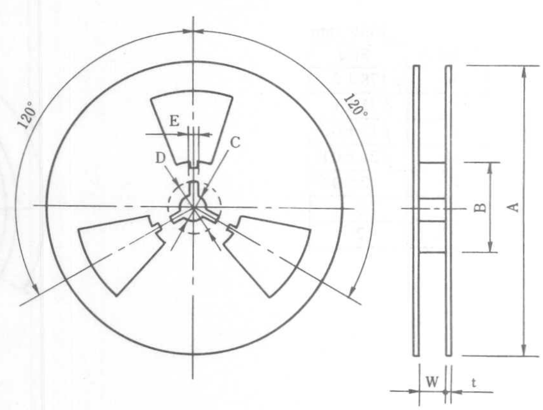
TE1



TE2

Unit : mm

Symbol	Size
A	ϕ 330±2
B	ϕ 80±1
C	ϕ 13±0.5
D	ϕ 21±0.5
E	2±0.5
W	16.4±1.5
W_1	2±0.2

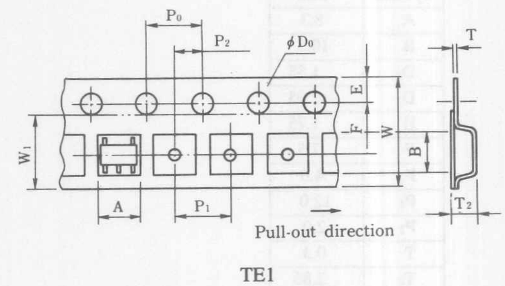


Pull-out beginning : Empty part more than 500mm+Cover tape more than 400mm
Pull-out end: Empty part more than 500mm

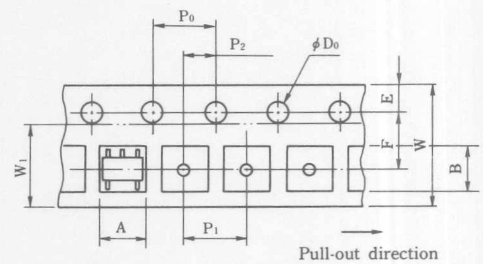
(7) Emboss Carrier Taping Dimensions for MTP5

Unit : mm

Symbol	Size	Remark
A	3.2±0.1	Bottom Size
B	3.23±0.1	Bottom Size
D_0	$1.5^{+0.1}_{-0}$	
D_1	1.0	
E	1.75±0.1	
F	3.5±0.05	
P_0	4.0±0.1	
P_1	4.0±0.1	
P_2	2.0±0.05	
T	0.27±0.05	
T_2	1.55	
W	8.0±0.3	
W_1	5.5±0.05	Thickness 0.1 MAX



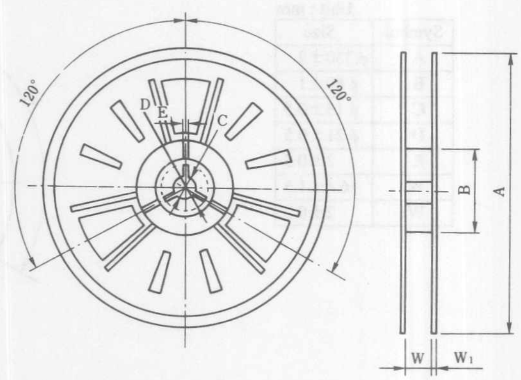
TE1



TE2

Unit : mm

Symbol	Size
A	φ178±2
B	φ75±1
C	φ13±0.5
D	φ21±0.8
E	2±0.5
W	7.5
W_1	2

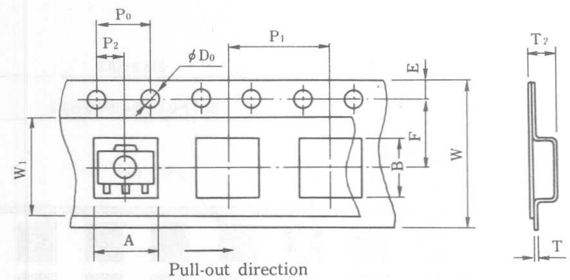


Pull-out beginning : Empty part more than 20 embosses+Cover tape more than one around reel
Pull-out end: Empty part more than 20 embosses

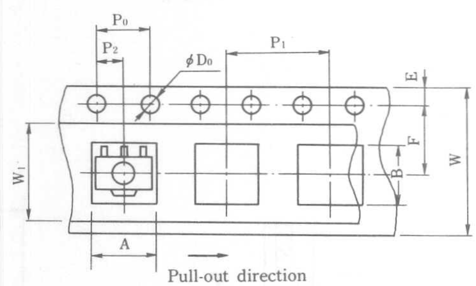
(8) Emboss Carrier Taping Dimensions for SOT89

Unit : mm

Symbol	Size	Remark
A	4.9±0.1	Bottom Size
B	4.5±0.1	Bottom Size
D_0	$1.5^{+0.1}_{-0}$	
E	1.5±0.1	
F	5.65±0.05	
P_0	4.0±0.1	
P_1	8.0±0.1	
P_2	2.0±0.05	
T	0.3±0.05	
T_2	2.0	
W	12.0±0.3	
W_1	9.5	Thickness 0.1 MAX



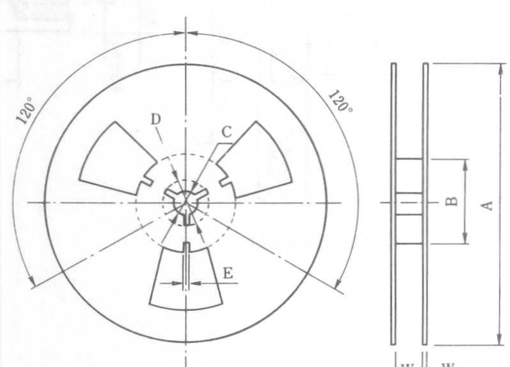
TE1



TE2

Unit : mm

Symbol	Size
A	φ 178±2
B	φ 80±1
C	φ 13±0.5
D	φ 21±0.8
E	2±0.5
W	14±1.5
W_1	$2^{+0.1}_{-0.5}$

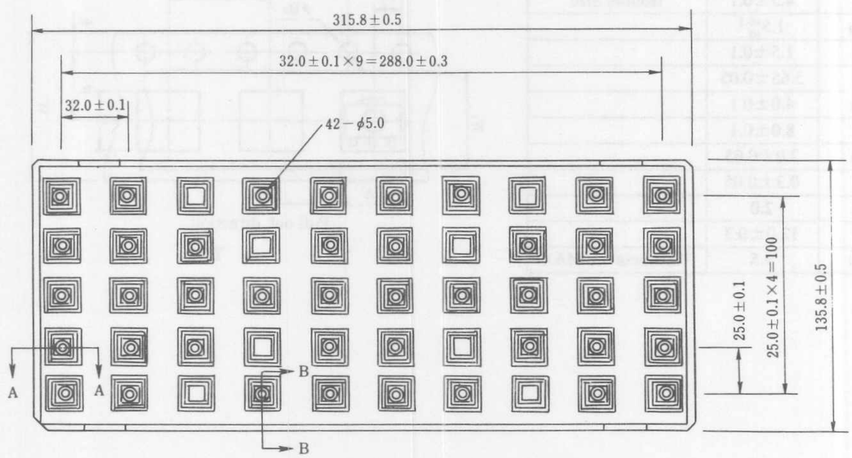


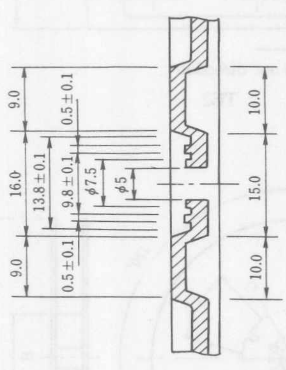
Pull-out beginning : Empty part more than 40mm+Cover tape more than 500mm
Pull-out end: Empty part more than 40mm

■ Tray Dimensions

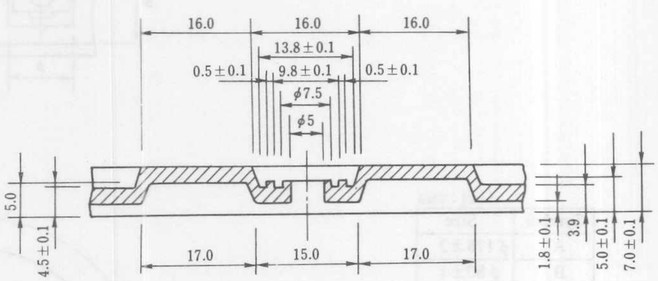
Two types of soft and hard tray are using as a QFP packing, the dimensions are shown in below.

(1) Hard Tray Dimensions for QFP44-A1,56-A1





BB Cross Section

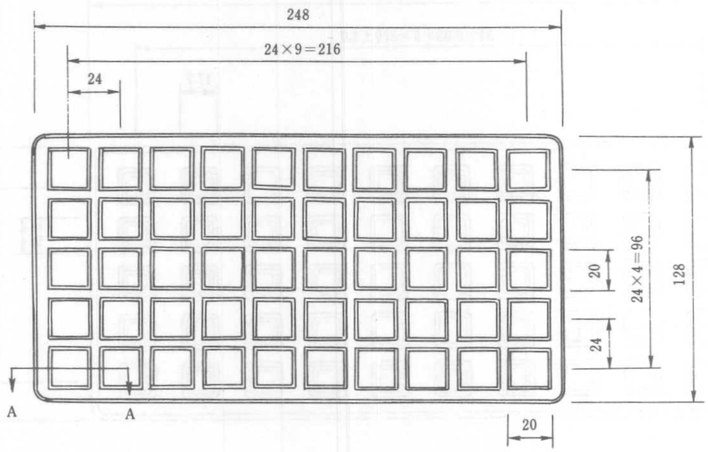


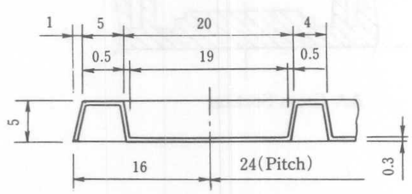
AA Cross Section

Unit: mm

Material	Polypropylene (Anti Electnstatic treatment)
Maximum Conents	50pcs

(2) Soft Tray Dimensions for QFP44-B1



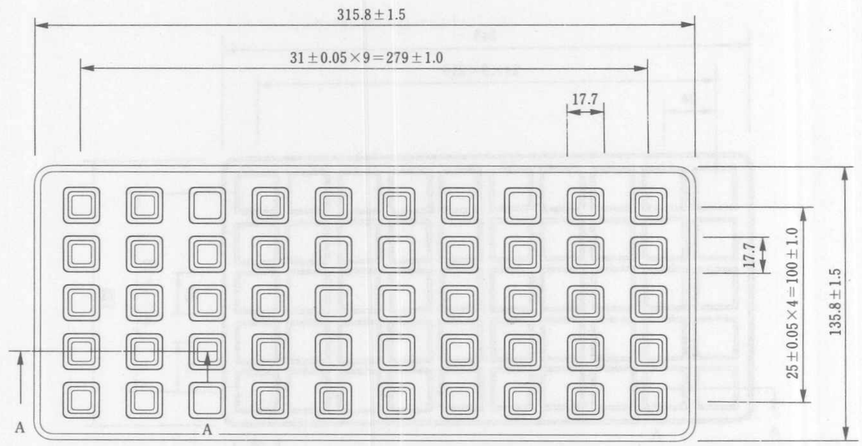


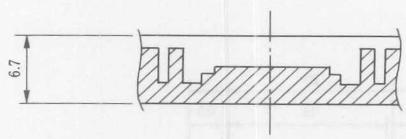
AA Cross Section

Unit:mm

Material	Conductive Vinyl Chloride Resin
Maximum Contents	50pcs

(3) Hard Tray Dimensions for QFP64-B2



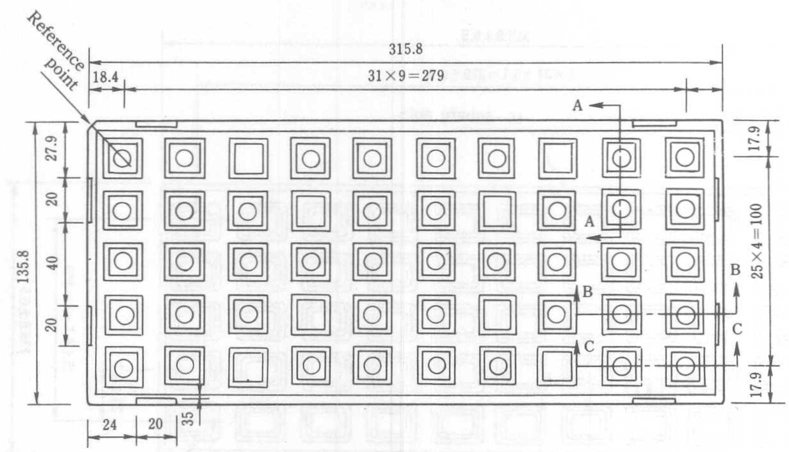


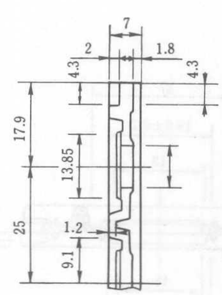
AA Cross Section

Unit:mm

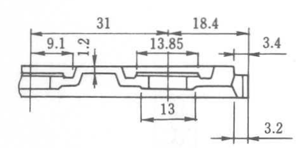
Material	Conductive Resin
Maximum Contents	50pcs

(4) Hard Tray Dimensions for QFP64-B3

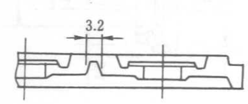




AA Cross Section



BB Cross Section

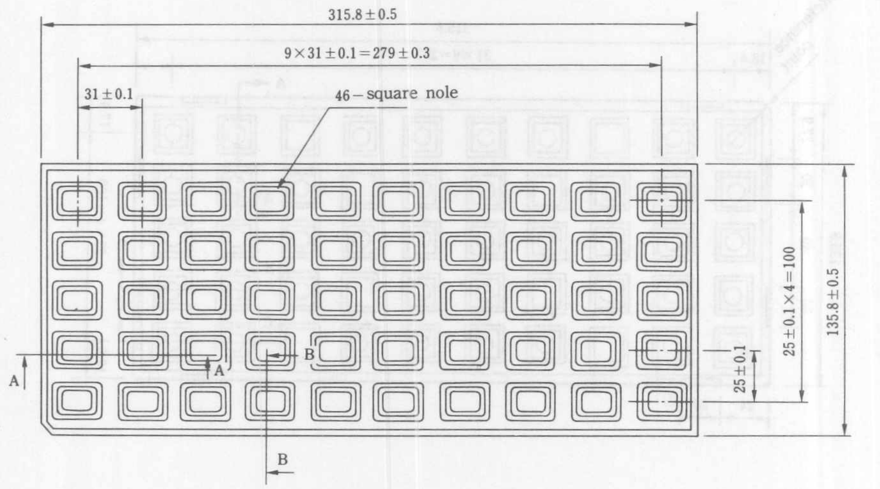


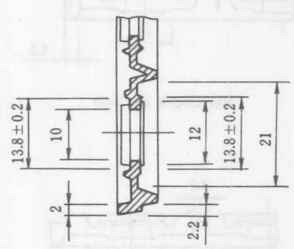
CC Cross Section

Unit:mm

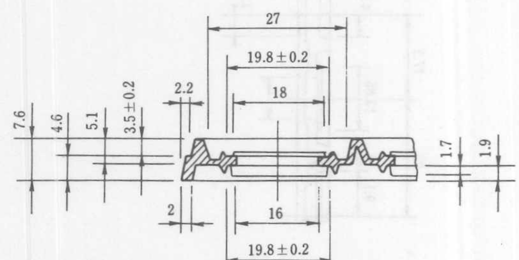
Material	Conductive Resin
Maximum Contents	50pcs

(5) Hard Tray Dimensions for QFP64-C1/C2,80-C1/C2,100-C1/C2





BB Cross Section

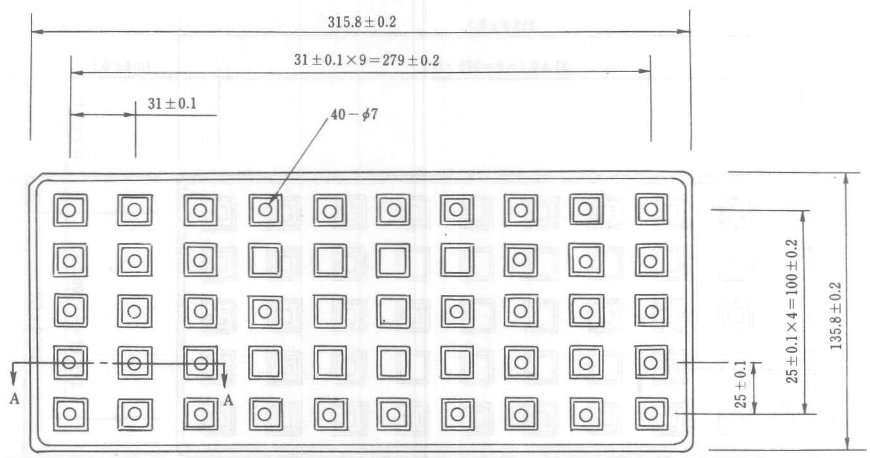


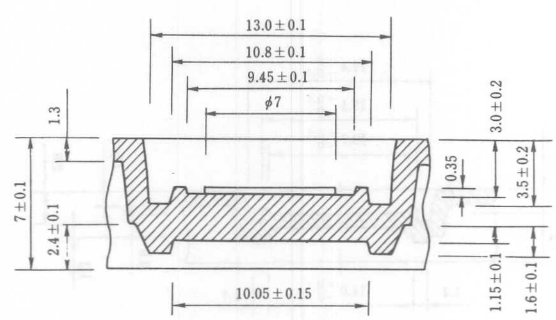
AA Cross Section

Unit:mm

Material	Polystyrene (Anti Electrostatic treatment)	
Maximum Conents		50pcs

(6) Hard Tray Dimensions for QFP64-D1



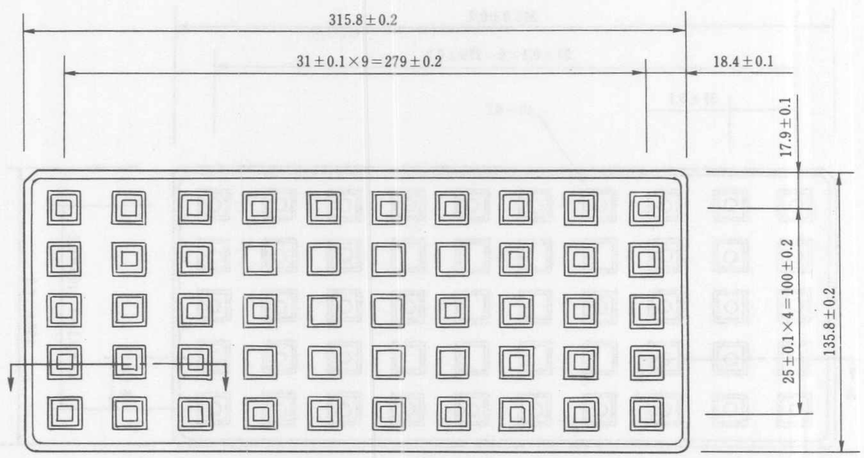


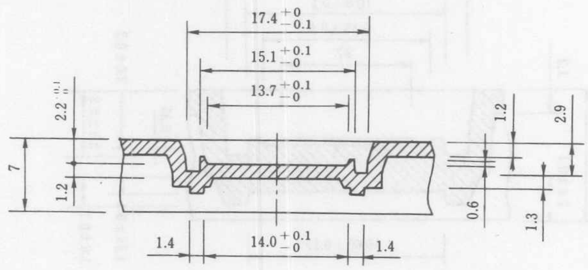
AA Cros Section

Unit:mm

Material	Polystyrene
Maximum Contents	50pcs

(7) Hard Tray Dimensions for QFP64-E1



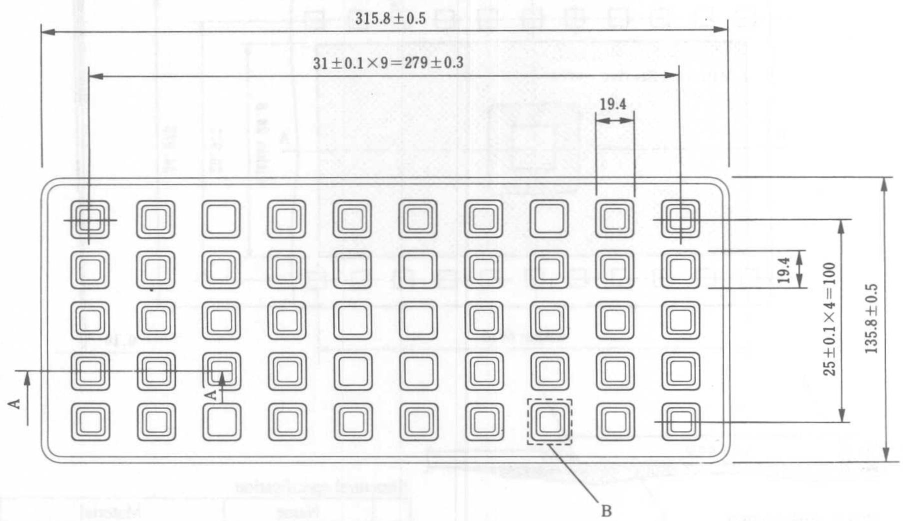


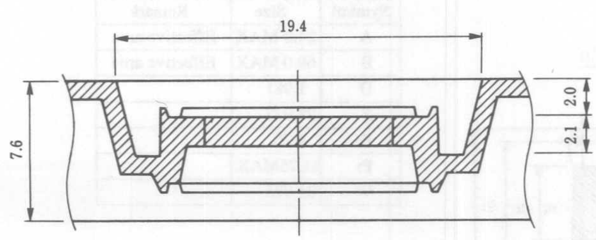
AA Cros Section

Unit:mm

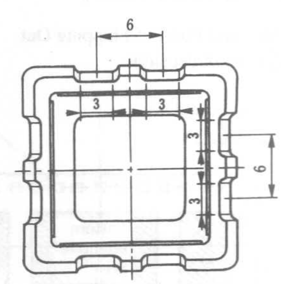
Material	Polystyrene
Maximum Contents	50pcs

(8) Hard Tray Dimensions for QFP64,80,100-G1





AA Cross Section



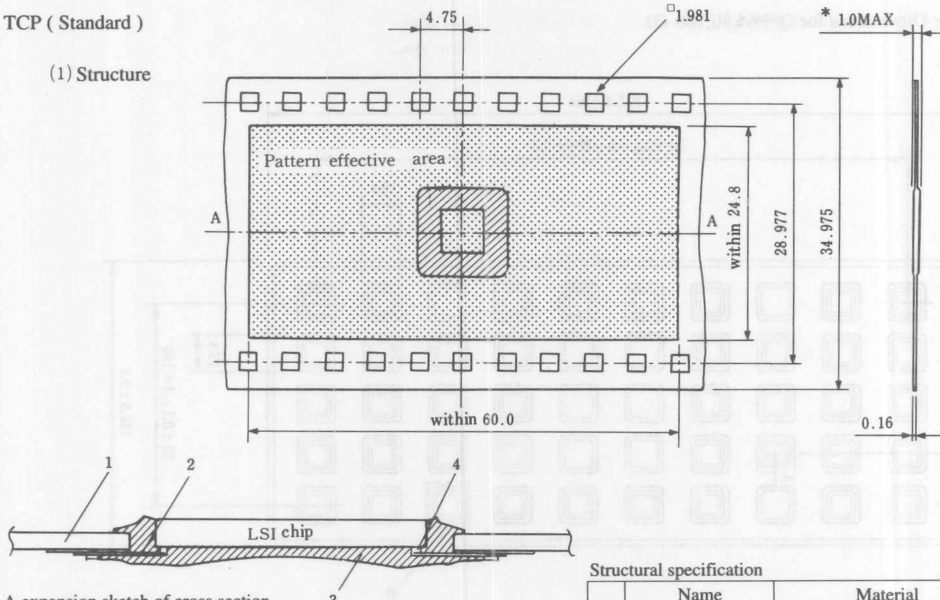
BB Cross Section

Unit:mm

Material	Polypropylene (Anti Electnstatic treatment)
Maximum Conents	50pcs

6. TCP (Standard)

(1) Structure



A-A expansion sketch of cross section

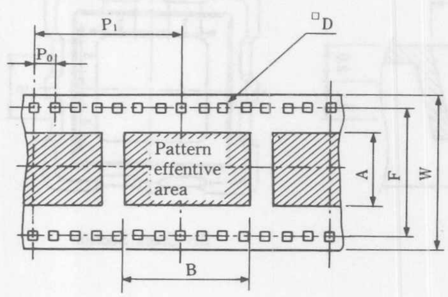
Note)
1) * Size indicates resin thickness included
2) Tape is used with 35mm width wide type
3) Tape rolling length is 20m long

Structural specification

	Name	Material
1	Basefilm	Polyimide
2	Conductive body Plating	Cu. thin film Electroless tin plating
3	Sealing Material	Epoxi type
4	Bump	Gold

(2) Standard Form of Shipping Out

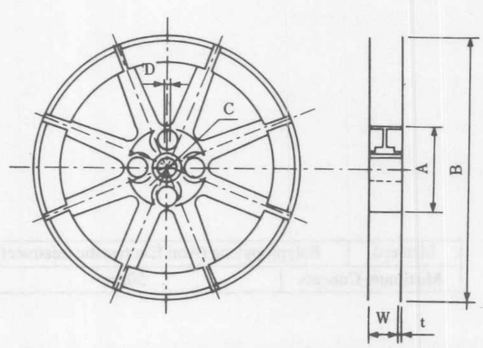
①Tape dimensions



Unit : mm

Symbol	Size	Remark
A	24.8 MAX	Effective area
B	60.0 MAX	Effective area
D	1.981	
F	28.977	
P_0	4.75	
P_1	61.75MAX	
W	34.975	

②Reel dimensions

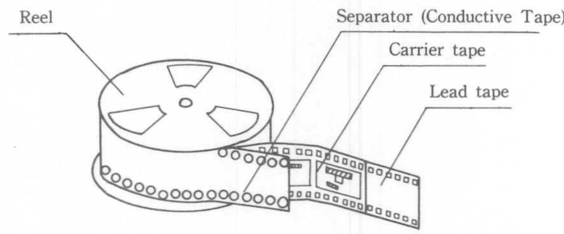


Unit : mm

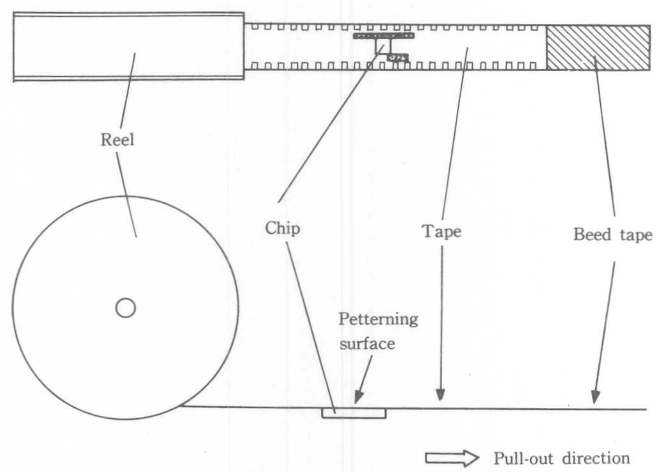
Symbol	Size
A	ϕ 330
B	ϕ 105
C	ϕ 25.9
D	4.0±0.2
W	37.0±0.5
t	2.5MAX

* Material: Styrol
(Prevention of electrification)

③Taping Specification

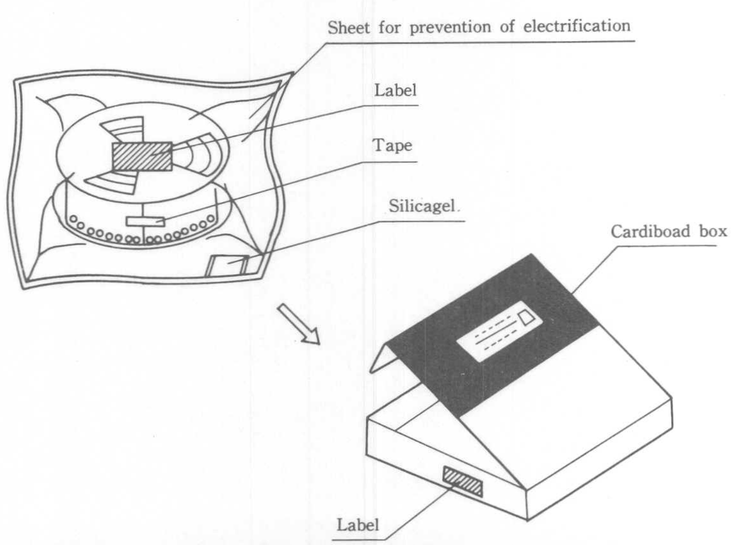


Carrier tape : 20^{+6}_{-8} m
Lead tape : 2 ± 1m
Conductive tape : 20^{+6}_{-8} m
Saparator : 20^{+6}_{-8} m



Structural specification

Name	Number of contained	Size	Material
Reel	—	ϕ 330x23^{w}	Styrol
Outer Box	1 reel	343x336x50	Cardbroad
Package bag	1 reel	440x480x0.08	Sheet for prevention of electrification



AUDIO 4

AUDIO SIGNAL ICs CROSS REFERENCE

NJRC			EQUIVALENT PRODUCTS BY OTHER COMPANIES					
FUNCTIONS		Types	N・S	MITSUBISHI	SONY	ROHM	SGS	OTHERS
POWER AMPLIFIER	Single	NJM386D	LM386N					
		NJM386L						
		NJM386M						
		NJM386BD	LM386N4					
		NJM386BL						
		NJM386BM						
		NJM2070D						
		NJM2070M						
	B.T.L.	NJM2113D						MC34119P
		NJM2113L						
		NJM2113M						MC34119M
		NJM2113E						MC34119D
		NJM2113V						
	Dual	NJM2073D					TDA2822M	
		NJM2073M						
		NJM2073S						
		NJM2076D						
		NJM2076M						
		NJM2076S						
		NJM2096D						
		NJM2096M						
		NJM2096S						
PRE AMPLIFIER		NJM387D	LM387N					
		NJM387L						
		NJM387M						
	for Head Phone Stereo	NJM2067D						
		NJM2067M				BA3404F		
PRE-POWER AMPLIFIER		NJM2128M						
STEREO MODULATOR		NJM2035D						
		NJM2035M						
SIGNAL LEVEL SENSOR		NJM2072D						
		NJM2072M						
ACTIVE BASS EXPANDER		NJM2106M						
RF AMPLIFIER FOR CD PLAYER		NJM2117V		M51593FP	CXA1571N			
DOLBY	N.R.	NJM2063AD						
		NJM2063AM						
		NJM2065AD						
		NJM2065AM						
		NJM2085M					TDA7335	
	SURROUND	NJM2177L		M69032P				
		NJM2177FB3						
		NJM2177AL						
		NJM2177AFB3						
		NJW1102L						
		NJW1102FG1						
MONORAL MIC AMPLIFIER		NJM2110M						
		NJM2110V						
		NJM2118M						
		NJM2118V						
AUDIO SWITCH		NJM2520D						
		NJM2520M						
		NJM2520V						
		NJM2520L						
		NJM2521D						
		NJM2521M						
		NJM2521V						
		NJM2521L						

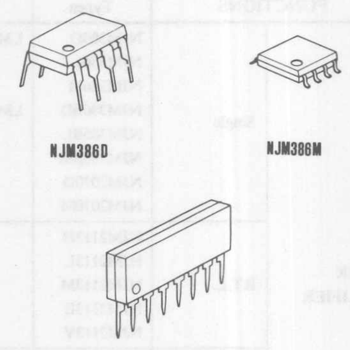
LOW VOLTAGE AUDIO POWER AMPLIFIER

■ GENERAL DESCRIPTION

The NJM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground reference while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the NJM386 ideal for battery operation.

■ PACKAGE OUTLINE



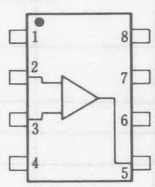
■ FEATURES

- Operating Voltage (4V~12V)
- Minimum External Components
- Low Operating Current (3mA)
- Voltage Gain (20~200)
- Single Supply Operation
- Self-centering of Output Offset Voltage
- Package Outline DIP8, SIP8, DMP8
- Bipolar Technology

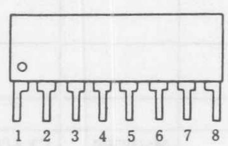
■ A PPLICATIONS

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasconic drivers
- Small servo drivers
- Power converters

■ PIN CONFIGURATION



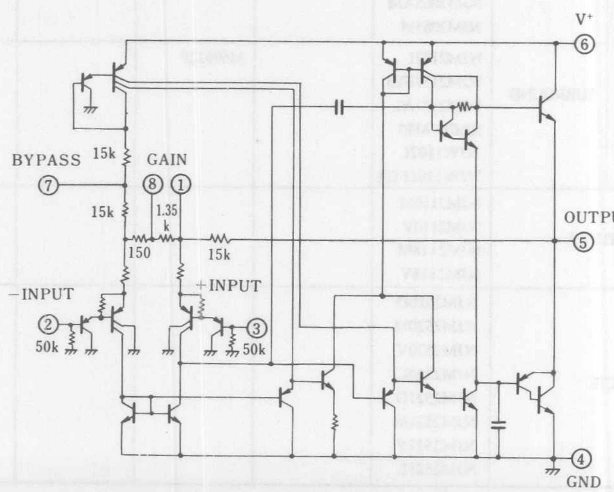
NJM386D
NJM386M



NJM386L

PIN CONNECTION
1. GAIN
2. −INPUT
3. +INPUT
4. GND
5. OUTPUT
6. V+
7. BYPASS
8. GAIN

■ EQUIVALENT CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS

(ta=25℃)

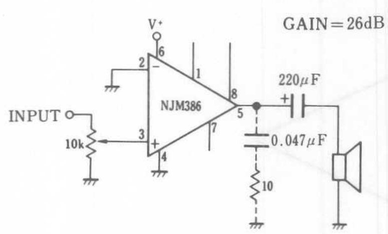
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DIP8) 700	mW
		(SIP8) 800	mW
		(DMP8) 300	mW
Input Voltage Range	V_{IN}	±0.4	V
Operating Temperature Range	T_{opr}	−20～+70	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

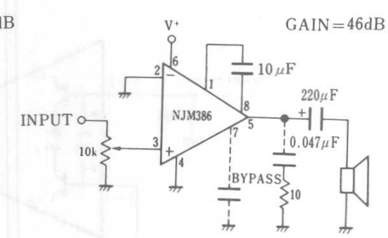
■ ELECTRICAL CHARACTERISTICS

(Ta=25℃)

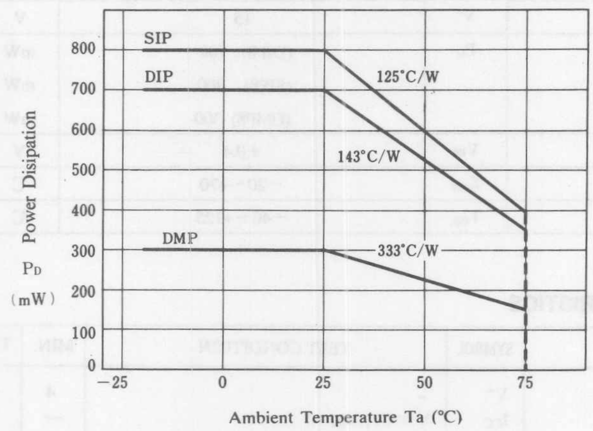
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		4	—	12	V
Operating Current	I_{CC}	V^+=6V, V_{IN}=0	—	3	8	mA
Output Power (note 2)	P_o	V^+=6V, R_L=8Ω, THD=10%	250	325	—	mW
		V^+=9V, R_L=16Ω, THD=10%	—	500	—	mW
Voltage Gain	A_V	V^+=6f, f=1kHz	24	26	28	dB
		10μF from Pin 1 to 8	43	46	49	dB
Bandwidth	BW	V^+=6V, Pins 1 and 8 Open		300	—	kHz
Total Harmonic Distortion	THD	V^+=6V, R_L=8Ω, P_{OUT}=125mW f=1kHz, Pins 1 and 8 open	—	0.2	—	%
Power Supply Rejection Ratio	SVR	V^+=6V, f=1kHz, C_{BYPASS}=10μF Pins 1 and 8 Open	—	50	—	dB
Input Resistance	R_{IN}	V^+=6V, Pins 2 and 3 Open	—	50	—	kΩ
Input Bias Current	I_B		—	250	—	nA

■ TYPICAL APPLICATION





■ POWER DISSIPATION VS. AMBIENT TEMPERATURE



■ NOTICE WHEN APPLICATION

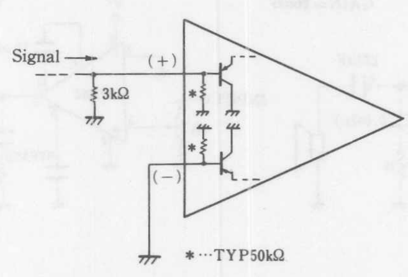
- **Prevention of Oscillation**

It is recommended to insert capacitors at around the supply source and the GND pins with the value of 0.1μF and more than 100μF which are featuring higher frequency efficiency.

When start of oscillation accordingly to the load condition, it is recommendable to insert the resistor of 10Ω and the capacitor of 0.047μF between the output and the GND pins.

- **How to use the Input Resistor** (TYP. 50kΩ)

The input resistors have much deviation in value generally, so that it is recommended not to use them as the constant of the circuit. The countermesure to be recommended si to apply the resistor of higher in value, which is so higher to be able to ignore the input deviation(3kΩ approximately) in parallel application.



- **Maintenance of Output Offset Voltage**

By making connection of both input pins with low value resistors (below 10KΩ approximately) to GND, the output offset voltage is automatically set in the medium range value of the supply source. However, the DC Gain of NJM386 is approximately at 20 times in value, so that when keeping one side input pin open, and the other side to GND on DC condition. The voltage drop caused by input resistor X input bias current, that is, (input resistor X input bias current) X 20 times voltage is to be added to the output offset voltage, and that the medium range output voltage is to be sheared, which in the result, no distortion output oscillation range shall be decreased.

In regard to dealing with the input pin, it is recommendable to put the input pin into the GND at first, and the other side of signal input pin, to be connected into GND with the resistor of less than about 10KΩ on DC condition

- **Concerning Cross-Over Distortion**

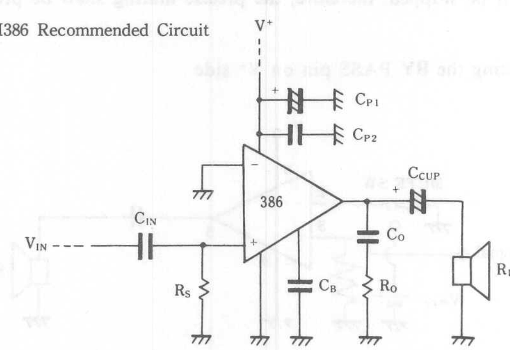
NJM386 in application, the cross-over distortion is to be generated in the high band operation.

The countermeasure for that, it is recommendable to have it replaced with NJM386B (But, be carful in prevention of oscillation). And for prevention of the cross-over distortion, it is recommendable to apply NJM2072, NJM2073.

- **The Application Purpose and Recommended Value of the External parts.**

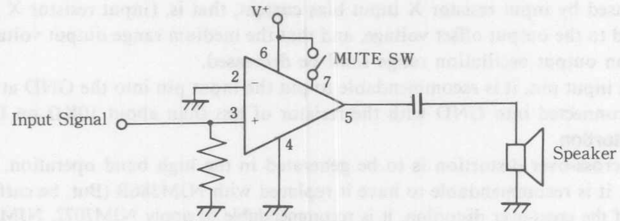
EXTERNAL PARTS	APPLICATION PURPOSE	RECOMMENDED VALUE	REMARKS
R_S	Current like nois reduction V_{OQ} stabilization	Below 10 KΩ	The noise becomes high when the input pin opend.
C_{IN}	V_{OQ} stabilization	1μF	It is not required in case when there is no DC offset in the input signal.
C_{P1}	V^+ stabilization	$\cong C_{CUP}$	It can be decreased in value when the output impedance source is low.
C_{P2}	Oscillation prevention	0.1μF	Insert near around the supply source and GND pins.
C_B	Ripple rejection to V_O by way of V^+	47μF	It is not required when the V^+ is stabilized.
C_O	Oscillation prevention	0.047μF	To be decided in value according to load condition.
R_O	Oscillation prevention	10Ω	To be decided in value according to load condition.
C_{CUP}	Output DC Decoupling	220μF when R_L =8Ω	Low band cutoff frequency(f_L) shall be decided by $C_{CUP}R_L$. When C_{CUP} is less in value, f_L is to be increased.

NJM386 Recommended Circuit



■ MUTING CIRCUIT EXAMPLE

(1) The way how to apply DC voltage to −INPUT pin.

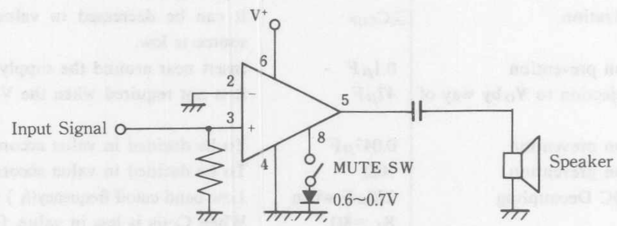


According to this method, when applicating DC voltage, Vmute to −INPUT PIN, the output voltage V_O at voltage gain A_V will be,

$V_O = V^+/2 - Vmute * A_V$

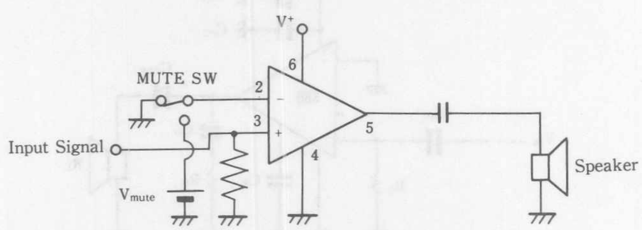
It is the way that the muting shall be proceeded by keeping V_O saturating at the GND side. Now, the output is saturated, so that there is no leakage of muting. However, when the peak value of signal input is increased higher than about the value of 1/4 Vmute, the leakage of muting shall be started.

(2) The way, how to connect gain. No. 8 PIN to GND



It is the way, originally that the pin which is to be used for adjusting the gain of NLM386, but to have it applied in connecting to GND side, and by doing so, to stop the earely stage motion, but keeping on for muting operation. The earely stage motion shall be stopped, therefore, the precise muting shall be proceeded with less leakage on operation.

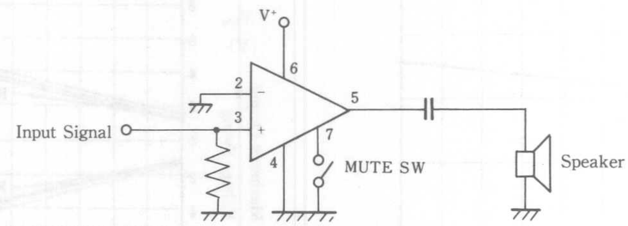
(3) The way how to proceed casting the BY PASS pin on V^+ side



By this way, the bias circuit within IC, to be stopped and then, further for stopping motion of driver level, and at the output level. However, the input level alone is operating, so that a slight leakage of signal to the output pin through inside resistor to be occured. The leakage level is to be inverse proportion to load, therefore, it is necessary to check accordingly through the load condition.

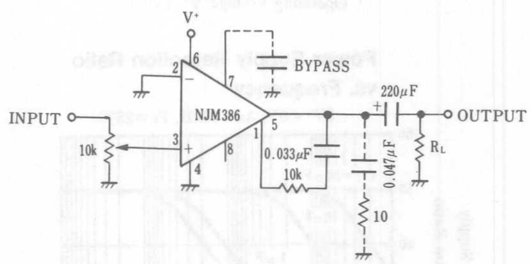
(Note) Improper Muting Circuit
Never to apply with the Muting Circuit, because of the fact that, there are cases when the muting does not operate depending on IC to be used.

The way how to connect the BY PASS PIN to GND.

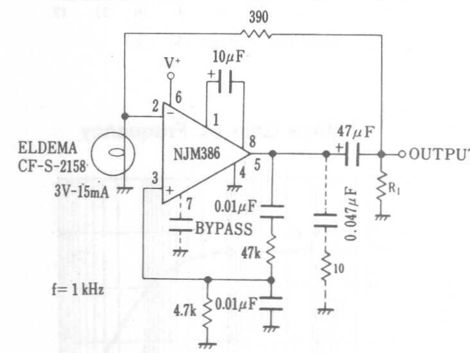


■ APPLICATION CIRCUIT EXAMPLE

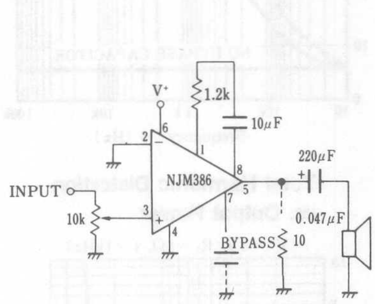
Amplifier 1



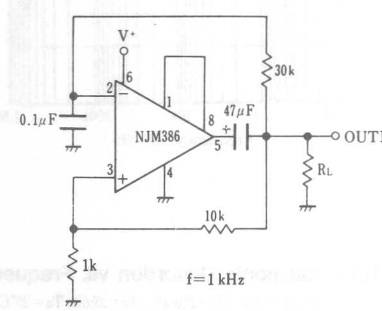
Low Distortion Power Wienbridge Oscillator



Amplifier 2



Square Wave Oscillator



■ WIDE RANGE APPLICATION

NJM386 is a small output power amplifier with minimum external parts, and also the gain of which is fixed, yet it can be made changeable in value, too.

GAIN CONTROL

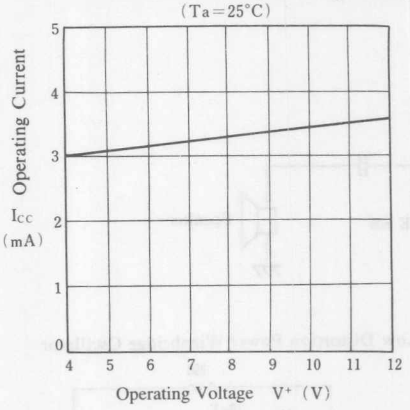
To make the NJM386 a more versatile amplifier, two pins (1 and 8) are provieded the gain contorol. With pins 1 and 8 open the 1.35kΩ resistor sets the gain at 20 (26dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35kΩresistor, the gain will go up to 200 (46dB). If a resistor is placed in series with the capacitor. the gain can be set to any value from 20 to 200. Gain contorol can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual appapplications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15kΩ resistor). For 6dB effective bass boost: R $\cong$ 15kΩ, the lowest value for good stable operation is R_{MIN}=10kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2kΩ can be used. This restriciton is because the amplifier is only compensated for closed-loop gains greater than 9.

■ TYPICAL CHARACTERISTICS

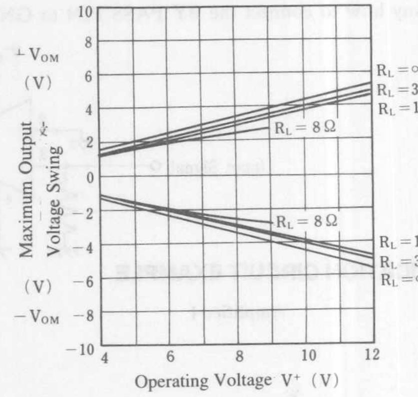
Operating Current vs. Operating Voltage

(Ta=25°C)



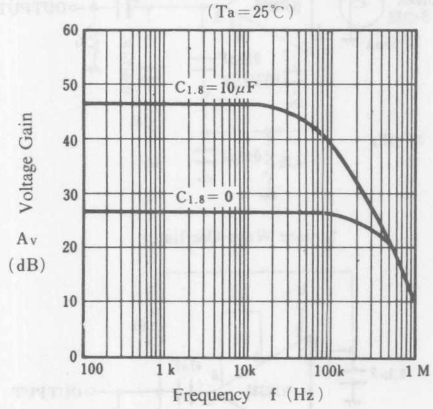
Maximum Output Voltage Swing vs. Operating Voltage

(Standard Application, Ta=25°C)



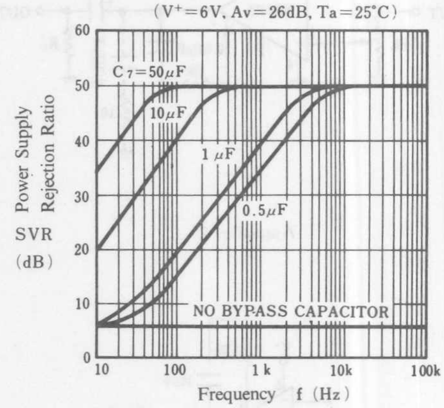
Voltage Gain vs. Frequency

(Ta=25°C)



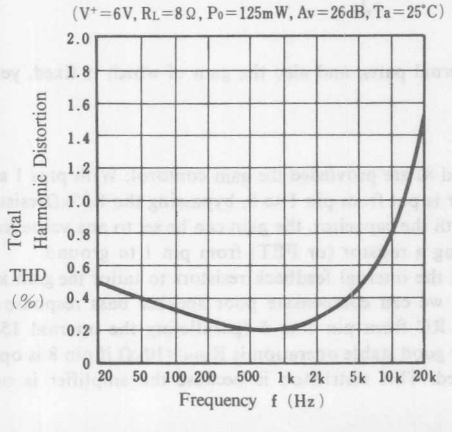
Power Supply Rejection Ratio vs. Frequency

(V+=6V, Av=26dB, Ta=25°C)



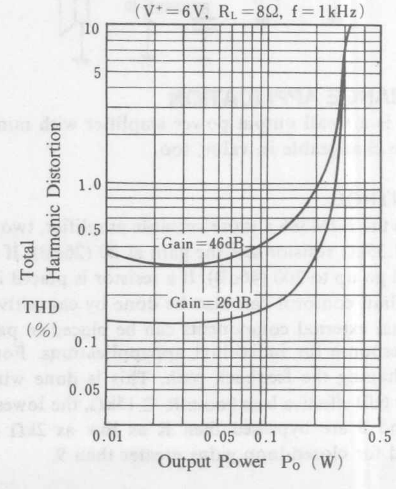
Total Harmonic Distortion vs. Frequency

(V+=6V, RL=8Ω, Po=125mW, Av=26dB, Ta=25°C)



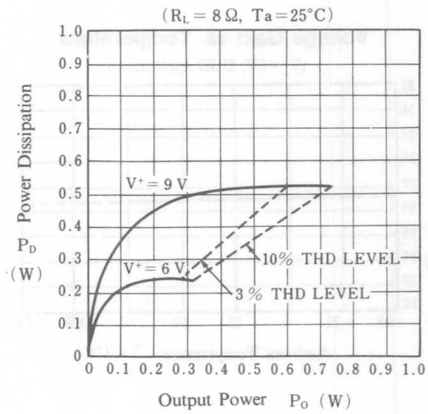
Total Harmonic Distortion vs. Output Power

(V+=6V, RL=8Ω, f=1kHz)

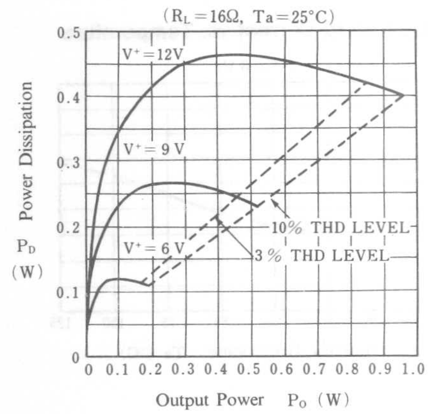


■ TYPICAL CHARACTERISTICS

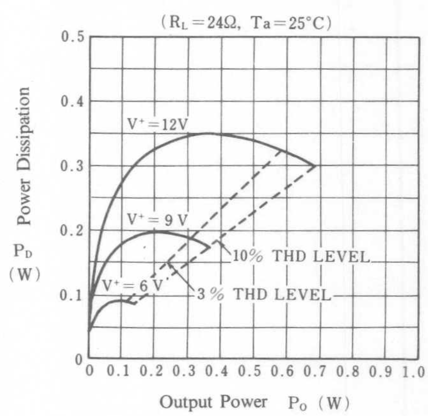
Power Dissipation vs. Output Power



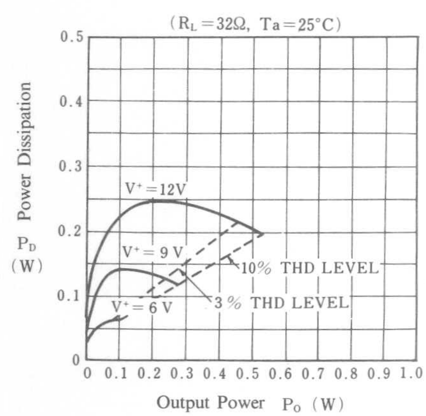
Power Dissipation vs. Output Power



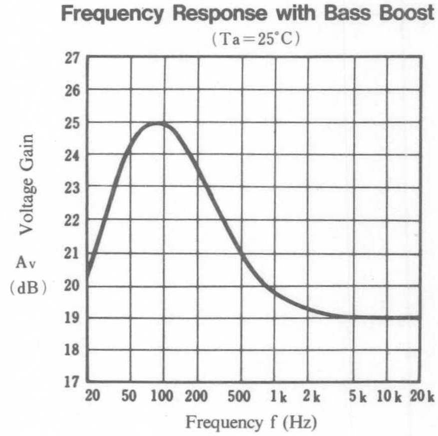
Power Dissipation vs. Output Power



Power Dissipation vs. Output Power

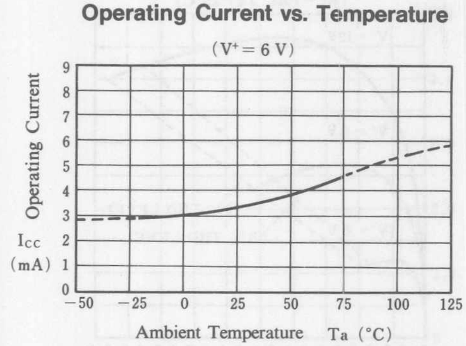


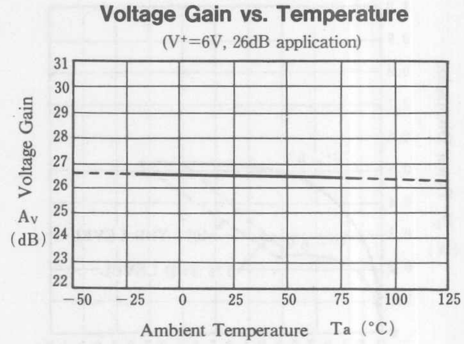
Frequency Response with Bass Boost



(Typical Application "Amplifier 1")

■ TYPICAL CHARACTERISTICS



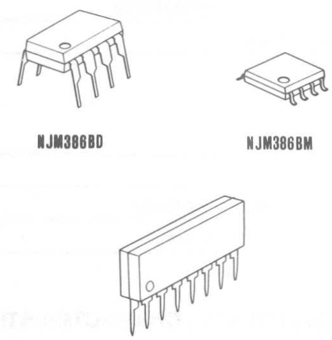


LOW VOLTAGE AUDIO POWER AMPLIFIER

■ GENERAL DESCRIPTION

The NJM386B is wider operating voltage and higher output power version of NJM386. The maximum operating voltage is 18V, and the maximum output power is up to 1W.

■ PACKAGE OUTLINE



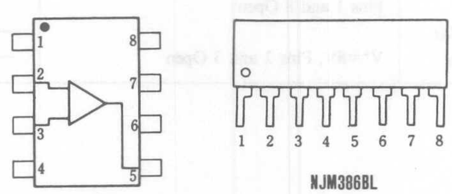
■ FEATURES

- Operating Voltage (4V～18V)
- Minimum External Components
- Low Operating Current (5mA)
- Voltage Gain (20～200)
- Single Supply Operation
- Self-centering of Output Offset Voltage
- Package Outline DIP8, SIP8, DMP8
- Bipolar Technology

■ APPLICATIONS

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultra-sonic Drivers
- Small servo drivers
- Power converters

■ PIN CONFIGURATION

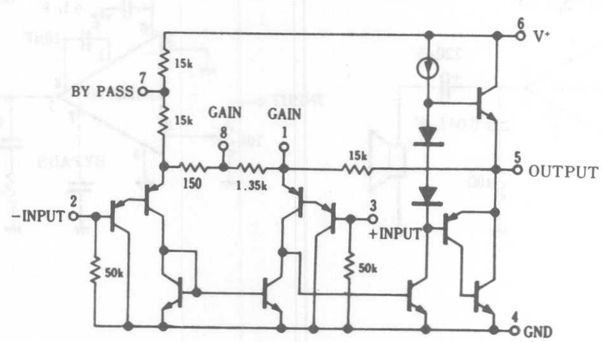


NJM386BD
NJM386BM

NJM386BL

PIN FUNCTION
1. GAIN
2. −INPUT
3. +INPUT
4. GND
5. OUTPUT
6. V⁺
7. BY PASS
8. GAIN

■ EQUIVALENT CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	22	V
Power Dissipation	P_D	(DIP-8) 700	mW
		(SIP-8) 800	mW
		(DMP-8) 300	mW
Input Voltage Range	V_{IN}	±0.4	V
Operating Temperature Range	T_{opr}	−20~+70	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

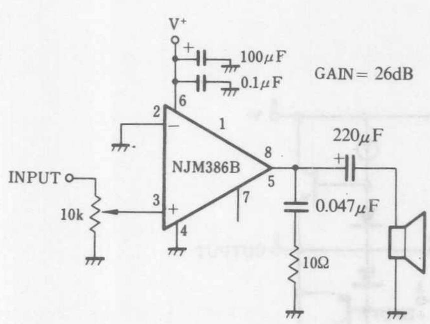
■ ELECTRICAL CHARACTERISTICS

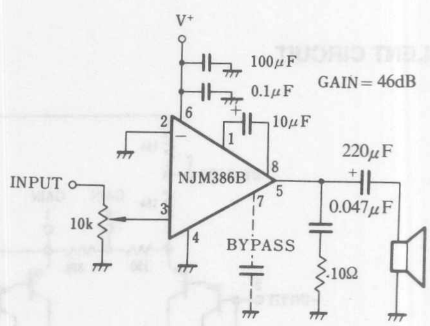
(Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		4		18	V
Operating Current	I_{CC}	V^+=6V, V_{IN}=0	—	5	8	mA
Output Power	P_O	V^+=6V, R_L=8Ω, THD=10%	250	325	—	mW
		V^+=9V, R_L=8Ω, THD=10% (note 2)	500	850	—	mW
		V^+=16V, R_L=32Ω, THD=10% (note 1)	700	1000	—	mW
Voltage Gain	A_V	Vs=6V, f=1kHz	24	26	28	dB
		10μF from Pin 1 to 8	43	46	49	dB
Bandwidth	BW	V^+=6V, Pins 1 and 8 Open		600	—	kHz
Total Harmonic Distortion	THD	V^+=6V, R_L=8Ω, P_{OUT}=125mV f=1kHz, Pins 1 and 8 Open	—	0.1	—	%
Power supply Rejection Ratio	SVR	V^+=6V, f=1kHz, C_{BYPASS}=10μF Pins 1 and 8 Open	—	50	—	dB
Input Resistance	R_{IN}		—	50	—	kΩ
Input Bias Current	I_B	V^+=6V, Pins 2 and 3 Open	—	100	—	nA

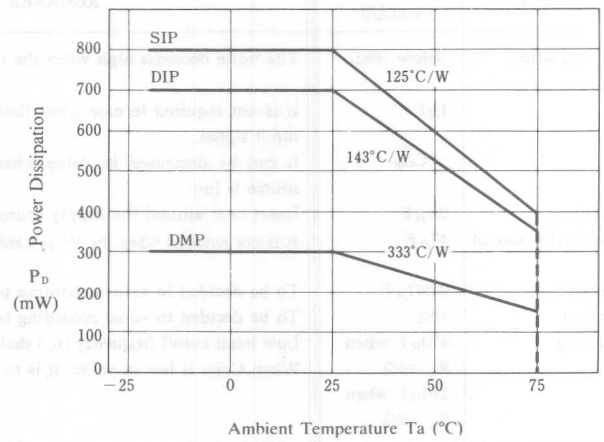
(note 1) NJM386BM: At on Board
(note 2) NJM386BS: At on Board

■ TYPICAL APPLICATION





■ POWER DISSIPATION VS. AMBIENT TEMPERATURE



■ NOTICE WHEN APPLICATION

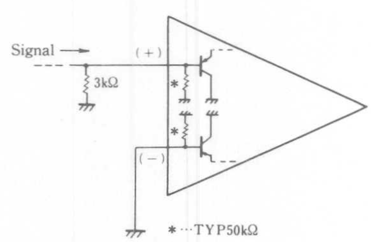
- **Prevention of Oscillation**

It is recommended to insert capacitors at around the supply source and the GND pins with the value of 0.1μF and more than 100μF which are featuring higher frequency efficiency.

When the speaker load condition, it is recommendable to insert the resisitor of 10Ω and the capacitor of 0.047μF between the output and the GND pins.

- **How to use the Input Resistor** (TYP. 50kΩ)

The input resistors have much deviation in value generally, so that it is recommended not to use them as the constant of the circuit. The countermeasure to be recommended is to apply the resistor of higher in value, which is so higher to be able to ignore the input deviation (3kΩ approximately) in parallel application.



- **Maintenance of Output Offset Voltage**

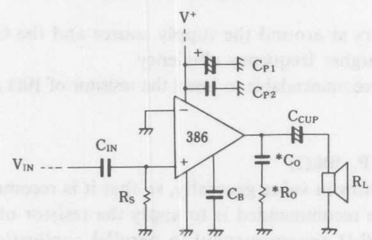
By making connection of both input pins with low value (below 10kΩ approximately) to GND, the output offset voltage is automatically set in the medium range value of the supply source. However, the DC Gain of NJM386 is approximately at 20 times in value, so that when keeping one side input pin open, and the other side to GND on DC condition. The voltage drop caused by input resistor × input bias current, that is, (input resistor × input bias current)× 20 times voltage is to be sheared, which in the result, no distortion output Oscillation range shall be decreeased.

In regard to dealing with the input pin, it is recommendable to put the input pin into the GND at first, and the other side of signal input pin, to be connected into GND with the resisitor of less than about 10kΩ on DC condition.

- **The Application Purpose and Recommended Value of the External Parts.**

EXTERNAL PARTS	APPLICATION PURPOSE	RECOMMENED VALUE	REMARKS
R_S	Current like noise reduction V_{OQ} stabilization	Below 10kΩ	The noise becomes high when the input pin opend.
C_{IN}	V_{OQ} stabilization	1μF	It is not required in case when there is no DC offset in the input signal.
C_{P1}	V^+ stabilization	$\cong C_{cup}$	It can be decreased in value when the output impedance source is low.
C_{P2}	Oscitallation prevention	0.1μF	Insert near around the supply source and GND pins.
C_V	Ripple rejection to V_O by way of V^+	47μF	It is not required when the V^+ is stabilized.
$^*C_O$	Oscillation preventon	0.047μF	To be decided in value according to load condition.
$^*R_O$	Oscillation prevention	10Ω	To be decided in value according to load condition.
C_{CUP}	Output DC decoupling	470μF when R_L =4Ω 220μF when R_L =8Ω	Low band cutoff frequency (f_L) shall be decided by C_{CUP} R_L . When C_{CUP} is less in value, f_L is to be increassed.

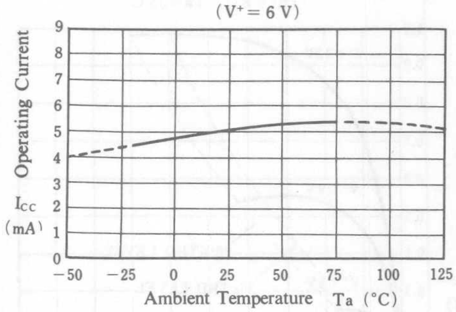
NJM386B Recommended Circuit



■ TYPICAL CHARACTERISTICS

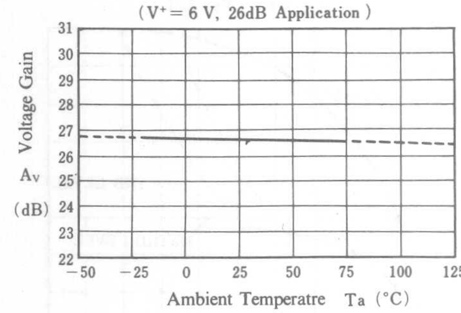
Operating Current vs. Temperature

($V^+ = 6$ V)



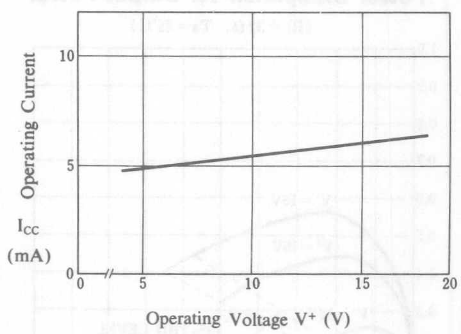
Voltage Gain vs. Temperature

($V^+ = 6$ V, 26dB Application)



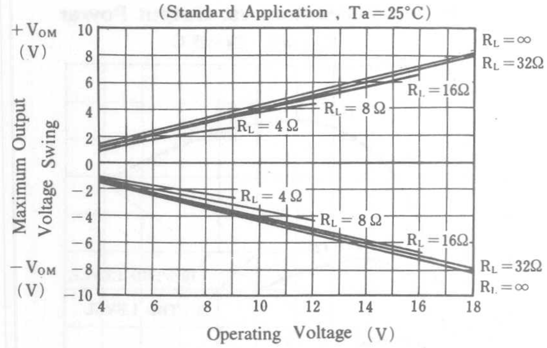
Operating Current vs. Operating Voltage

(Ta=25°C)



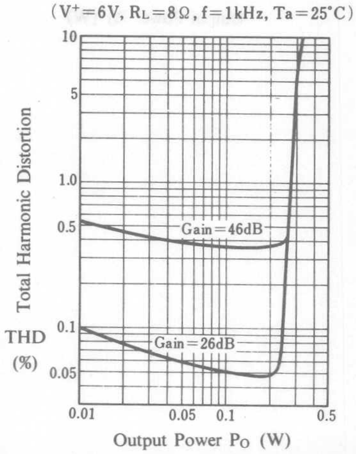
Maximum Output Voltage Swing vs. Operating Voltage

(Standard Application, Ta=25°C)

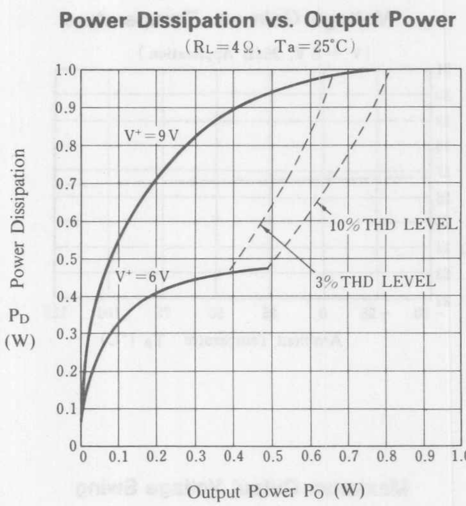


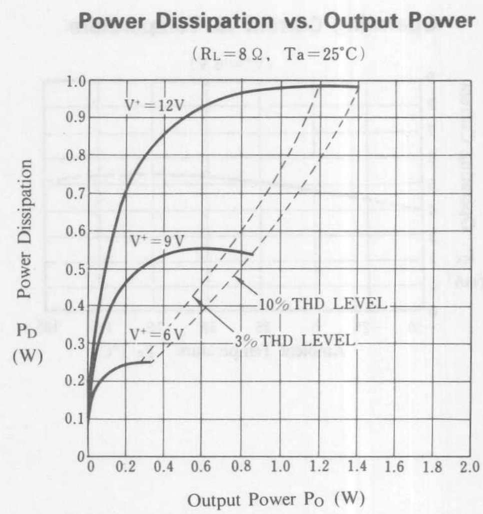
Total Harmonic Distortion vs. Output Power

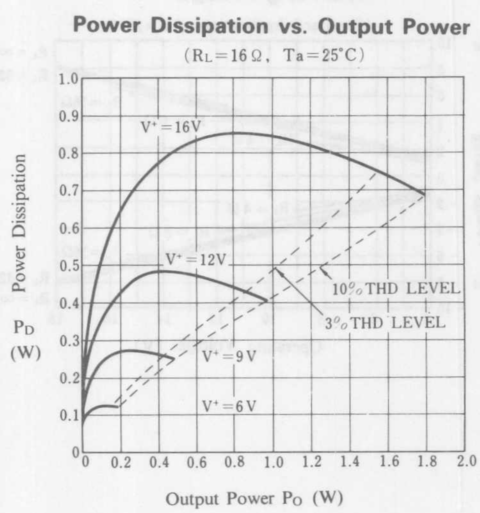
(V^+=6V, R_L=8Ω, f=1kHz, Ta=25°C)

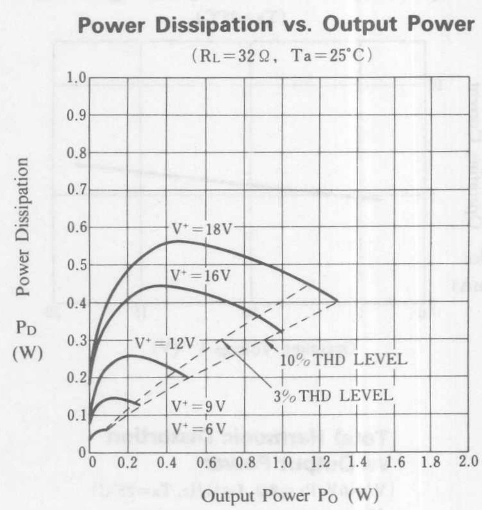


■ TYPICAL CHARACTERISTICS









STEREO MODULATOR

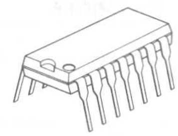
■ GENERAL DESCRIPTION

The NJM2035 is an integrated circuit used to generate a stereo composite signal and obtain switching output and 19kHz pilot signal due to two input audio signal and 38kHz X-tal and a few external CR.

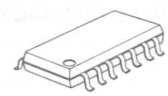
The NJM2035 operates at 1.5V battery typically and even at 1.2V obtains separation more than 25dB.

NJM2035 can generate stereo multiplex signal easily by combination battery generator section.

■ PACKAGE OUTLINE



NJM2035D

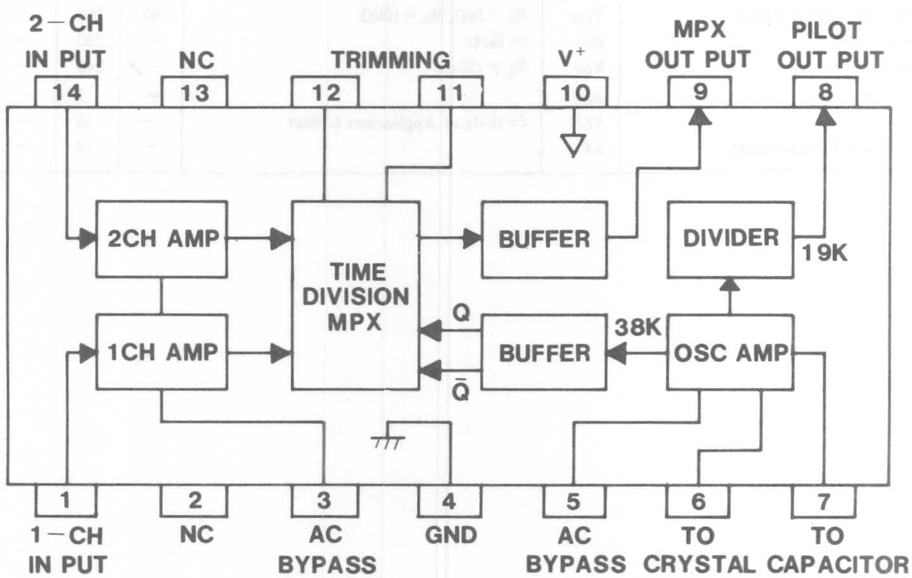


NJM2035M

■ FEATURES

● Low Operating Voltage	($V^+ \geqq 1.0V$)
● Low Operating Current	($Icc \leqq 3.0mA$)
● High Separation	($SEP \geqq 25dB$)
● Voltage Gain	(20～200)
● Separation Adjustable	
● Package Outline	DIP14, DMP14
● Bipolar Technology	

■ BLOCK DIAGRAM



NJM2035D
NJM2035M

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	3.6	V
Power Dissipation	P_D	(DIP14) 500 (DMP14) 300	mW mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

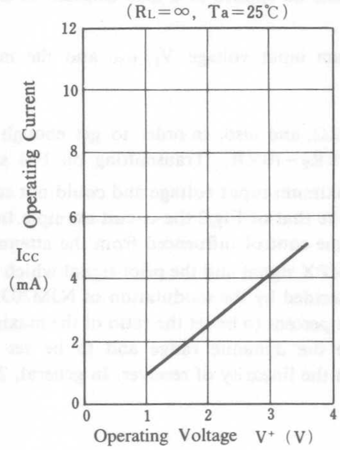
(Ta=25℃, V^+=1.5V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Cuurent	I_{CC}	$R_L=\infty$	—	1.8	3.0	mA
Input Impendance	Z_{IN}	f=1kHz	—	420	—	Ω
Maximum Input Current	I_{IM}		—	4.1	—	μA
Voltage Gain	G_V	$R_S=2k\Omega$, $R_L=10k\Omega$	16	20	—	dB
Difference Gain Between Channels	G_{VD}	$R_S=2k\Omega$, $R_L=10k\Omega$	—	—	2.0	dB
Equivalent Input Noise Voltage	V_{NI}	$R_S=2k\Omega$, $R_L=10k\Omega$, AWEIGHTED	—	—	2.0	μVrms
Maximum Output Voltage Swing	V_{OM}	$R_S=2k\Omega$, $R_L=10k\Omega$	140	200	—	mVp-p
Output Impendance	Z_O	f=1kHz	—	230	—	Ω
Pilot Output Voltage	V_{OP}	$R_L=150k\Omega$	—	240	—	mV
Pilot Output Impendance	R_{OP}		—	3	—	kΩ
Separation	SEP	f=1kHz at Application Circuit	—	40	—	dB
Internal Separation Compensation	S.C		—	−19	—	dB

■ TYPICAL CHARACTERISTICS (✻: BY APPLICATION CIRCUIT)

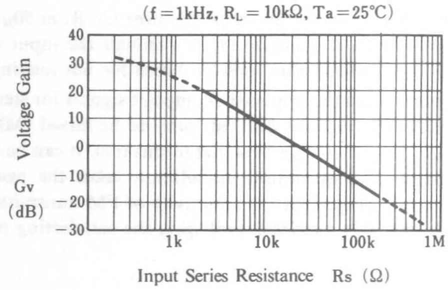
Operating Current vs. Operating Voltage

($R_L=\infty$, $Ta=25°C$)



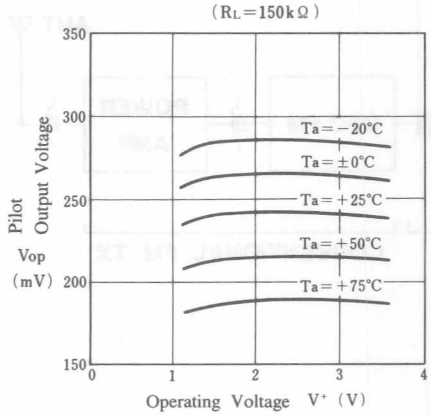
Voltage Gain vs. Input Series Resistance

($f=1kHz$, $R_L=10k\Omega$, $Ta=25°C$)



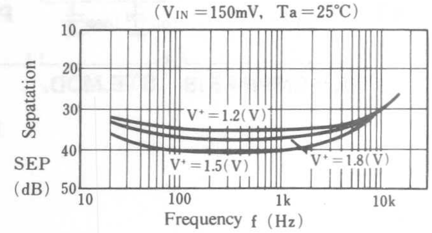
Pilot Output Voltage vs. Operating Voltage

($R_L=150k\Omega$)



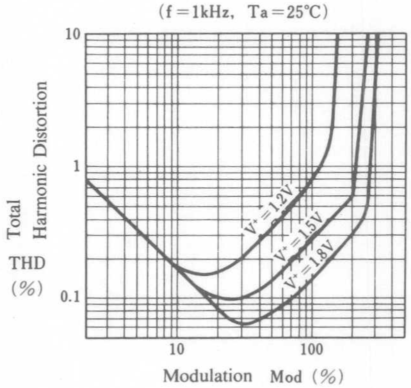
✻ Separation vs. Frequency

($V_{IN}=150mV$, $Ta=25°C$)



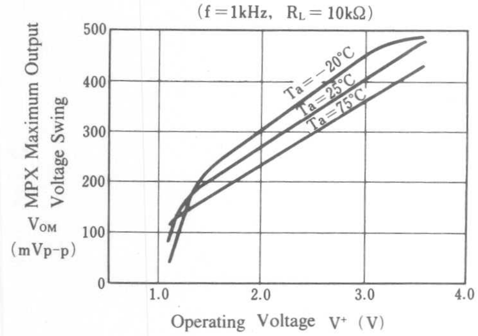
✻ Total Harmonic Distortion vs. Modulation

($f=1kHz$, $Ta=25°C$)



MPX Maximum Output Voltage Swing vs. Operating Voltage

($f=1kHz$, $R_L=10k\Omega$)



■ APPLICATION CIRCUIT EXAMPLES

The following block diagram shows an FM stereo transmitter using NJM2035. Input a current mode signal, because two inputs of NJM2035 are of a low impedance type. Also, the pre-emphasis can be applied at a time constant of C_L and R_L by utilizing this characteristic.

Input series resistance Rs of low band can be obtained from the maximum input voltage $V_{IM(P-P)}$ and the maximum input current I_{IM} of NJM2035.

$$Rs=V_{IM}/2I_{IM} \quad (Rs=R_1+R_2)$$

However, the circuit for stabilized operation, R_2 must stay between $2\sim12k\Omega$, and also, in order to get enough pre-emphasis characteristics, R_1 is repuired to maintain within the range of $5\times R_2\sim10\times R_2$. Transmitting on FM stereo. it is advisable to set the pre-emphasis time C_1, R_1 at $50\mu s$. When it is large maximum input voltage and could not satisfy R_1, R_2 condition, it is important to attenuate the input voltage beforehand, like that of Fig.2 the circuit example. In this case however, special care must be taken for not making the pre-emphasis time control influenced from the attennuter.

In order to get the important composit signals for stereo transmitting, the MPX signal and the pilot signal which were delivered output at each different pins, to be mixed (MIX) and the ratio is decided by the modulation of NJM2035 the maximum output voltage V_{OM} that means that, it can be decided by how much percent to be set the ratio of the maximum modulation. The maximum modulation takes the essential part to decide the dynamic range and to be set with consideration of modulation sensitivity of FM transmitter, S/N and also with the linearity of receiver. In general, 200% modulation ($\Delta f=\pm150MHz$) will give the satisfacting result.

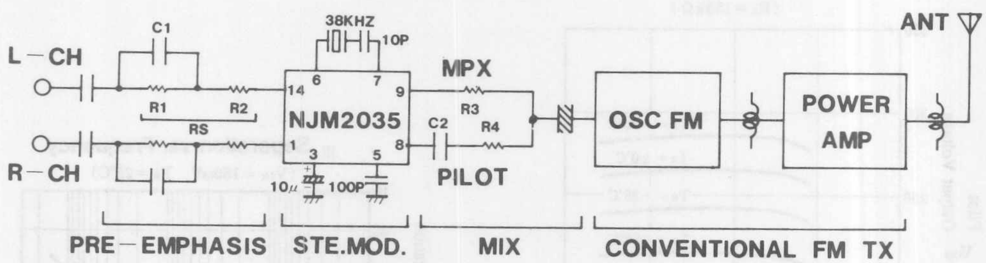


Fig1

■ RECOMMENDED APPLICATION CIRCUIT & EACH WAVEFORM

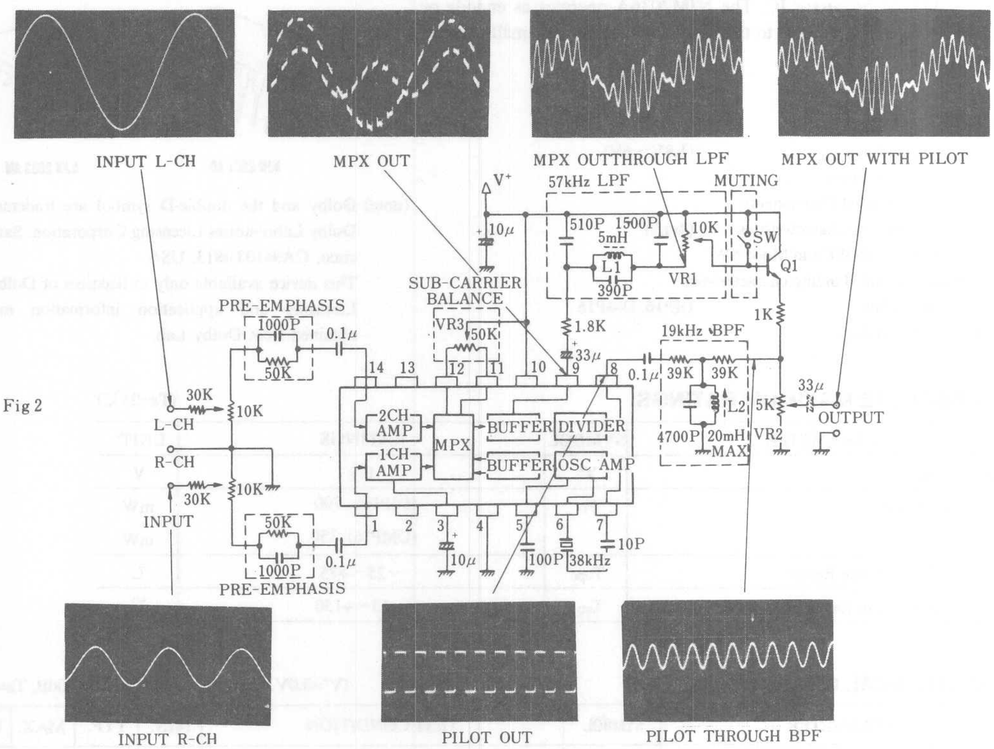


Fig 2

Recommended Appkication Circuit & Each Waveform on the other hand, the pilot level is to be modulated 10% with no connection of Max. modulation ratio, so that the following relation can be set.

$$\frac{R_O+R_3}{R_{OP}+R_4}\times\frac{2\sqrt{2}\,V_{OP}}{V_{OM}}\doteqdot\frac{10}{200}$$

Howerer, for the stability in operation, it is advisable to control MPX signal loading more than 1.8kΩ, and the pilot signal loading more than 39kΩ.

As in example of Fig.1 Simplified Application Circuit, when making the rectangular wave like output to be the composit signal itself, the separating effect shall be reduced due to influence by harmonic components included in MPX signal, so that it requires to make the adjustment to be able to get ample separation of pilot signal phase by the operation ot C_2, R_4, time signal. In this procedure, there is defectine side of getting slightly difference of the best position of separating effect depending upon the tunner of receiver's side, however, when $R_3=2k\Omega$, $R_4=150k\Omega$, $C_2=330pF$ then the ample separation can be obtained practically.

Special care must be taken that the pilot signal's the third harmonic wave 57kHz will be the cause of dangerous beating.

Fig 2 idicates the example of recommende application circuit of stereo modulaton when NJM2035 in used. As explained in the wave form, high quality composit signal can be obtained by only putting a simpl filter beforehand. Then the previousely mentioned problems can be improved a great deal.

The input in mondulated 30% at AUX level (150mV) —— changeable of +3dB~−∞ by volume control.

V_{R1} corresponds to the fluctuation of GV feature of NJM2035, and also for fluctuation of modulation sensitivity of FM modulation circuit which in connected after V_{R2}.

V_{R3} is to make minimum adjustment of 38kHz sub-carrier leakage, and with this adjustment, it can control until about −50dB in comparing to 100% modulation level.

■ The adjustment proceduce in the recommended application circuit.

① Sub-carrier leakage can be minimized by the adjustment of V_{R3}.
② The maximum output voltage of pilot can be obtained by the adjustment of L_2
③ V_{R2} adjustment of the pilot will help to bring the modulation ratio a little over 10% ($\triangle f=\pm7.5kHz$)
④ The modulation ratio can be increased as much as 30% at V_{R1} by putting designed standard input.
⑤ By putting only the input for L-channel, and making re-adjustment of L_2, so that the maximum power of output at L-cannel can be obtained at the receiver's side. (19kHz phase adjustment)
Against 100% modulation at the recommended circuit S/N at A curve +15kHz LPF 77dB, ane at 15kHz LPF 67dB approximately can be obtained.

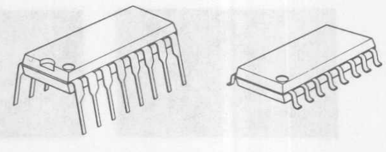
■ GENERAL DESCRIPTION

The NJM2063A is the dual low-voltage operating DOLBY B-type noise reduction processor IC. The NJM2036A operates as encode or decode mode and is suitable to the headphone stereo and small cassette tape recorder.

■ FEATURES

- Operating Voltage (1.8V~6V)
- 16 pins, Dual Circuit
- Minimum External Components
- Good temperature characteristics (4mA)
- Internal NR ON/OFF and Mode SW
- Excellent Signal Handing characteristics
- Package Outline DIP16, DMP16
- Bipolar Technology

■ PACKAGE OUTLINE



NJM 2063 AD NJM 2063 AM

(note) Dolby and the double-D symbol are trademarks of Dolby Labolatories Licensing Corporation. San Francisco, CA94103-4813, USA.
This device available only to licensees of Dolby Lab. Licensing and application information may be obtained from Dolby Lab.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	6.5	V
Power Dissipation	P_D	(DIP16) 700	mW
		(DMP16) 350	mW
Operating Temperature Range	T_{opr}	−25~+75	℃
Storage Temperature Range	T_{stg}	−55~+150	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=3.0V. Dolby Level=100mVrms=0dB, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+	—	1.8	3.0	6.0	V
Operating Current	I_{CC}	NR ON (ENCODE)	—	8.0	15.0	mA
Voltage Gain	$G_{v2\text{-}3}$ / $G_{v15\text{-}14}$	f=1kHz, 0dB	9.0	10.0	11.0	dB
	$G_{v2\text{-}4}$ / $G_{v15\text{-}13}$		9.0	10.0	11.0	dB
Total Harmonic Distortion	THD	f=1kHz, ENCODE	—	0.2	0.6	%
Signal Handing	—	V^+=1.8V, f=1kHz, THD<1%	12.0	—	—	dB
S/N Ratio	S/N	Rg=5.6kΩ CCIR/ARM FILTER				
		Encode	64.0	72.0		dB
		Decode	—	83.0	—	
		NR-OFF	—	74.0	—	
N.R Encode Boost $20\log\frac{V_{3(14)}(\text{N.R ON})}{V_{3(14)}(\text{N.R OFF})}$	ENC-1.4k	f=1.4kHz, $V_{3(14)}$(N.R OFF)=−20dB	2.9	4.4	5.9	dB
	ENC-1.4k	f=1.4kHz, $V_{3(14)}$(N.R OFF)=−30dB	6.0	7.5	9.0	dB
	ENC-5k	f=5kHz, $V_{3(14)}$(N.R OFF)=−20dB	1.7	3.2	4.7	dB
	ENC-5k	f=5kHz, $V_{3(14)}$(N.R OFF)=−30dB	6.7	8.2	9.7	dB
	ENC-10k	f=10kHz, $V_{3(14)}$(N.R OFF)=0dB	−1.1	0.4	1.9	dB
	ENC-10k	f=10kHz, $V_{3(14)}$(N.R OFF)=−40dB	9.8	10.4	11.8	dB

DOLBY B·C TYPE NOISE REDUCTION PROCESSOR

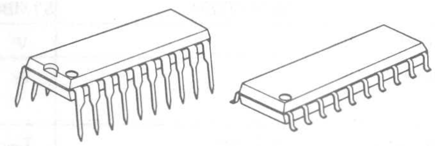
■ GENERAL DESCRIPTION

The NJM2065A is a low-voltage operating DOLBY B·C-type noise reduction processor IC. The NJM2065A is a suitable to the headphone stereo and small cassette tape recorder.

■ FEATURES

- Low Operating Voltage (1.8V~6.0V)
- Minimum External Components
- Good temperature characteristics (4mA)
- Internal Switch of NR ON/OFF ENCODE/DECODE
- Dolby Level Encode Output Level 100mVrms
  Decode Output Level 100mVrms
- Package Outline DIP20, DMP20
- Bipolar Technology

■ PACKAGE OUTLINE



NJM2065AD NJM2065AM

(note) Dolby and the double-D symbol are trademarks of Dolby Labolatories Licensing Corporation. San Francisco, CA94103-4813, USA.
This device available only to licensees of Dolby Lab. Licensing and application information may be obtained from Dolby Lab.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	6.5	V
Power Dissipation	P_D	(DIP16) 700	mW
		(DMP16) 350	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=3.0V. (note 1). Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION R/P	NR	f(Hz)	OTTHER CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_{opc}					1.8		6	V
Operating Current	I_{cc}	R	OFF		No signal	1.5	3	5	mA
Voltage Gain (REC)	G_{VR}	R	OFF	1k		9	10	11	dB
(MON)	G_{VM}	R	OFF	1k		9	10	11	dB
Encode Characteristics									
B Type (1)	B-1	R	B	5k	0dB	−1.2	0.3	1.8	dB
B Type (2)	B-2	R	B	1.4k	−15dB	0.8	2.3	3.8	dB
B Type (3)	B-3	R	B	1k	−25dB	4.2	5.7	7.2	dB
B Type (4)	B-4	R	B	5k	−30dB	6.7	8.2	9.7	dB
B Type (5)	B-5	R	B	5k	−40dB	9.8	10.3	11.8	dB
C Type (1)	C-1	R	C	5k	0dB	−4.3	−2.3	−0.3	dB
C Type (2)	C-2	R	C	1k	−20dB	3.9	5.9	7.9	dB
C Type (3)	C-3	R	C	500	−30dB	9.8	11.8	13.8	dB
C Type (4)	C-4	R	C	700	−40dB	14.5	16.5	18.5	dB
C Type (5)	C-5	R	C	5k	−60dB	19.4	20.4	22.4	dB
Decode Characteristics									
B Type	B_d	P	B	5k	−30dB		−8.2		dB
C Type	C_d	P	C	1k	−40dB		−16.5		dB
Signal Handling	SH	P	C	1k	THD=1%. V^+=1.8V	12	13		dB
S/N Ratio(PIN9)									
C Type	SN_c	R	C		Rg=5.6kΩ CCIR/ARM	60	62		dB
B Type	SN_B	R	B		Rg=5.6kΩ CCIR/ARM		71		dB
NR OFF	SN_o	R	OFF		Rg=5.6kΩ CCIR/ARM		78		dB
Total Harmonic Distortion									
NR OFF (REC)	THD1	R	OFF	1k	0dB		0.03	0.2	%
NR OFF (MON)	THD2	P	OFF	1k	0dB		0.03		%
B Type (REC)	THD3	R	B	1k	0dB		0.05		%
B Type (MON)	THD4	P	B	1k	0dB		0.05		%
C Type (REC)	THD5	R	C	1k	0dB		0.09	0.4	%
C Type (MON)	THD6	P	C	1k	0dB		0.08		%
Control Voltage									
REC	V_{ctR}	Voltage between both terminals of 10kΩ register connected to pin 20				0		0.2	V
PLAY	V_{ctP}	Voltage between both terminals of 10kΩ register connected to pin 20				1.6		V^+	V
NR OFF	V_{ctO}	Voltage between both terminals of 8.2kΩ register connected to pin 1					open		V
B Type	V_{ctB}	Voltage between both terminals of 8.2kΩ register connected to pin 1				1.6		V^+	V
C Type	V_{ctC}	Voltage between both terminals of 8.2kΩ register connected to pin 1				0		0.2	V

(note 1): Definition of 0dB DOLBY LEVEL.

Encode Mode: On NR-OFF condition. put 400 Hz input signal to PIN19, and adjust the voltage of PIN15 to 31.6mV, At this condition the voltage of PIN9 is about 100mV which is 0dB.

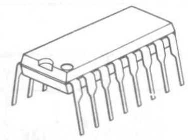
Decode Mode: On NR-OFF condition, put 400Hz input signal, to PIN19, and adjust the voltage of PIN15 to 31.6mV. At this condition the voltage of PIN10 is about 100mV which is 0dB.

3V AUTO-REVERSE DUAL PRE-AMPLIFIER

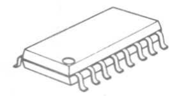
■ GENERAL DESCRIPTION

NJM2067 is dual pre-amplifier including channel switch which was designed for 3V Auto-reverse Head Phone Stereo.

■ PACKAGE OUTLINE



NJM2067D

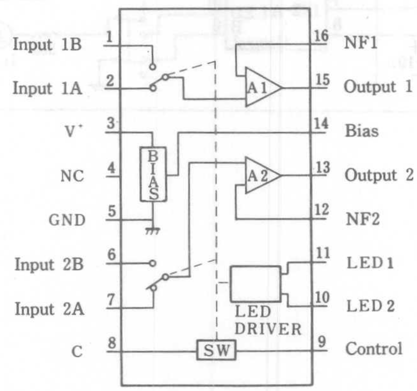


NJM2067M

■ FEATURES

- Internal Switch of Input Channel
- Package Outline DIP16, DMP16
- Bipolar Technology

■ PIN CONFIGURATION



NJM2067D
NJM2067M

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

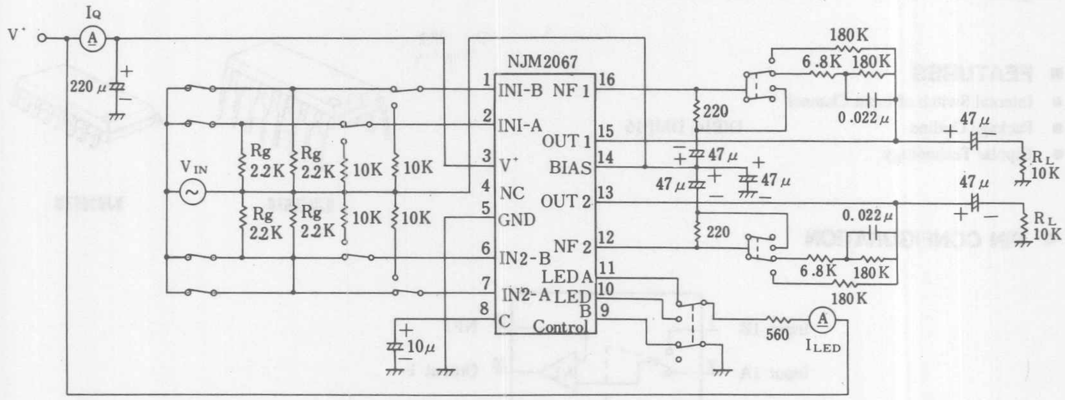
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	4.5	V
Power Dissipation	P_D	(DIP16) 700	mW
		(DMP16) 350	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V^+=3V, R_L=10kΩ)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	V_{IN}=0V	0.9	2.3	4.0	mA
Open Loop Voltage Gain	G_V	V_O=−10dBm, f=1kHz	70	80	—	dB
Equivalent Input Noise Voltage	V_{NI}	V_{IN}=0, R_g=2.2kΩ	—	1.2	—	μVrms
Maximum Output Voltage	V_{OM}	THD=1%, f=1kHz	250	450	—	mVrms
Crosstalk between Channels	CST	Other channels V_O=−10dBm, f=1kHz	55	65	—	dB
Crosstalk between A and B Channel	CT	Other chanels V_O=−10dBm, f=1kHz	55	65	—	dB
Total harmonic Distortion	THD	V_O=0.2Vrms, f=1kHz	—	0.08	0.15	%
Input Bias Current	I_B	V_{IN}=0Vrms	—	100	310	nA
Maximum LED Current	I_{LED}		—	5	—	mA

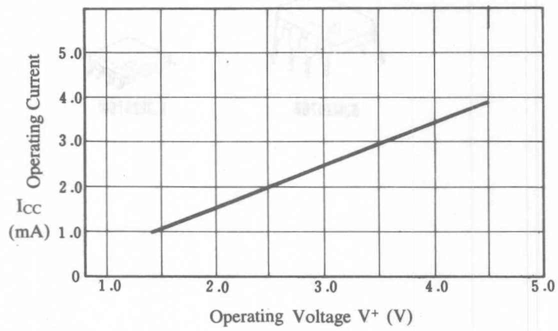
■ TEST CIRCUIT



■ TYPICAL CHARACTERISTICS

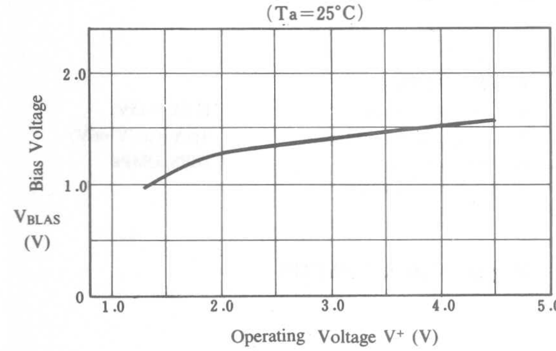
Operating Current vs. Operating Voltage

($V_{IN}=0V$, $Ta=25°C$)



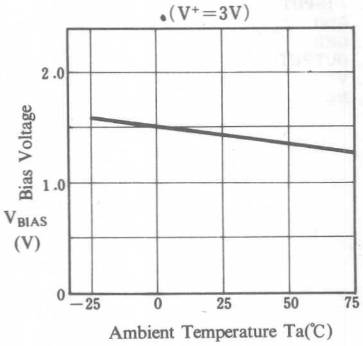
Bias Voltage vs. Operating Voltage

($Ta=25°C$)



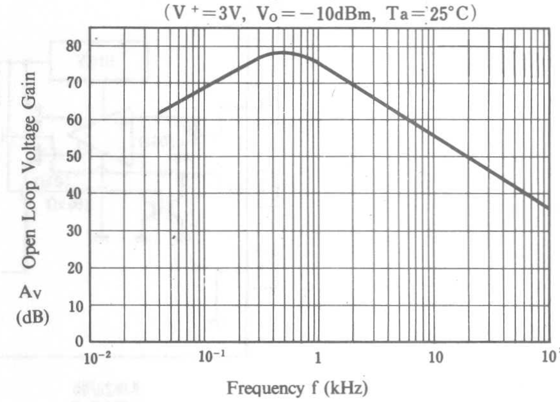
Bias Voltage vs. Ambient Temperature

($V^+=3V$)



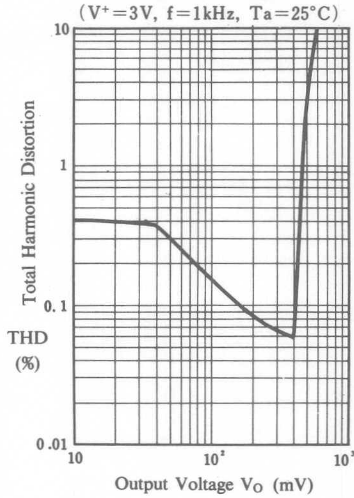
Open Loop Voltage Gain vs. Frequency

($V^+=3V$, $V_O=-10dBm$, $Ta=25°C$)



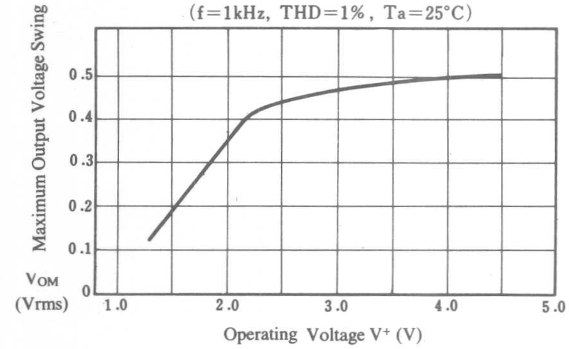
Total Harmonic Distortion vs. Output Voltage

($V^+=3V$, $f=1kHz$, $Ta=25°C$)



Maximum Output Voltage Swing vs. Operating Voltage

($f=1kHz$, $THD=1\%$, $Ta=25°C$)



LOW VOLTAGE POWER AMPLIFIER

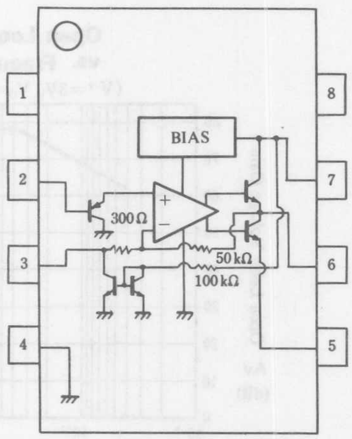
■ GENERAL DESCRIPTION

NJM2070 is a power amplification monolithic IC of wide Operating voltage range. It is applied for audio power amplifier in portable radio and handy cassette player.

■ FEATURES

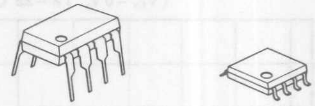
● Operating Voltage	(1.8V～15V)
● Low Operating Current	4mA typ : V^{+}=6V)
● Package Outline	DIP8, DMP8
● Bipolar Technology	

■ PIN CONFIGURATION



NJM2070D
NJM2070M

■ PACKAGE OUTLINE



NJM2070D NJM2070M

PIN FUNCTION

1 . NC
2 . +INPUT
3 . −INPUT
4 . GND
5 . GND
6 . OUTPUT
7 . V^{+}
8 . NC

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Output Peak Current	I_{OP}	1	A
Power Dissipation	P_D	(DIP8) 700	mW
		(DMP8) 500 (note)	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

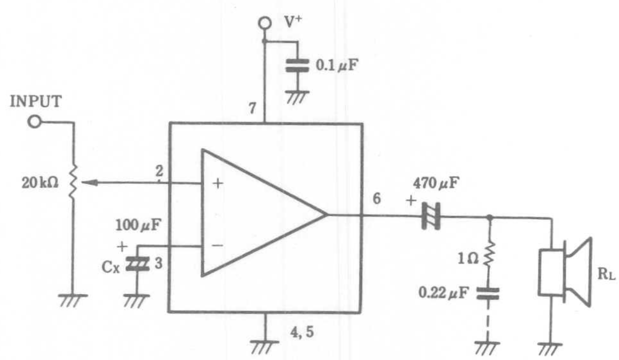
(note) At on PC board

■ ELECTRICAL CHARACTERISTICS

(V^+=6V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		1.8	—	15	V
Output Voltage	V_O		—	2.7	—	V
Operating Current	I_{CC}	$R_L=\infty$	—	4	7	mA
Input Bias Current	I_{IB}		—	200	—	nA
Output Power		THD=10%, f=1kHz				
	P_O	V^+=6V, R_L=4Ω	0.5	0.6	—	W
	P_O	V^+=4.5V, R_L=4Ω	—	0.32	—	W
	P_O	V^+=3V, R_L=4Ω	—	120	—	mW
	P_O	V^+=2V, R_L=4Ω	—	30	—	mW
		THD=1%, f=1kHz				
	P_O	V^+=6V, R_L=4Ω	—	500	—	mW
	P_O	V^+=4.5V, R_L=4Ω	—	250	—	mW
Total Harmonic Distortion	THD	P_O=0.4W, R_L=4Ω, f=1kHz	—	0.25	—	%
Voltage Gain	A_V	f=1kHz	41	44	47	dB
Input Impedance	Z_{IN}	f=1kHz	100	—	—	kΩ
Equivalent Input Noise Voltage	V_{NI1}	R_S=10kΩ, A Curve	—	2.5	—	μV
	V_{NI2}	R_S=10kΩ, B=22Hz～22kHz	—	3	—	μV
Ripple Rejection	RR	f=100Hz, C_X=100μF	24	30	—	dB
Cut Off Frequency	f_H	A_V=−3dB from f=1kHz R=8Ω, P_O=250mW	—	200	—	kHz

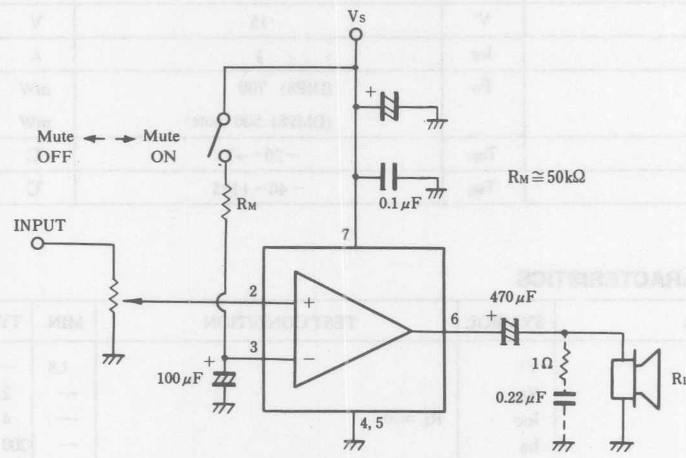
■ TYPICAL APPLICATION AND TEST CIRCUIT



■ OSCILLATION PREVENTION

Put in series a 1Ω resistor and a 0.22 μF capacitor on parallel to load, if the load is speaker. Recommend putting in parallel between pin 4 and pin 7, 0.1 μF and more than 100 μF capacitors with good high frequency characteristics near to the ground and supply voltage pins on parallel.

■ MUTING CIRCUIT

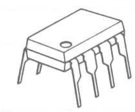


SIGNAL LEVEL SENSOR SYSTEM

■ GENERAL DESCRIPTION

The NJM2072 is a monolithic integrated circuit designed for signal level sensor system. The NJM2070 features low power, low voltage operation, and high input sensitivity and is suited for the signal level sensor system for micro cassette, vox for telecommunications.

■ PACKAGE OUTLINE



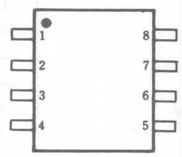
NJM2072D

NJM2072M

■ FEATURES

- Operating Voltage (0.9V~7V)
- Low Operating Current 0.55mA typ.
- High Input Sensitivity -36dB typ.
- Package Outline DIP8, DMP8
- Bipolar Technology

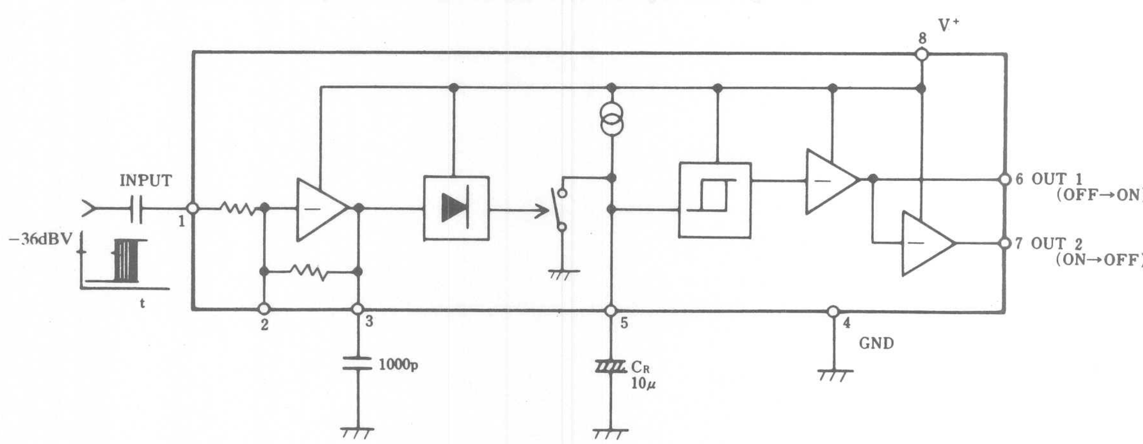
■ PIN CONFIGURATION



NJM2072D
NJM2072M

PIN FUNCTION
1. INPUT
2. Gain Control
3. Amp. Output
4. GND
5. Capacitor for Recovery time
6. OUT1
7. OUT2
8. V⁺

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
Operating Temperature Range	T_{opr}	$-25 \sim +75$	℃
Storage Temperature Range	T_{stg}	$-40 \sim +125$	℃
Maximum Input Voltage	V_{imax}	$V^+ - 1$	V

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V+=3V)

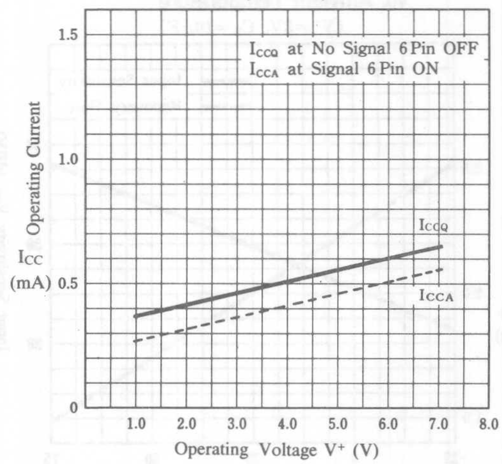
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		0.9	—	7	V
Operating Current	I_{cc}	$V_{IN}=0mVrms, R_L=\infty$	0.2	0.55	1.5	mA
Input Sensitivity	V_{ins}	f=1kHz	-39	-36	-33	dBV
Attack Time (note 1)	T_{atc}	$C_R=10\mu F$, f=1kHz	—	1	25	mSec
Recovery Time (note 2)	T_{rec}	$C_R=10\mu F$, f=1kHz	—	2	—	Sec
Output Current at ON(OUT 1)	$I_{O1\ on}$	$V_{in}=30mVrms$, $V_o=0.3V$	1	3	—	mA
Output Current at ON(OUT 2)	$I_{O2\ on}$	$V_{in}=0mVrms$, $V_o=0.3V$	1	3	—	mA
Output Current at OFF(OUT1)	$I_{O1\ off}$	$V_{in}=0mVrms$, $V_o=8V$	—	—	1	μA
Output Current at OFF(OUT2)	$I_{O2\ off}$	$V_{in}=30mVrms$, $V_o=8V$	—	—	1	μA
Input Resistance	R_{in}		16	20	24	kΩ
Charge Current	I_{chg}		1.0	2.0	3.0	μA

(note 1) Attack Time: Period from putting input signal of more than minimum input sensitive signal to output level change.
(note 2) Recovery Time: Period from input signal becoming lower than minimum input sensitine signal to output level change.

■ TYPICAL CHARACTERISTICS

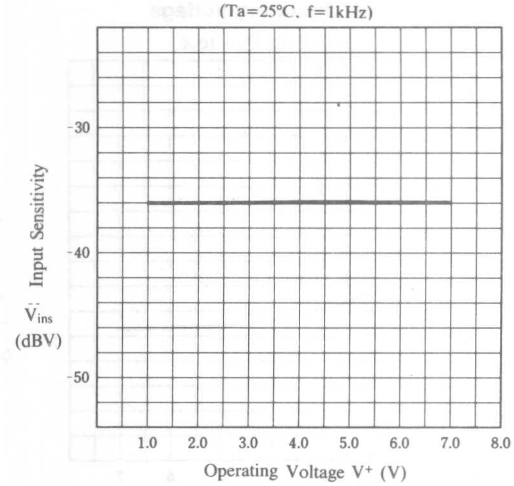
Operating Current vs. Operating Voltage

(Ta=25°C)



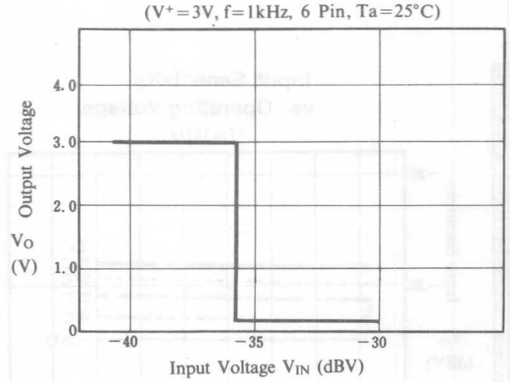
Input Sensitivity vs. Operating Voltage

(Ta=25°C, f=1kHz)

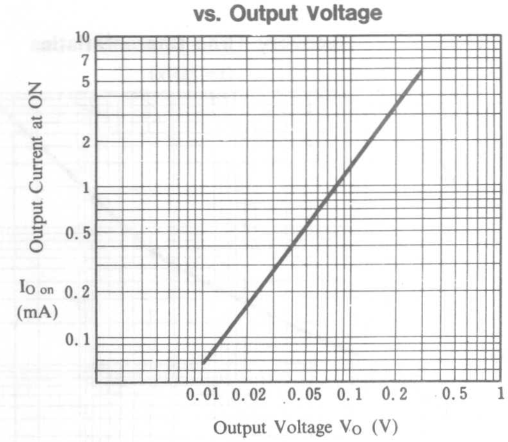


Output Voltage vs. Input Voltage

(V+=3V, f=1kHz, 6 Pin, Ta=25°C)

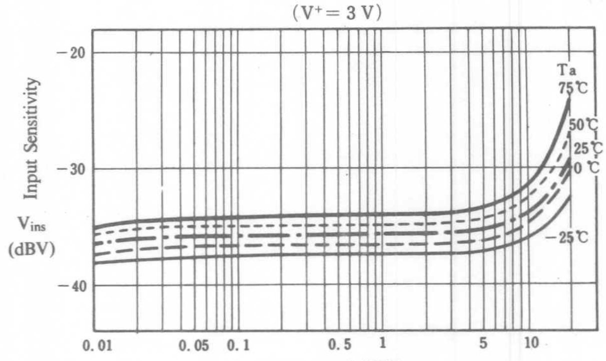


Output Current at ON vs. Output Voltage



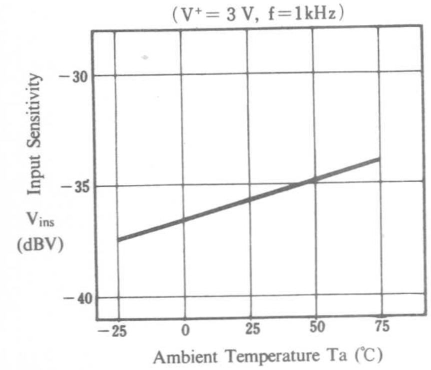
Input Sensitivity vs. Frequency

(V+ = 3 V)



Input Sensitivity vs. Ambient Temperature

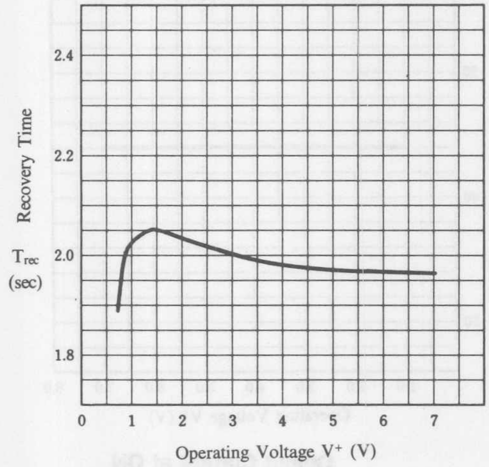
(V+ = 3 V, f=1kHz)



■ TYPICAL CHARACTERISTICS

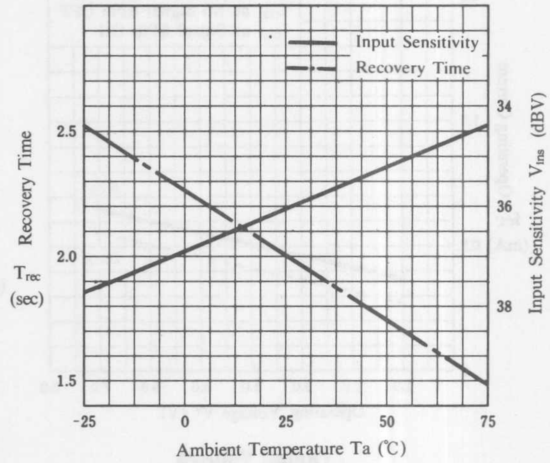
Recovery Time vs. Operating Voltage

(Ta=25°C, C_R=10μF)



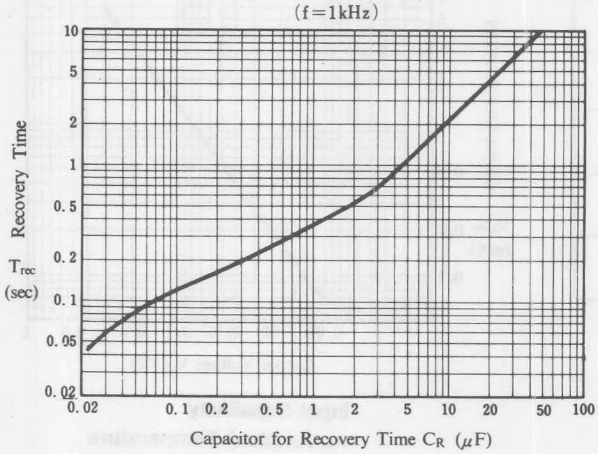
Input Sensitivity Recovery Time vs. Amvient Temperature

(V^+=3V, C_R=10μF)



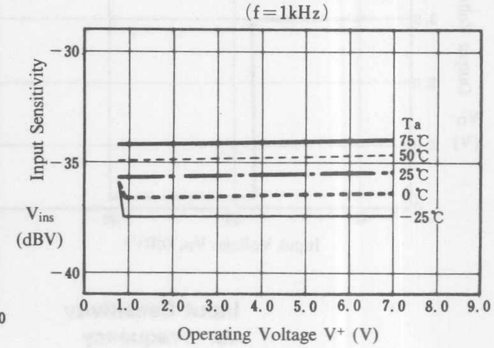
Recovery Time Characteristics

(f=1kHz)

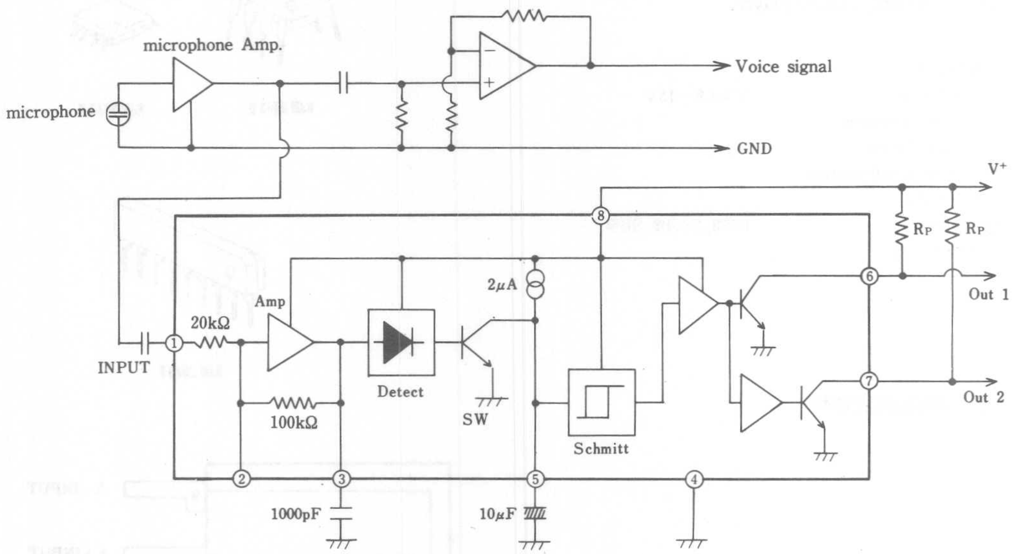


Input Sensitivity vs. Operating Voltage

(f=1kHz)



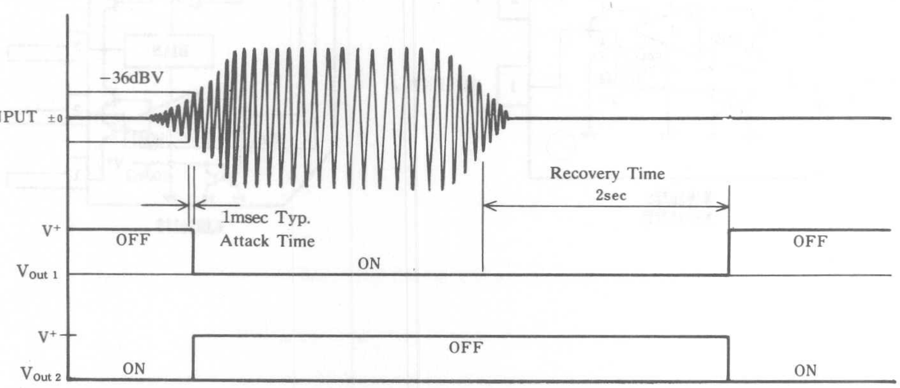
■ TYPICAL APPLICATIONS



Pins 6 and 7 show an open collector. Mount resistor R_p shown by the following equation.

$$R_p = (V^+_{MIN} - 0.2)/0.3\ (k\Omega)$$

Resistor R_P to pin 7 is omissible, if pin 6 only is used. But resistor R_P to pin 6 should be put when Out 2 only is used. V^+_{MIN} is minimum supply voltage.



DUAL LOW VOLTAGE POWER AMPLIFIER

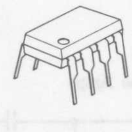
■ GENERAL DESCRIPTION

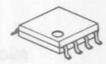
The NJM2073 is a monolithic integrated circuit in 8 lead dual-in-line package, which is designed for dual audio power amplifier in portable radio and handy cassette player.

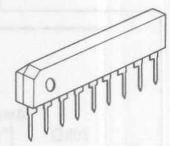
■ FEATURES

- Operating Voltage V^+=1.8~15V
- Low Crossover Distortion
- Low Operating Current
- Bridge or Stereo Configuration
- No Turn-on Noise
- Package Outline DIP8, DMP8, SIP9
- Bipolar Technology

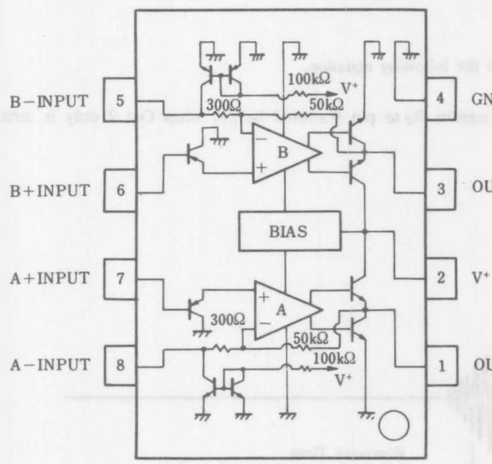
■ PACKAGE OUTLINE


NJM 2073 D

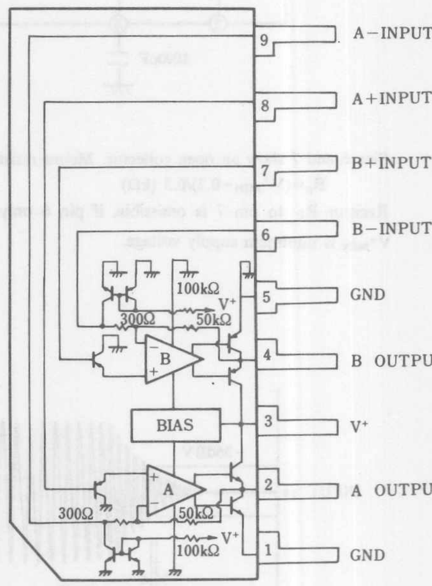

NJM 2073 M


NJM 2073 S

■ PIN CONFIGURATION



NJM2073D
NJM2073M



NJM2073S

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	22	V
Output Peak Current	I_{OP}	1	A
Power Dissipation	P_D	(DIP8) 700	mW
		(SIP9) 700	mW
		(DMP8) 300	mW
Input Voltage Range	V_{IN}	±0.4	V
Operating Temperature Range	T_{opr}	−20~+70	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

■ ELECTRICAL CHARACTERISTICS

(1) BTL Configuration (Test Circuit Fig. 1)

(V^+=6V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		1.8	—	15	V
Operating Current	I_{CC}	$R_L=\infty$	—	6	9	mA
Output Offset Voltage (Between the Outputs)	ΔV_O	$R_L=8\Omega$	—	10	50	mV
Input Bias Current	I_B		—	100	—	nA
Output Power		THD=10%, f=1kHz				
	P_O	V^+=9V, $R_L=16\Omega$ (Note)	—	2.0	—	W
	P_O	V^+=6V, $R_L=8\Omega$ (Note)	0.9	1.2	—	W
	P_O	V^+=4.5V, $R_L=8\Omega$	—	0.6	—	W
	P_O	V^+=4.5V, $R_L=4\Omega$ (Note)	—	0.8	—	W
	P_O	V^+=3V, $R_L=4\Omega$	200	300	—	mW
	P_O	V^+=2V, $R_L=4\Omega$	—	80	—	mW
		THD=1%, f=40kHz~15kHz				
	P_O	V^+=6V, $R_L=8\Omega$	—	1.0	—	W
	P_O	V^+=4.5V, $R_L=4\Omega$	—	0.6	—	W
Total Harmonic Distortion	THD	P_O=0.5W, $R_L=8\Omega$, f=1kHz	—	0.2	—	%
Close Loop Voltage Gain	A_V	f=1kHz	41	44	47	dB
Input Impedance	Z_{IN}	f=1kHz	100	—	—	kΩ
Equivalent Input Noise Voltage	$V_{NI}1$	$R_S=10k\Omega$, A Curve	—	2	—	μV
	$V_{NI}2$	$R_S=10k\Omega$, B=22Hz~22kHz	—	2.5	—	μV
Ripple Rejection	RR	f=100Hz	—	40	—	dB
Cutoff Frequency	f_H	A_V=−3dB from f=1kHz, $R_L=8\Omega$, P_O=1W	—	130	—	kHz

(Note) At on PC Board

(2) Stereo Configuration (Test Circuit Fig. 2)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		1.8	—	15	V
Output Voltage	V_O		—	2.7	—	V
Operating Current	I_{CC}	$R_L=\infty$	—	6	9	mA
Input Bias Current	I_B		—	100	—	nA
Output Power (Each Channel)		THD=10%, f=1kHz				
	P_O	$V^+=6V$, $R_L=4\Omega$ (Note)	0.5	0.65	—	W
	P_O	$V^+=4.5V$, $R_L=4\Omega$	—	0.32	—	W
	P_O	$V^+=3V$, $R_L=4\Omega$	—	120	—	mW
	P_O	$V^+=2V$, $R_L=4\Omega$	—	30	—	mW
		THD=1%, f=1kHz				
	P_O	$V^+=6V$, $R_L=4\Omega$	—	500	—	mW
	P_O	$V^+=4.5V$, $R_L=4\Omega$	—	250	—	mW
Total Harmonic Distortion	THD	$P_O=0.4W$, $R_L=4\Omega$, f=1kHz	—	0.25	—	%
Voltage Gain	A_V	f=1kHz	41	44	47	dB
Channel Balance	ΔA_V		—	—	±1	dB
Input Impedance	Z_{IN}	f=1kHz	100	—	—	kΩ
Equivalent Input Noise Voltage	$V_{NI}1$	$R_S=10k\Omega$, A Curve	—	2.5	—	μV
	$V_{NI}2$	$R_S=10k\Omega$, B=22Hz~22kHz	—	3	—	μV
Ripple Rejection	RR	f=100Hz, $C_X=100\mu F$	24	30	—	dB
Cutoff Frequency	f_H	$A_V=-3dB$ from f=1kHz $R_L=8\Omega$, $P_O=250mW$	—	200	—	kHz

(Note) At on PC Board

■ ELECTRICAL CHARACTERISTICS M-Type

(1) BTL Configuration (Test Circuit Fig. 1)

(V^+=6V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		1.8	—	15	V
Operating Current	I_{CC}	$R_L=\infty$	—	6	9	mA
Output Offset Voltage (Between the Outputs)	ΔV_O	$R_L=8\Omega$	—	10	50	mV
Input Bias Current	I_B		—	100	—	nA
Output Power		THD=10%, f=1kHz				
	P_O	$V^+=6V$, $R_L=16\Omega$ (Note)	—	0.8	—	W
	P_O	$V^+=4V$, $R_L=8\Omega$ (Note)	350	460	—	mW
	P_O	$V^+=3V$, $R_L=4\Omega$ (Note)	200	300	—	mW
	P_O	$V^+=2V$, $R_L=4\Omega$	—	80	—	mW
		THD=1%, f=40Hz~15kHz				
	P_O	$V^+=4V$, $R_L=8\Omega$	—	380	—	mW
Total Harmonic Distortion	THD	$V^+=4V$, $R_L=8\Omega$, $P_O=200mW$, f=1kHz	—	0.2	—	%
Close Loop Voltage Gain	A_V	f=1kHz	41	44	47	dB
Input Impedance	Z_{IN}	f=1kHz	100	—	—	kΩ
Equivalent Input Noise Voltage	V_{NI1}	$R_S=10k\Omega$, A Curve	—	2	—	μV
	V_{NI2}	$R_S=10k\Omega$, B=22Hz~22kHz	—	2.5	—	μV
Ripple Rejection	RR	f=100Hz	—	40	—	dB
Cutoff Frequency	f_H	$A_V=-3dB$ from f=1kHz, $R_L=16\Omega$, $P_O=0.5W$	—	130	—	kHz

(Note) At on PC Board

(2) Stereo Configuration (Test Circuit Fig. 2)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		1.8	—	15	V
Output Voltage	V_O		—	2.7	—	V
Operating Current	I_{CC}	$R_L=\infty$	—	6	9	mA
Input Bias Current	I_B		—	100	—	nA
Output Power (Each Channel)		THD=10%, f=1kHz				
	P_O	$V^+=6V$, $R_L=16\Omega$	—	240	—	mW
	P_O	$V^+=5V$, $R_L=8\Omega$ (Note)	—	270	—	mW
	P_O	$V^+=4V$, $R_L=4\Omega$ (Note)	180	250	—	mW
	P_O	$V^+=3V$, $R_L=4\Omega$	—	120	—	mW
	P_O	$V^+=2V$, $R_L=4\Omega$	—	30	—	mW
		THD=1%, f=1kHz				
	P_O	$V^+=4V$, $R_L=4\Omega$	—	180	—	mW
Total Harmonic Distortion	THD	$V^+=4V$, $R_L=4\Omega$, $P_O=150mW$, f=1kHz	—	0.25	—	%
Voltage Gain	A_V	f=1kHz	41	44	47	dB
Channel Balance	ΔA_V		—	—	±1	dB
Input Inpedance	Z_{IN}	f=1kHz	100	—	—	kΩ
Equivalent Input Noise Voltage	V_{NI1}	$R_S=10k\Omega$, A Curve	—	2.5	—	μV
	V_{NI2}	$R_S=10k\Omega$, B=22Hz~22kHz	—	3	—	μV
Ripple Rejection	RR	f=100Hz, Cx=100μF	24	30	—	dB
Cutoff Frequency	f_H	$A_V=-3dB$ from f=1kHz, $R_L=16\Omega$, $P_O=125mW$	—	200	—	kHz

(Note) At on PC Board

■ TYPICAL APPLICATION & TEST CIRCUIT

Fig.1 BTL Configuration

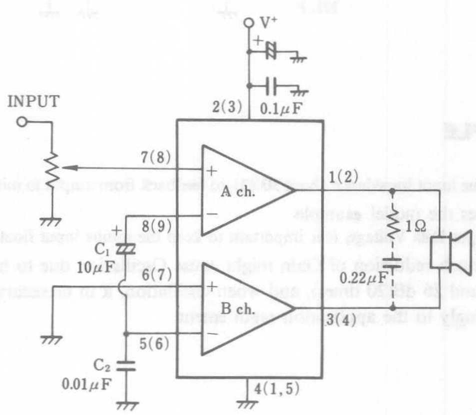
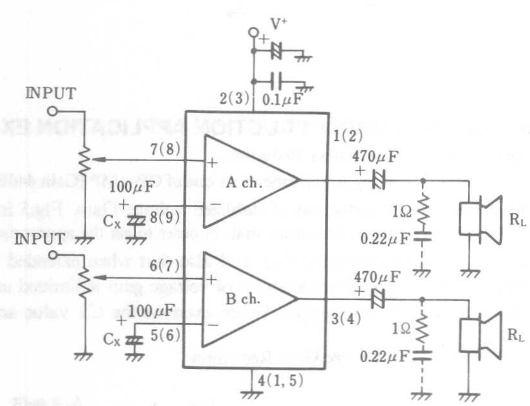


Fig.2 Stereo Configuration

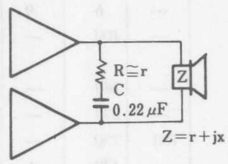


note: pin No. to D,M-Type
( )to S-Type

■ PARASITIC OSCILLATION PREVENTING CIRCUIT

Put 1Ω + 0.22μF on parallel to load, if the load is speaker. Recommend putting 0.1μF and more than 100μF capacitors with good high frequency characteristics in to near ground and supply voltage pins.

In BTL operation of less than 2V supply voltage, parasitic oscillation may be occurred with R = 1Ω. And so recommended R to be the same valve of pure resistance(r) when it is lower than 3V.



■ MUTING CIRCUIT

When Mute ON, OUTPUT level saturates to GND side.

Fig.3 BTL Configuration

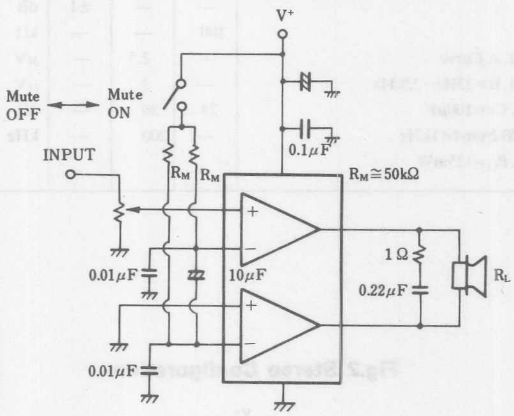
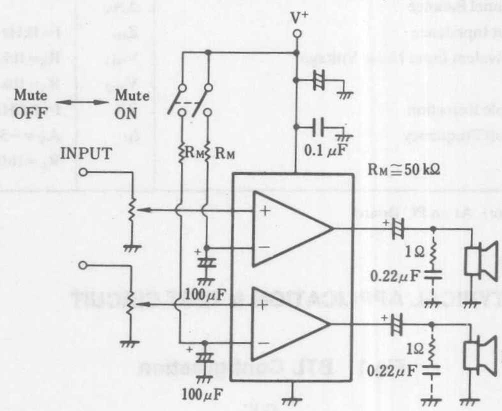


Fig.4 Stereo Configuration



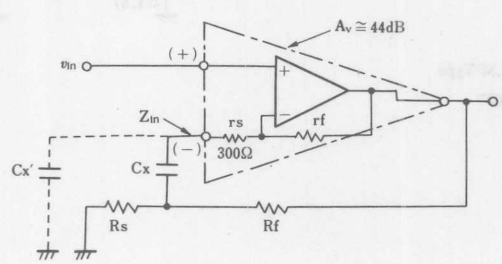
■ VOLTAGE GAIN REDUCTION APPLICATION EXAMPLE

(1) Outline of way to further Reduction

NJM2073 by taking in assamption, as one of OP-AMP (Gain 44dB, minus input impedance about 300Ω), to feedback from output to minus input helps to get reduction of stablized voltage Gain. Fig.5 indicates the model example.

Here is the point to be noticed that, in order to get the appropriate output Bias Voltage, it is important to keep the minus input floating as DC condition,(inserting C_X), and also that when extended too much reduction of Gain might cause Oscillation due to high band phase margin. The reduction of voltage gain is limitted at around 26 dB(20 times), and when oscillation, it in necessary to attach the oscillation atopper. Please examine the C_X value accordingly to the application reguirement.

Fig.5 Model of Voltage Gain Reduction



$$A_v = \frac{v_o}{v_{in}} \cong \frac{Rs+Rf}{Rs + \underset{(A_v)}{\frac{Rs+Rf}{160}} + \underset{(A_v)(Z_{in})}{\frac{Rs\times Rf}{160\times 300}}} \text{〔倍〕}$$

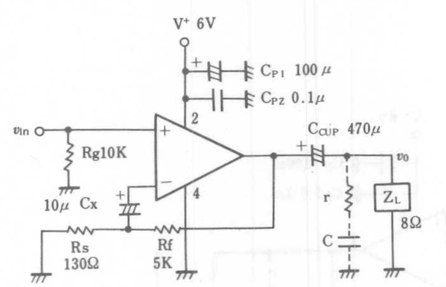
(2) The Application Example of Voltage Gain Reduction.(STEREO)

Fig.6 indicates the application example and Table 1 indicates the recommendable value of parts to be attached externally.

Table 1, Applicating purpose and Recommended Value of Externally parts to be attached.

EXTERNAL PARTS	APPLICATION PURPOSE	RECOMMENDED VALUE	REMARKS
R_g	Plus input to be grounded by fixed DC	Under about 100kΩ	Catch the noise when much higher.
R_s	AV shall be decided with R_f	—	
R_f	AV shall be decided with Rs	About 5kΩ	The co-temperature of AV becomes higher in case when Rs is higher resistance. The current from output pin to GND becomes higher, in case when Rs is lower resistance. (The current sinks in vain.)
C_X	Minus input to be grounded by fixed DC	—	Low-band Cut off frequency (fL) is to be decided. The rise time becomes longer in case that C_X is big.
C_{CUP}	Output DC Decoupling	When $R_L = 8\Omega$, More than $220\mu F$	fL shall be decided by C_{CUP} and Z_L.
C_{P1}	Stabilization of V^+	More than about C_{cup}	Inserting near around V^+ pin and GND pin.
C_{P2}	Prevention of Oscillation	More than $0.1\mu F$	
r	〃	About R_L	〃
C	〃	$0.22\mu F$	To be examined by about the resisitor volume of the speaker load.

Fig.6 STEREO Application Example.



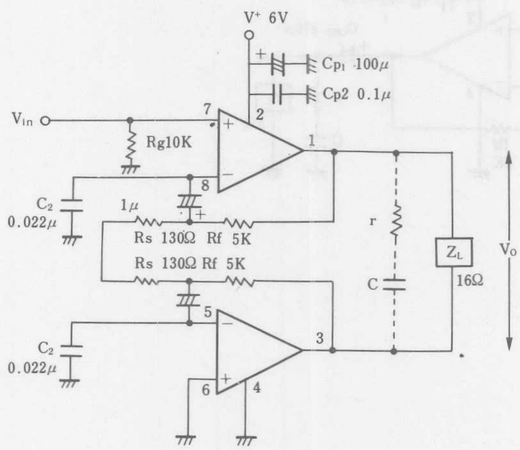
● Application for Voltage Gain Reduction (BTL)

Fig.7 indicates the application example, Table 2 shows recommended value of externally attaching parts.

Table 2 Applicating purpose and Recommended Value of External Part

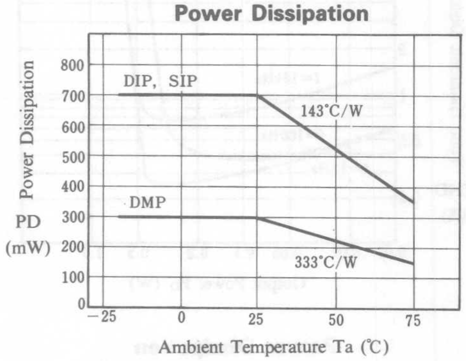
EXTERNAL PARTS	APPLICATION PURPOSE	RECOMMENDED VALUE	REMARKS
R_g	DC condition ground of plus input	Below about 10kΩ	Making noise when higher.
R_s	AV shall be decided with R_f		
R_f	AV shall be decided with R_s	About 5kΩ	Temperature feature to be increased accordingly as in higher AV value. When lower, to be trended of Oscillation.
C_1	Releasing minus input in to DC condition		Setting up low band Cut-off frequency (fL). More higher, the rise time become longer.
C_2	Preventing Oscillation	About 0.02μF	The more higher in ralue, the high band THD, due to phase slippling to be deteriorated. When lower, to be trended of oscillation.
C_{P1}	Stability of V^+ Preventing Oscillation	more than about 100μF	Inserting near around at V^+ and the GND pin.
C_{P2}	Preventing Oscillation	mote than 0.1μF	〃
r	〃	About R_L	To be examined at around pure resister Value of speaker load.
C	〃	0.22μF	

Fig.7 BTL Application

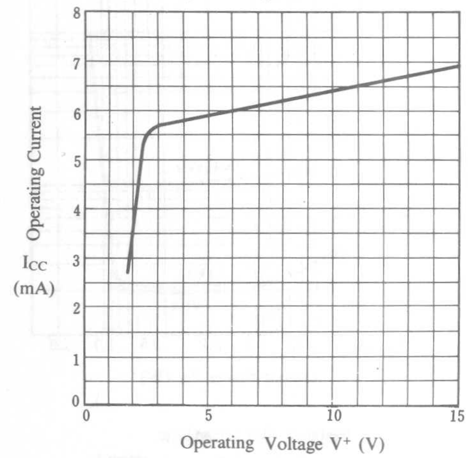


■ TYPICAL CHARACTERISTICS

Power Dissipation

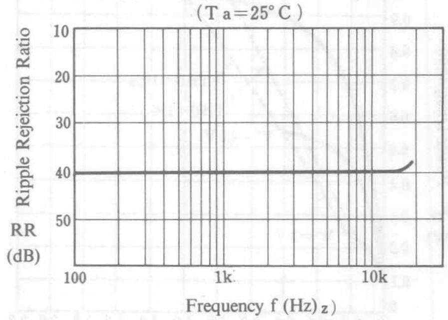


Operating Current



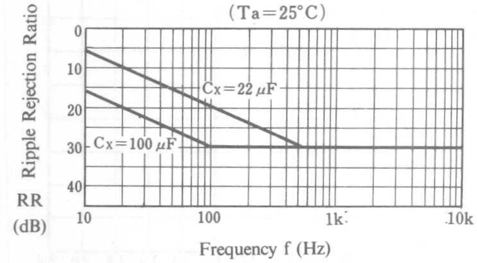
Ripple Rejection Ratio (BTL)

(Ta=25°C)



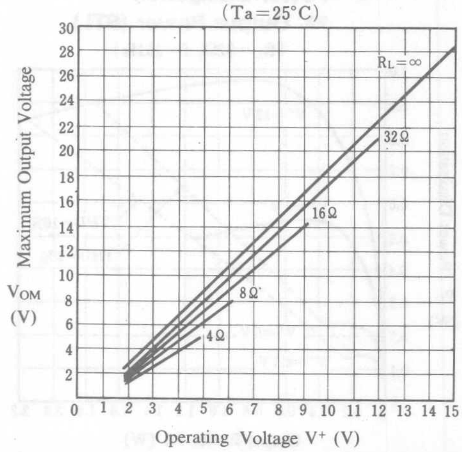
Ripple Rejection Ratio (Stereo)

(Ta=25°C)



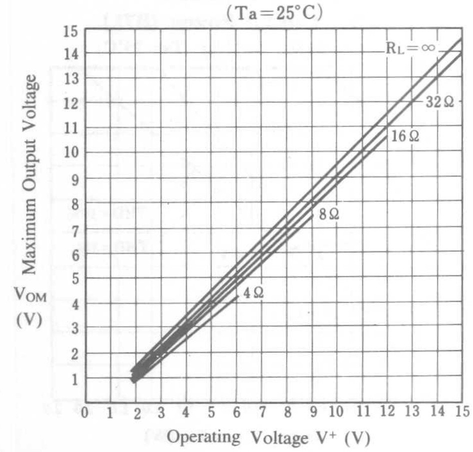
Maximum Output Voltage (BTL)

(Ta=25°C)



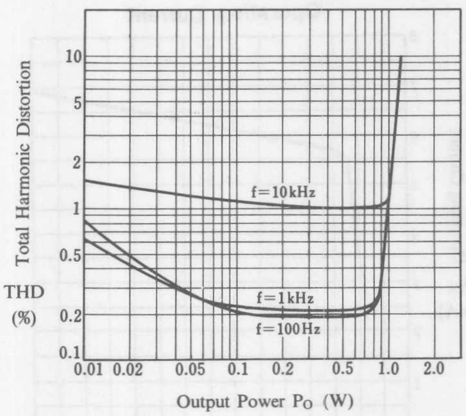
Maximum Output Voltage (Stereo)

(Ta=25°C)

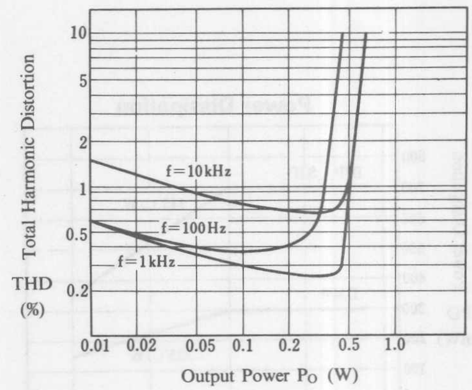


■ **TYPICAL CHARACTERISTICS**

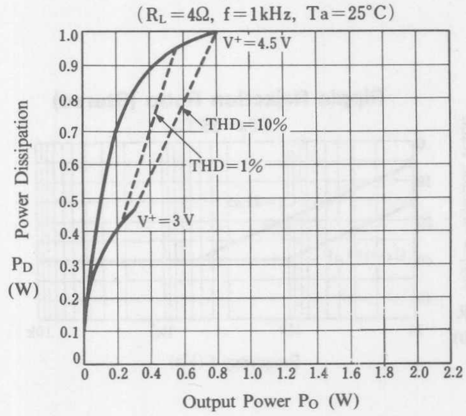
Total Harmonic Distortion (BTL)
($V^+=6V$, $R_L=8\Omega$)



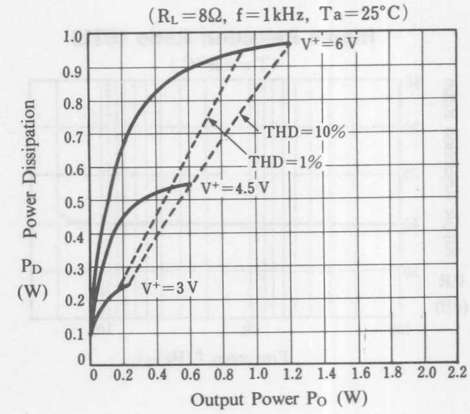
Total Harmonic Distortion (Stereo)
($V^+=6V$, $R_L=4\Omega$)



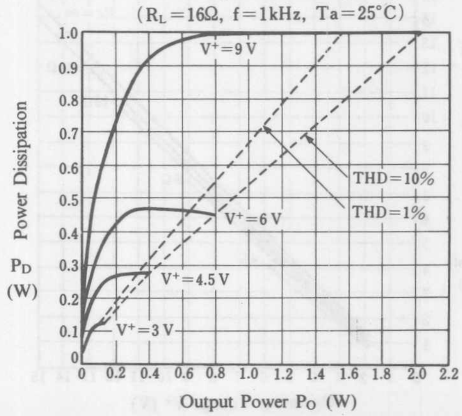
Power Dissipation vs. Output Power (BTL)
($R_L=4\Omega$, f=1kHz, Ta=25°C)



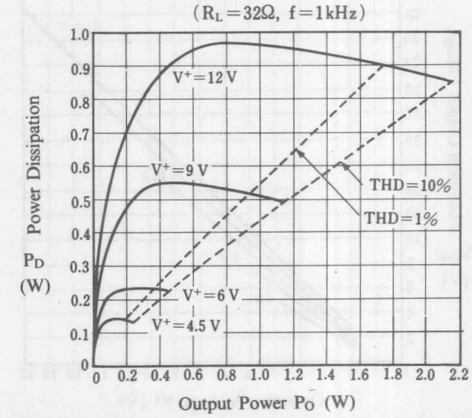
Power Dissipation vs. Output Power (BTL)
($R_L=8\Omega$, f=1kHz, Ta=25°C)



Power Dissipation vs. Output Power (BTL)
($R_L=16\Omega$, f=1kHz, Ta=25°C)



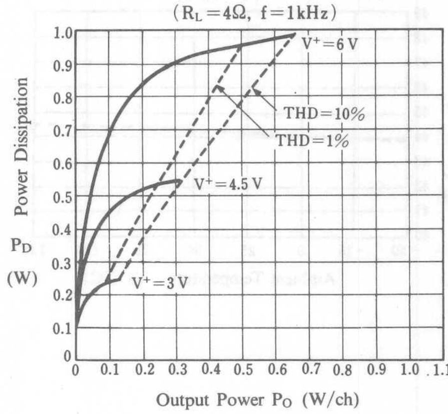
Power Dissipation vs. Output Power (BTL)
($R_L=32\Omega$, f=1kHz)



■ TYPICAL CHARACTERISTICS

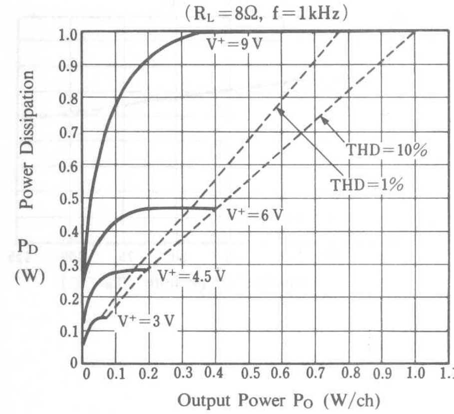
Power Dissipation vs. Output Power (Stereo)

($R_L=4\Omega$, f=1kHz)



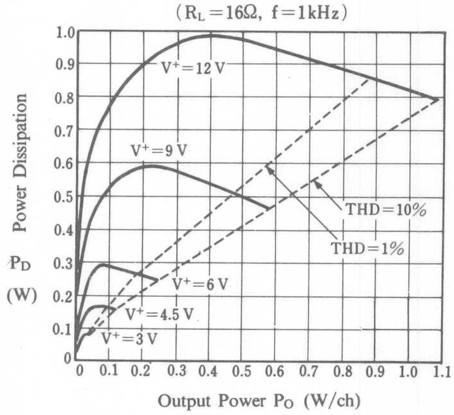
Power Dissipation vs. Output Power (Stereo)

($R_L=8\Omega$, f=1kHz)



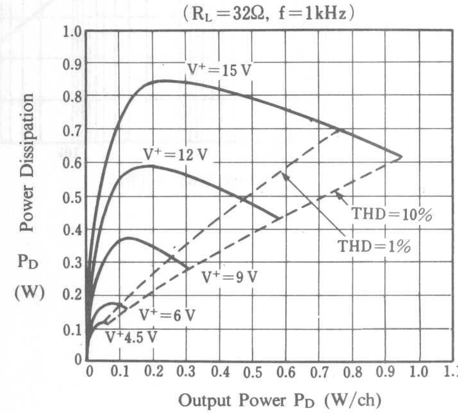
Power Dissipation vs. Output Power (Stereo)

($R_L=16\Omega$, f=1kHz)

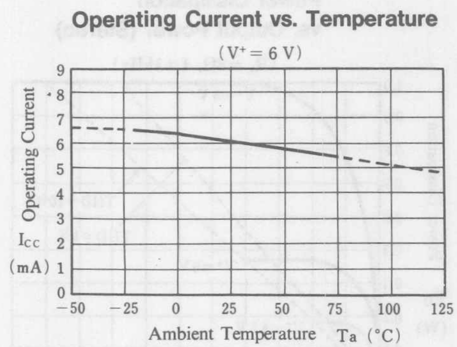


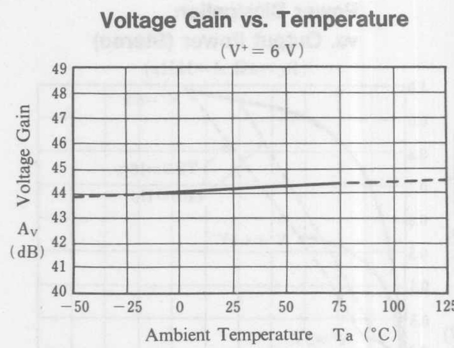
Power Dissipation vs. Output Power (Stereo)

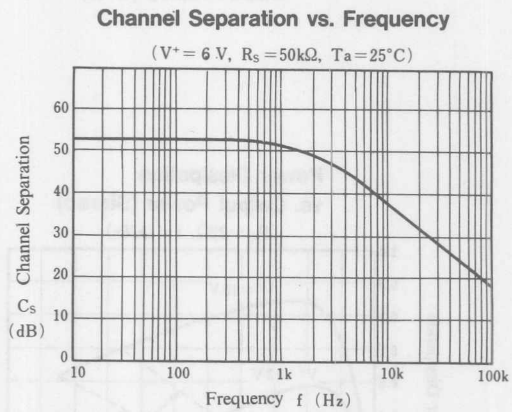
($R_L=32\Omega$, f=1kHz)



■ TYPICAL CHARACTERISTICS





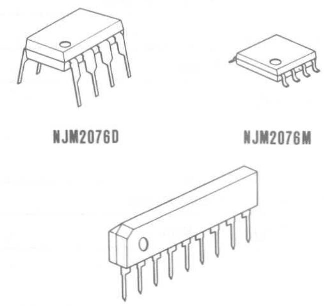


DUAL LOW VOLTAGE POWER AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2076 is a dual power amplifier, which operates with 1.0V minimum supply voltage. The NJM2076 is suitable to small radio and head-phone of stereo and single BTL application.

■ PACKAGE OUTLINE



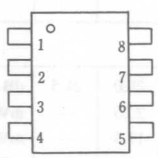
NJM2076D NJM2076M

NJM2076S

■ FEATURES

- BTL operation P_O=90mW type.
- Minimum external components
- Headphone stereo Amp. with external transistors
- Low Operation Voltage (1.0V MIN.)
- Low Operating Current (4.7mA TYP.)
- Package Outline DIP8, DMP8, SIP9
- Bipolar Technology

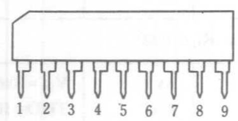
■ PIN CONFIGURATION



NJM2076D
NJM2076M

PIN FUNCTION

1. Inverting Amp. Input (A)
2. Non-Inverting Amp. Input(B)
3. V+
4. Base(B)
5. (B) Output
6. GND
7. (A) Output
8. Base (A)



NJM2076S

PIN FUNCTION

1. V+
2. Base (B)
3. (B) Output
4. Power GND
5. GND
6. (A) Output
7. Base (A)
8. Inverting Amp Input (A)
9. Non-Inverting Amp Input (B)

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	4.5	V
Maximum Input Signal	V_{IN}	200	mVrms
Power Dissipation	P_D	(DIP 8) 500	mW
		(SIP 9) 500	mW
		(DMP 8) 500	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

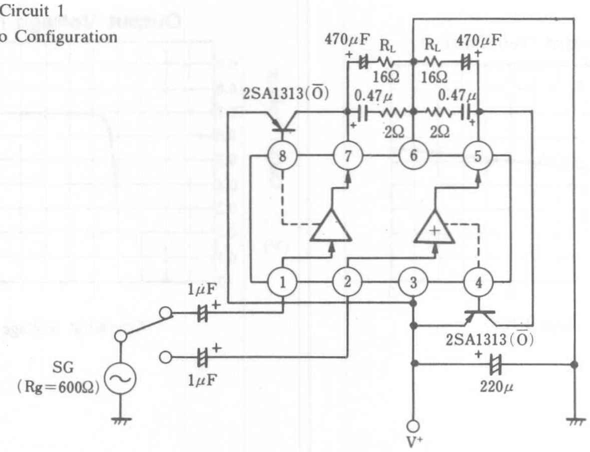
■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V^+=1.5V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{cc}	Input: Open	—	4.7	7.0	mA
(I) Stereo Configuration (Test Circuit 1. R_L=16Ω)						
Voltage Gain	Av	V_{IN}=10mVrms	26.5	28.0	29.5	dB
Max. Output Power	P_{O1}	THD=10%(S-Type)	15	20.0	—	mW
		THD=10%(D, M-Type)	15	17.5	—	mW
	P_{O2}	THD=10%, V^+=1.0V	—	3	—	mW
Total Harmonic Distortion	THD_1	P_O=1mW (126mVrms/16Ω)	—	0.4	0.8	%
Output Noise Voltage	V_{NO1}	Rg=0, A Curve	—	50	150	μV
Ripple Rejection Ratio	RR_1	Rg=0.f_R=1kHz, V_R=30mvrms	25	35	—	dB
Input Resistance	R_{IN}		25	33	43	kΩ
Output Pin Voltage	V_O (DC)		0.62	0.70	0.77	V
(II) BTL Configuration (Test Circuit 2. R_L=8Ω)						
Max. Output power	P_{O3}	THD=10% (S-Type)	75	100	—	mW
		THD=10% (D,M-Type)	75	90	—	mW
	P_{O4}	THD=10%, V^+=1.0V (S-Type)	—	30	—	mW
		THD=10%. V^+=1.0V(D, M-Type)	—	20	—	mW
Total Harmonic Distortion	THD_2	P_O=10mW(283mVrms/8Ω	—	1.5	4.5	%
Output Noise Voltage	V_{NO2}	Rg=0, A Curve	—	85	250	μV
Ripple Rejection Ratio	RR_2	Rg=0, f_R=1kHz, V_R=30mVrms	20	25	—	dB
Voltage Difference between Two Output Pins	ΔV_O(DC)		—	—	50	mV

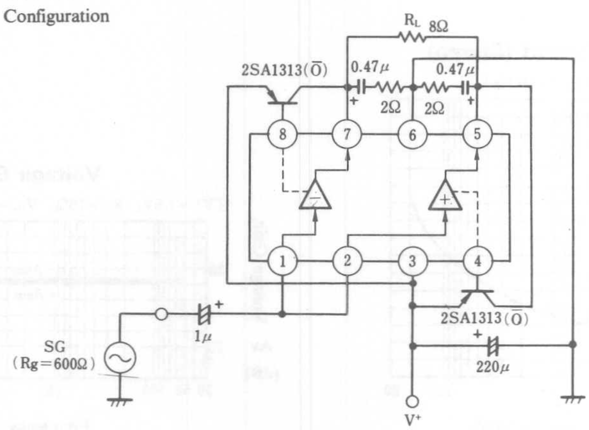
■ TEST CIRCUIT

Test Circuit 1
Stereo Configuration



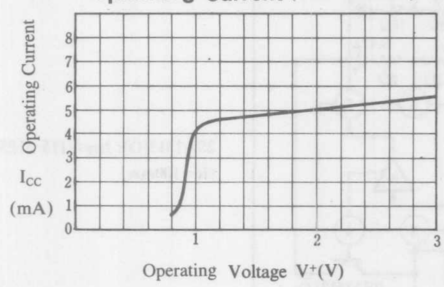
2SA1313(Ō): h_{FF}=115~125
(Ic=100mA)

Test Circuit 2
BTL Configuration

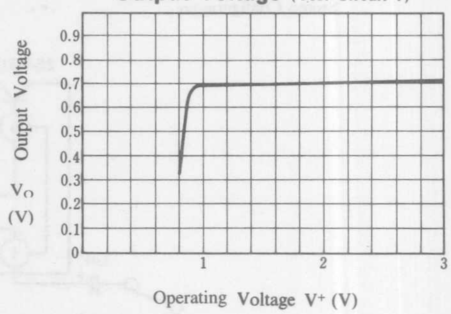


■ TYPICAL CHARACTERISTICS

Operating Current (Test Circuit 1)

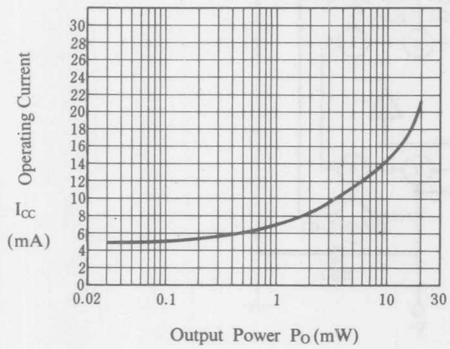


Output Voltage (Test Circuit 1)



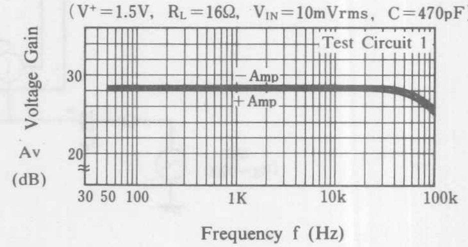
Operating Current (Stereo)

(V^+=1.5V, f=1kHz)



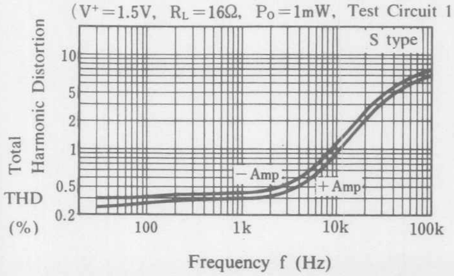
Voltage Gain

(V^+=1.5V, R_L=16Ω, V_{IN}=10mVrms, C=470pF)



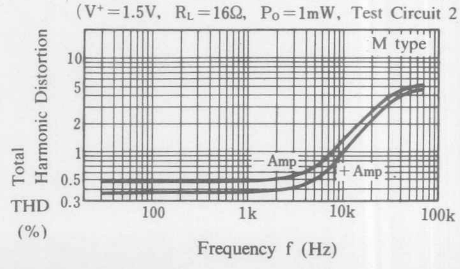
Total Harmonic Distortion (Stereo)

(V^+=1.5V, R_L=16Ω, P_O=1mW, Test Circuit 1)



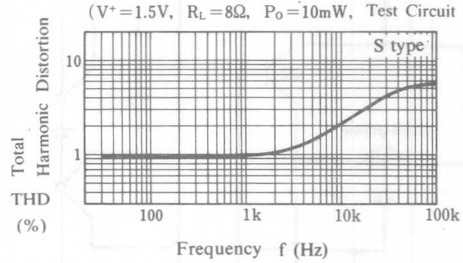
Total Harmonic Distortion (Stereo)

(V^+=1.5V, R_L=16Ω, P_O=1mW, Test Circuit 2)

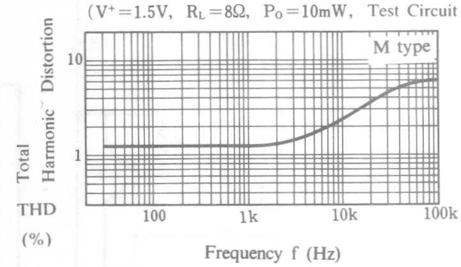


■ TYPICAL CHARACTERISTICS

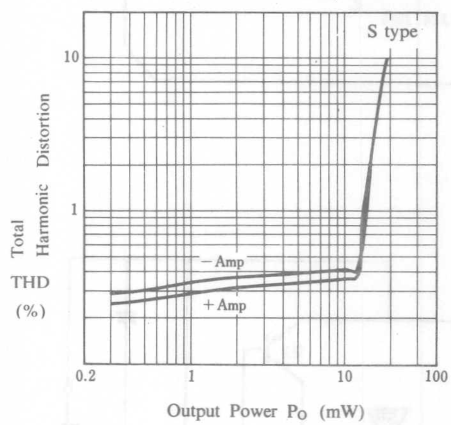
Total Harmonic Distortion (BTL)
(V^+=1.5V, R_L=8Ω, P_O=10mW, Test Circuit 2)



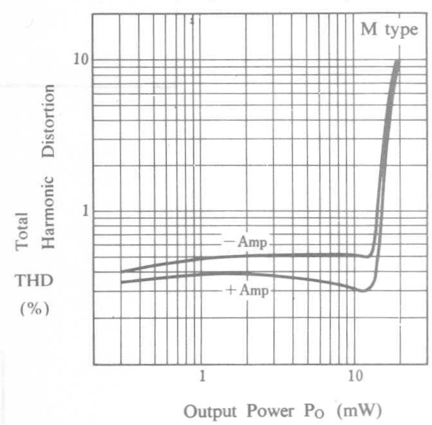
Total Harmonic Distortion (BTL)
(V^+=1.5V, R_L=8Ω, P_O=10mW, Test Circuit 2)



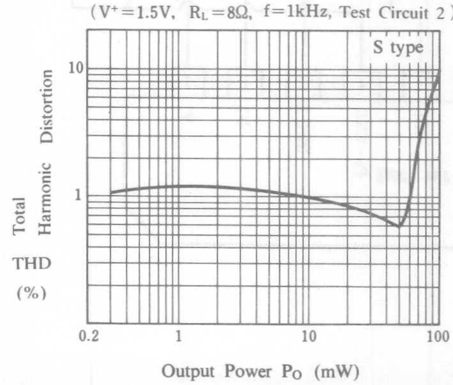
Total Harmonic Distortion (Stereo)
(V^+=1.5V, R_L=16Ω, f=1kHz, Test Circuit 1)



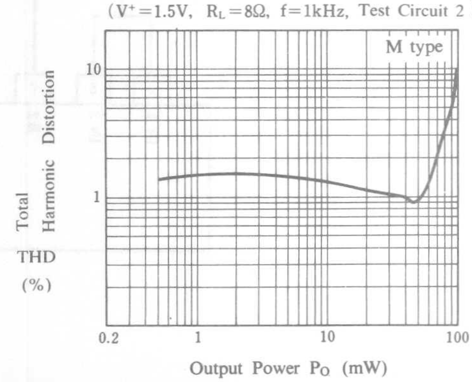
Total Harmonic Distortion (Stereo)
(V^+=1.5V, R_L=16Ω, f=1kHz, Test Circuit 1)



Total Harmonic Distortion (BTL)
(V^+=1.5V, R_L=8Ω, f=1kHz, Test Circuit 2)

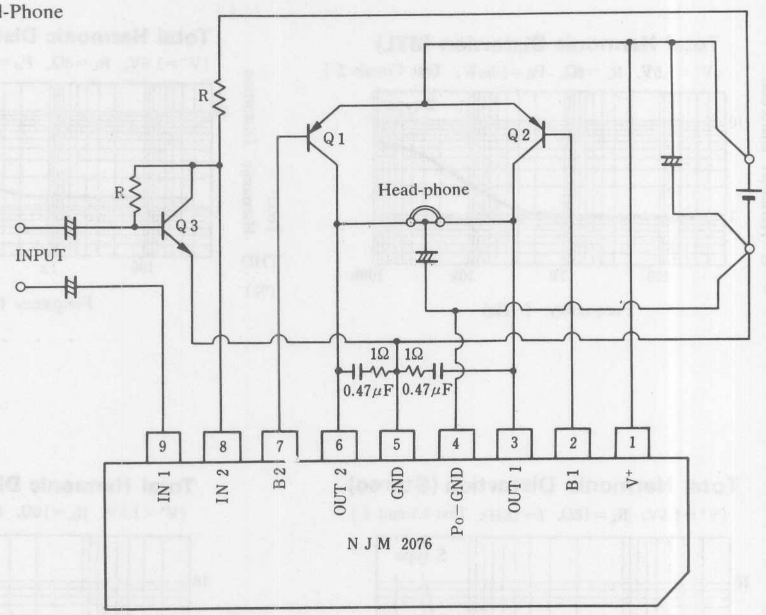


Total Harmonic Distortion (BTL)
(V^+=1.5V, R_L=8Ω, f=1kHz, Test Circuit 2)

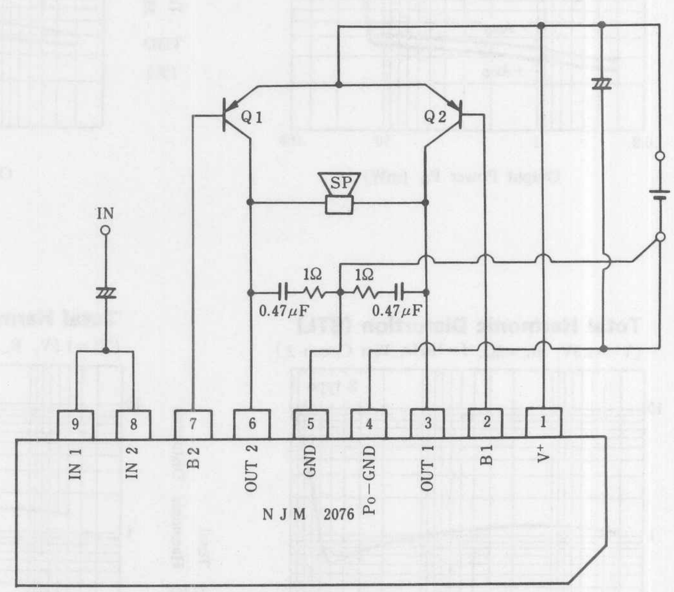


■ TYPICAL APPLICATION

1. For Stereo Head-Phone



2. BTL Amp. for Speaker



■ NOTICE

(1) External PNP Transistor

Maximum output power becomes large with low saturation voltage transistor, and so select transistor of low saturation.

Saturation Voltage: less than 0.1V (I_C=100mA. I_B=10mA). h_{FE}: 120

(2) External Frequency Compensation

Recommend tantalum capacitor with low tanδ (less than 0.25 at f=10kHz) and 1Ω resistor. Stable with large capacitor of less high frequency distortion and worse tanδ. For example: 1μF, tanδ ≦ 0.6

(3) Layout on PCB

Be careful to get maximum output power and low distortion set.

DIP/DMP: Signal ground has to be close to IC ground pin. Impedance of ground line must be low.

SIP: Two terminals (Power GND, GND) are connected at one point on PCB.

■ GENERAL DESCRIPTION

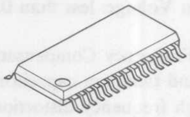
The NJM2085 is a monolithic BiCMOS IC designed for use in the car stereo cassette player system. The audio signal system for cassette player can be realized very easy, as the device includes two channel low noise preamplifiers. Dolby B type noise reduction decorders and an audiomusic sensor.

(note) Dolby and the double-D symbol are trade marks of Dolby Labolatories Licensing Corporation San Francisco. CA94103-4813, USA.

This device available only to licensees of Dolby Lab.

Licensing and application information may be obtained from Dolby Lab.

■ PACKAGE OUTLINE



NJM2085M

■ FEATURES

- Operating Voltage (8～10.5V)
- The dual preamplifier contains mute, auto-reverse matel/norm, facilities for application of low level signal in applications requring very low noise performances. Each channel consisits of a 36dB fixed gain amplifier, having switchable input for forward/reverse, allows magnetic heads connection directry to ground and operational amplifier for switching the external eqalizing networks.
- The audio music sensor detects the interprogram space and then the starting point of musical program.
- Dolby B Type Noise Reduction Decorders require few external components.
- Package Outline SDMP30
- Bipolar Technology

■ FUNCTIONS

- Low noise head preamplifiers
- Mute and auto-reverse functions
- Internal switches for equalization
- 2 channel Dolby B Type Noise Reduction Decoders
- Audio music sensor

■ ABSOLUTE MAXIMUM RATINGS AT TA=25℃

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	12	V
Total Power Dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	−40～+85	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, all levels reference to −6dBm/400Hz at DOLBY OUT NR OFF, Unless otherwise specified.)

□SUPPLY

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage Range	V_{OP}		8	8.5	10.5	V
Operating Current	I_S		—	18	25	mA
Reference Voltage	V_{ref}		4.0	4.3	4.6	V
DC Voltage Pin 14	V_{dc}		1.15	1.25	1.35	V
MUTE ON LEVEL	MUTE ON		0	—	1.2	V
MUTE OFF LEVEL	MUTE OFF		2.2	—	V^+	V
MUTE	ATT		55	65	—	dB
MUTE Current	IMUTE		—	10	—	μA

□PREAMPLIFIER

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Resistance	R_i		30	50	70	kΩ
Input Bias Current	I_i		—	—	10	μA
Voltage Gain	G_V	pin4～5 and 26～27 shorted	32.5	35.5	38.5	dB
Voltage Gain Matching	ΔG_V		−1	—	1	dB
Resistor Metal Position	R_m		4.35	5.8	7.25	kΩ
Resistor Normal Position	R_n		—	150	400	kΩ
Total Input Noise	en 1	Rg=600Ω B=20−20kHz	—	0.8	—	μV
	en 2	Rg=600Ω, A-Weight	—	0.5	—	
Forward/Rev. Low Level	FRL	IN 2=ON; IN 1=OFF	0	—	0.8	V
Forward/Rev. High Level	FRH	IN 2=OFF; IN 1=ON	2	—	V^+	V
Metal/Normal Low Level	NML	EQSW=ON	0	—	1.5	V
Metal/Normal High Level	NMH	EQSW=OFF	3.5	—	V^+	V
Output Impedance	R_O		—	1.2	1.7	Ω

□AUDIO MUSIC SENSOR

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Low Level Voltage	Vl		—	—	800	mV
Input Current	I_{in}		—	—	1	μA
ON/OFF Low level	AMSL		—	—	0.8	V
ON/OFF High Level	ANSH		2	—	V^+	V
Interprogram Threshold Voltage	VTH 1		1.2	1.45	1.7	V
Interspace Threshold Voltage	VTH 2		4.0	4.3	4.6	V
AMS Threshold	AMSVTH 1		1.19	1.39	1.59	V
	AMSVTH 2		0.6	0.8	1.0	V
Switch Pin Current	Vol		—	18	—	μA

□ DOLBY SECTION

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
		NR	f(Hz)	OTHER CONDITIONS				
Voltage Gain	G_V	OFF	1K		−1	0	1	dB
Channel Matching	ΔG_V	OFF	1K		−0.5	—	0.5	dB
Signal Handling	S/H	ON	1K	V_{CC}=8V, THD=1%	12	13	—	dB
Decode Cut	B-DEC1	ON	10K	Vout=0dB	−1.1	0.4	1.9	dB
	B-DEC2	ON	500	Vout=−25dB	1.4	2.9	4.4	dB
$20\log\frac{\text{Vout (off)}}{\text{Vout (on)}}$	B-DEC3	ON	2K	Vout=−25dB	5.5	7.0	8.5	dB
	B-DEC4	ON	5K	Vout=−25dB	3.9	5.4	6.9	dB
	B-DEC5	ON	10K	Vout=−40dB	8.9	10.4	11.9	dB
ON/OFF Low Level	NRoff				0	—	0.8	V
ON/OFF Hight Level	NRon				2.0	—	V^+	V

□ GENERAL

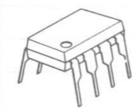
PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
		NR	f(Hz)	OTHER CONDITIONS				
Total Harmonics Distortion	THD1	OFF	1K	V_O=0dB	—	0.12	—	%
	THD2	ON	1K	V_O=0dB	—	0.08	—	%
	THD3	OFF	10K	V_O=0dB	—	0.18	—	%
	THD4	ON	10K	V_O=0dB	—	0.2	—	%
Signal to Noise Ratio	S/N1	OFF		Rg=600Ω, V_O=0dB	—	60	—	dB
	S/N2	ON		CCIR/ARM	—	70	—	dB
Channel Separation	CS1	OFF	1K	Rg=600Ω	—	55	—	dB
	CS2	ON	1K	Rg=600Ω	—	60	—	dB
Channel Cross Talk	CT1	OFF	1K	Rg=600Ω	—	58	—	dB
	CT2	ON	1K	R_g=600Ω	—	67	—	dB
Supply Voltage Rejection	SVR1	OFF	1K	Rg=600Ω	—	90	—	dB
	SVR2	ON	1K	Rg=600Ω	—	95	—	dB

LOW VOLTAGE DUAL POWER AMPLIFIER

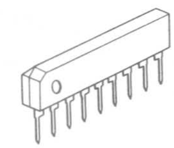
■ GENERAL DESCRIPTION

The NJM2096 is a dual power amplifier, which operates with 1.0V minimum supply voltage. The NJM2096 is suitable to small radio and head-phone stereo. The NJM2096 is resemble to the NJM2076, but two amplifiers are the same.

■ PACKAGE OUTLINE



NJM 2096 D



NJM 2096 S

NJM 2096 M

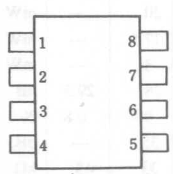
■ FEATURES

- Low Operating Voltage (1.0V min)
- Minimum external components
- Low Operating Current
- Package Outline DIP8, DMP8, SIP9
- Bipolar Technology

■ APPLICATION

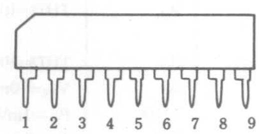
- Head-phone Stereo, Portable Radio, Portable TV, Hand-carry Tele-communication Set.

■ PIN CONFIGURATION



NJM2096D
NJM2096M

PIN FUNCTION
1. Non-Inverting Amp. Input (A)
2. Non-Inverting Amp. Input (B)
3. V^+
4. Base (B)
5. (B) Output
6. GND
7. (A) Output
8. Base (A)



NJM2096S

PIN FUNCTION
1. V^+
2. Base (B)
3. (B) Output
4. Power GND
5. GND
6. (A) Output
7. Base (A)
8. Non-Inverting Amp. Input (A)
9. Non-Inverting Amp. Input (B)

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

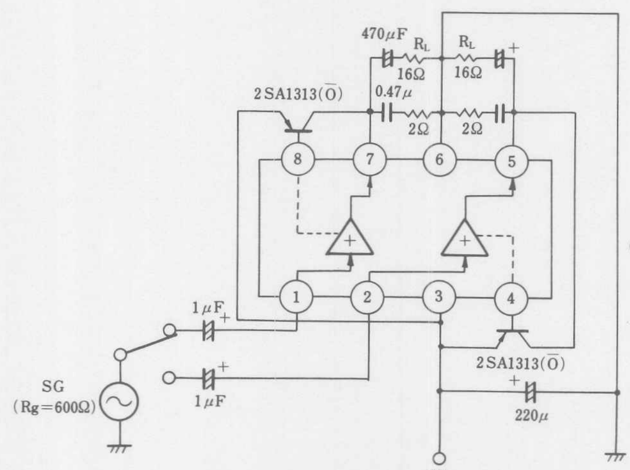
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	4.5	V
Power Dissipation	P_D	(DIP8) 500	mW
		(SIP9) 500	mW
		(DMP8) 300	mW
Maximum Input Signal	V_{IN}	200	mVrms
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V^+=1.5V. R_L=16Ω)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{cc}	V_{IN}=Open	—	4.7	7	mA
Maximum Output Power	P_{OI}	THD=10% D&S	15	20	—	mW
		M	15	17.5	—	mW
Max. Output Power at Low Supply Voltage	P_O	THD=10%, V^+= 1.0V		3	—	mW
Voltage Gain	Av	V_{IN}=10mVrms	26.5	28	29.5	dB
Total Harmonic Distortion	THD	P_O=1mW		0.4	0.8	%
Ripple Rejection Ratio	RR	Rg=0Ω, V_r =30mVrms. F_r =1kHz	25	35	—	dB
Input Resistance	R_{IN}		25	33	43	kΩ
Output Noise Voltage	V_{NO}	Rg=0Ω, A Curve	—	40	150	μV
Output Pin Voltage	V_O (DC)		0.62	0.70	0.77	V
Voltage Difference between Two Output Pins	ΔV_O (DC)		—	—	50	mV

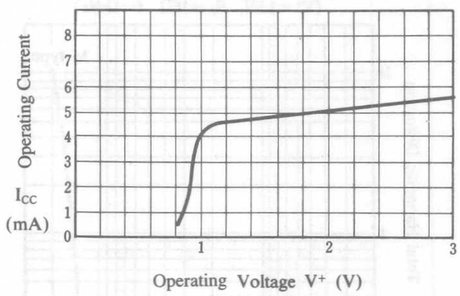
■ TEST CIRCUIT



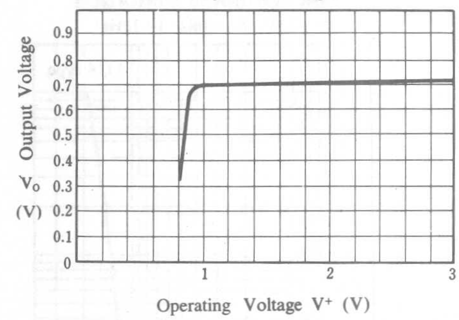
2SA1313 (Ō) : h_{FE}=115～125
(I_C=100mA)

■ TYPICAL CHARACTERISTICS

Operating Current

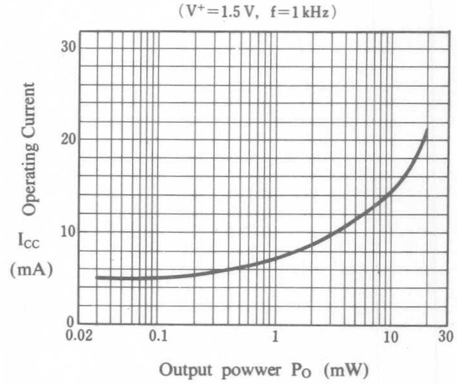


Output Voltage



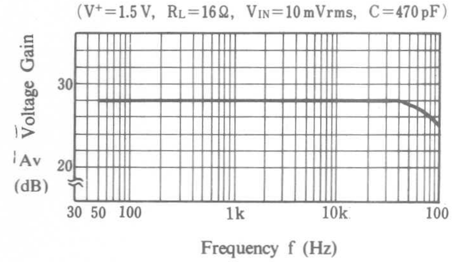
Operating Current

(V^+=1.5 V, f=1 kHz)



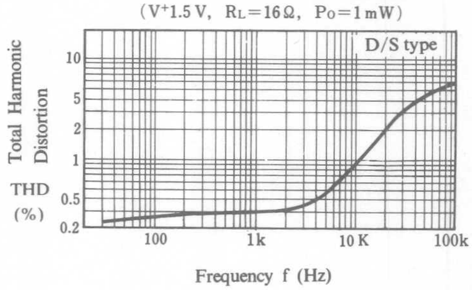
Voltage Gain

(V^+=1.5 V, R_L=16 Ω, V_{IN}=10 mVrms, C=470 pF)



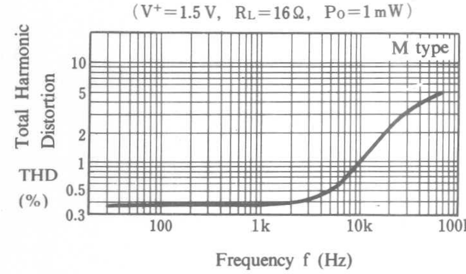
Total Harmonic Distortion

(V^+1.5 V, R_L=16 Ω, P_O=1 mW)

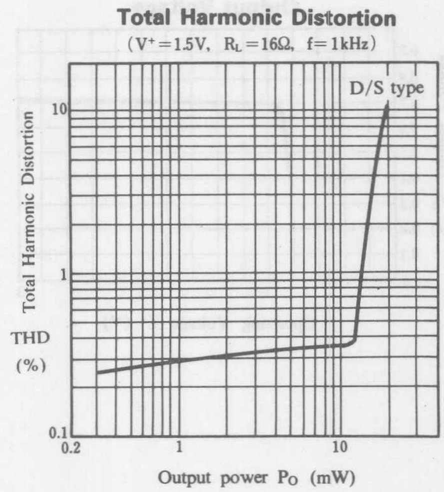


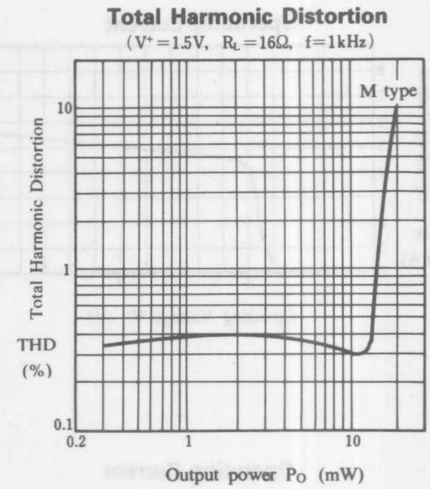
Total Harmonic Distortion

(V^+=1.5 V, R_L=16 Ω, P_O=1 mW)



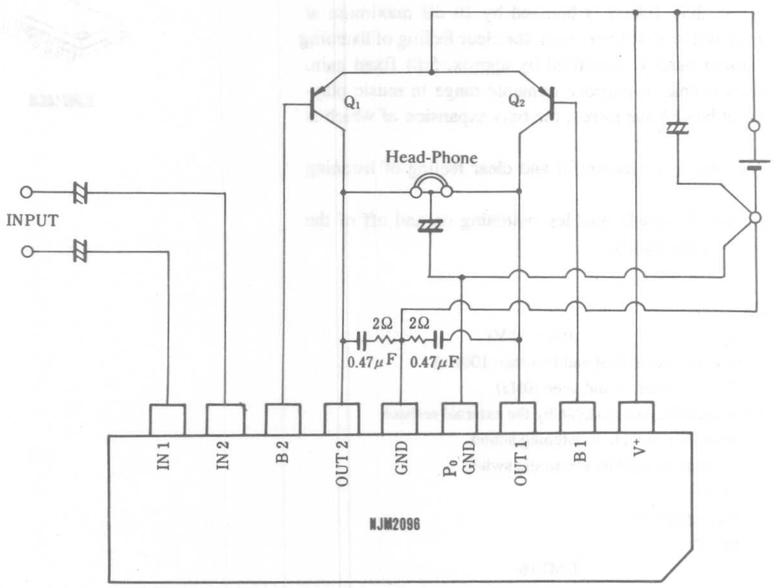
■ TYPICAL CHARACTERISTICS





■ TYPICAL APPLICATION

Stereo Head-Phone



■ NOTICE

(1) External PNP Transistor

Maximum output power becomes large with low saturation voltage transistor, and so select transistor of low saturation voltage.

h_{FF}: 120

(2) External Frequency Compensation

Recommend tantalum capacitor with low tan δ (less than 0.25 at f=10kHz) and 2Ω resistor. Stable with large capacitor of less high frequency distortion and worse tanδ. For example: 1μF. tanδ≦0.6

(3) Layout on PCB

Be careful to get maximum output power and low distortion set.

DIP/DMP: Signal ground has to be close to IC ground pin. Impedance of ground line must be low.

SIP: Two terminals (Power GND, GND)are connected at one point on PCB.

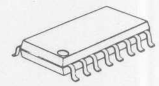
■ GENERAL DESCRIPTION

NJM2106 is the active bass expander to be specifically used in the headphone type stereo operating at 1.5V power supply (standard). The low sound band less than 100Hz is boosted by 20 dB maximum at medium level input and at low level input, the clear feeling of listening sound, the high sound band is amplified by approx. 5dB fixed gain. These performances enable to improve dynamic range in music play-back by the compact headphone stereo, the bass expansion of which is not good enough.

Thus the IC enables to get powerful and clear feeling of listening sound.

The electronic switch simply enables switching on and off of the boost, circuit, and the mute circuit.

■ PACKAGE OUTLINE

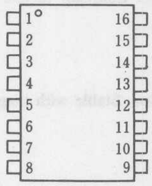


NJM2106M

■ FEATURES

- Operating Voltage (0.9～2.5V)
- Boost Value: 20dB max. (variavle at and less than 100Hz)
  50dB (fixed at and over 10Hz)
- Boost value in low sound band adjustable by the external resistor
- Internal mute circuit with a low click swtching sound
- On & Off boost and mute circuits by electronic switch
- Low power dissipation
- Minimum external components
- Low Operating Current
- Package Outline DMP16
- Bipolar Technology

■ PIN CONFIGURATION

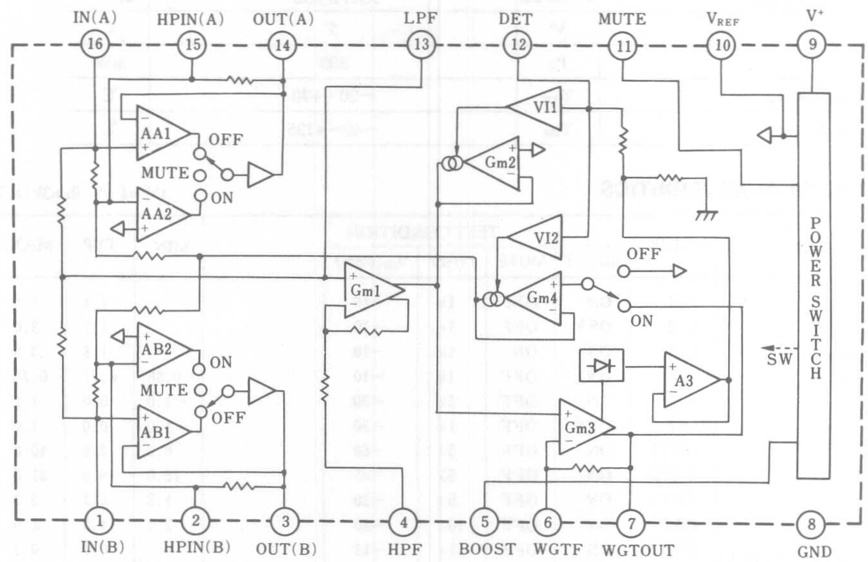


NJM2106M

PIN FUNCTION

1. Signal Input (B)	9 . Supply Voltage
2. High Band Signal Input (B)	10. Reference Voltage
3. Signal Output (B)	11. Mute Control
4. HPF	12. DET
5. Boost Control	13. LPF
6. WGTF	14. Signal Output (A)
7. Boost Signal Output	15. High Band Signal Input (A)
8. GND	16. Signal Input (A)

■ **BLOCK DIAGRAM**



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	5	V
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	−20～+70	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=1.1V, R_L=3kΩ, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION					MIN.	TYP.	MAX.	UNIT
		BOOST	MUTE	f (Hz)	V_{IN} (dBm)					
Operating Current 1	$I_{CC}1$	ON	OFF	1k	−10		−	2.1	3.5	mA
Operating Current 2(Note 1)	$I_{CC}2$	OFF	OFF	1k	−10		−	1.7	3.0	mA
Operating Current 3 (Note 1)	$I_{CC}3$	ON	ON	1k	−10		−	1.8	3.5	mA
Reference Voltage (Note 1)	V_{REF}	ON	OFF	1k	−10		0.66	0.71	0.76	V
Voltage Gain 1	G_V1	ON	OFF	1k	−30		−1.0	0.0	1.0	dB
Voltage Gain 2	G_V2	OFF	OFF	1k	−30		−1.0	0.0	1.0	dB
Boost Value 1	BST1	ON	OFF	50	−60		0.0	2.6	10.0	dB
Boost Value 2	BST2	ON	OFF	50	−45		15.0	18.0	21.0	dB
Boost Value 3	BST3	ON	OFF	50	−20		1.3	3.3	5.3	dB
Boost Value 4	BST4	ON	OFF	10k	−20		2.5	4.5	6.5	dB
Total Harmonic Distortion 1 (Note 1)	THD1	ON	OFF	1k	−18		−	0.1	0.6	%
Total Harmonic Distortion 2	THD2	OFF	OFF	1k	−18		−	0.1	0.6	%
Ripple Rejection Ratio	RR	ON	OFF	Ripple (400Hz, −40dBm) is applied on V^+			40.0	43.5	−	dB
Output Noise Voltage (Note 1)	V_{NO}	OFF	OFF	20-20kHz BPF, R_G=600Ω			−	2.7	4.0	μV
Mute Attenuation 1	MAT1	ON	ON	50	−20		43.0	50.0	−	dB
Mute Attenuation 2 (Note 1)	MAT2	OFF	ON	50	−20		43.0	59.0	−	dB
Boost On Sensitivity (Note 2)	V_{BON}	ON	OFF	50	−45			Open		
Boost Off Sensitivity Voltage (Note 3)	V_{BOFF}	ON	OFF	50	−45		0.0	−	0.2	V
Boost Off Sensitivity Current	I_{BOFF}	ON	OFF	50	−45	⑤ Pin=0V	−	12.0	30.0	μA
Mute On Sensitivity Voltage (Note 4)	V_{MON}	ON	ON	50	−20		0.0	−	0.2	V
Mute On Sensitivity Current	I_{MON}	ON	ON	50	−20	⑪Pin=0V	−	12.0	30.0	μA
Mute Off Sensitivity (Note 5)	V_{MOFF}	ON	ON	50	−20			Open		
Crosstalk (Note 1)	CT	ON	OFF	1k	−20		−	−27.0	−22.0	dB

(Note 1): These parameters are guaranteed by design. The testing during the productions are not to be conducted.

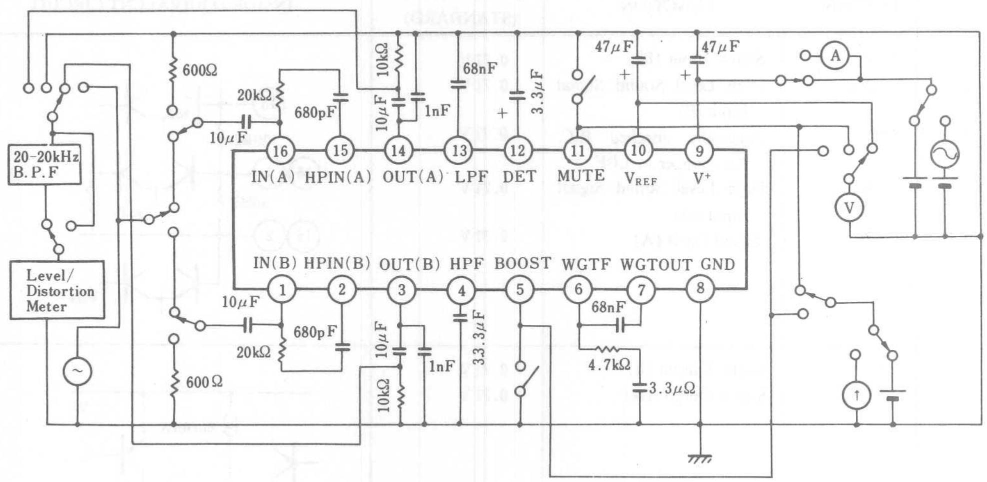
(Note 2): Recommendable (5) pin to be left open, under Boost on state.

(Note 3): Recommendable (5) pin on GND under Boost off state. In case of applying voltage, recommendable to be conducted within the range of the standard value.

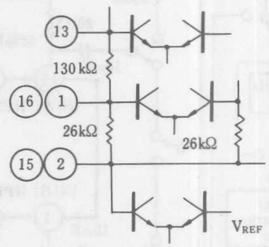
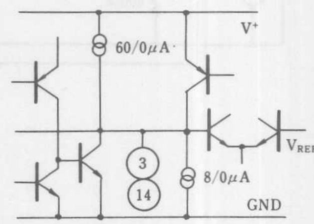
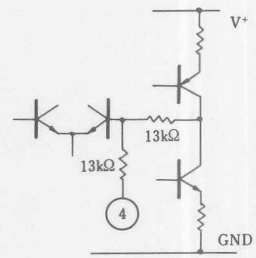
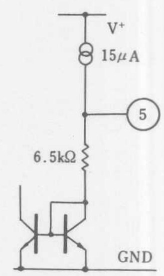
(Note 4): Recommendable (11) pin on GND under Mute on state. In case of applying voltage, to be conducted within the range of the standard value.

(Note 5): Recommendable (11) pin to be left open under Mute Off state. At this time, when operating IC with the current running, there might be cases of making oscillations.

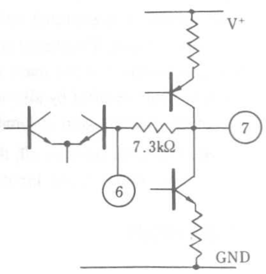
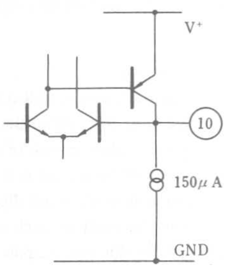
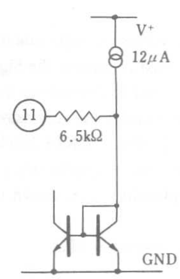
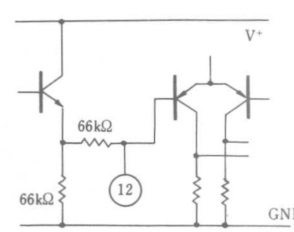
■ TEST CIRCUIT



■ TERMINAL DESCRIPTION

PIN NO.	PIN SYNBOL	FUNCTION	PIN VOLTAGE (STANDARD)	INSIDE EQUIVALENT CIRCUIT
1 2 13 15 16	IN (B) HPIN (B) LPF HPIN (A) IN (A)	Signal Input (B) High Level Sound Signal Input (B) Externally attached R.C. Pin number at LPF High Level Sound Signal Input (A) Signal Input (A)	0.71 V 0.71 V 0.71 V 0.71 V 0.71 V	
3 14	OUT (B) OUT (A)	Signal Output (B) Signal Output (A)	0.71 V 0.71 V	
4	HPF	Externally attached R.C. pin number at HPF. Adjustment of Boost Value.	0.71 V	
5	BOOST	On/Off Switch of Boost Circuit. Open: On GND: Off	ON State 0.75 V	

■ TERMINAL DESCRIPTION

PIN NO.	PIN SYNBOL	FUNCTION	PIN VOLTAGE (STANDARD)	INSIDE EQUIVALENT CIRCUIT
6	WGTF	Externally attached R.C. Pin number of weighting filter Amp.	0.71 V	
7	WGTOUT	Boost Signal Output	0.71 V	
10	V_{REF}	Reference Voltage	0.71 V	
11	MUTE	On/Off Switch of Mute Circuit Open: Off GND: On	Off State 0.65 V	
12	DET	Control Voltage Output Pin		

■ PRINCIPLE OF OPERATION

NJM2106 is consists of the circuit of high sound band amplifier, low sound band amplifier, the circuit to add amplifired signals on the main signal, and the mute which shuts off the signal.

Higher sound band element: It is supplied to 2 and 15 pins after passing through external R &C. This signal plus main signal input in 1 and 16 pins is output from 3 and 14 pins.

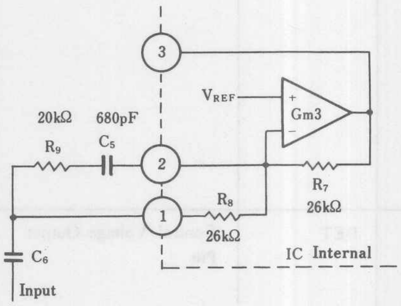
Low sound band element: It is extracted by bandpass filter consisted of internal resistors in 1 & 16 pins, external capacitor in 13 pin and Gm1 upon input in 1 and 16 pins. This signal goes through Gm4 after amplified in narrower bandwidth at Gm3, and output at 3 and 14 pins after added by the addition circuit of the main signal. The above circuits operate as the bigger signal, the larger amplification. Gm3 has one more output. The output signal rectified by all-wave rectifying circuit becomes controlled voltage by being balanced by external 12 pin capacitor. The controlled voltage controls the gain at Gm4 and Gm2 operates as limitter circuit to avoid saturation as the input signal becomes larger than some certain level. When the boost is off, the input signals at 1 & 16 pins output as they are by the gain 1 amplifier. When the mute is on, the signal is shut off by output circuit input connected to V_{REF}.

■ APPLICATION NOTE

1. Power supply
   The NJM2106 is a single power supply IC operated at the voltages from 0.9V to 2.5V. The standard voltage generated at 10 pin is fixed at about 0.71V considering the low voltage operation. As such head room is not expandable even though the supply voltage is increased. Accordingly, the IC is suitable for single supply voltage operation by one dry cell battery and at 3V setting, the signal level is required to be lowered.

2. Operation mode control
   The NJM2106 functions are controlled by internal electronic switch. the switch of the operation modes is designed to be controlled by either connecting or opening on & off of the boost and mute at 2 terminals. So, the use of mechanical switch is recommended. the following precausion should be taken in case of using NPN transistor to control.
   (1) The voltage should be loaded at 5 & 11 pins lower than 0.2V on 9 & v^+ and higher than 0.4V on 8 pin(GND).
   (2) As 11 pin, mute control, is not digitally controlled, in case of switch on for mute, the voltage should be less than 0.2V, and in case of off, it should be open as much as possible. In case that it cannot be opened at switch off, the current coming into 11 pin should be less than 2uA. In this case outputs at 3 and 14 pins sometime oscillate, so stop it by putting the capacitor (1000 through 5000 pF) between 3/14 pins and ground. When the mute is on, 3 & 14 pins are in not signal position and generates the same voltage (approx. 0.71V) of that of V_{REF}.

3. Control of boost volume in high sound band
   The boost is obtained by adding the high sound band element taken out by HPF at A and B channels to the main signal.
   The signal in high sound band is boosted by the following equations.
   Gain: $GH=R7\cdot\{1/R_8+1/(R_9+1j\omega C_5)\}$
   Cutoff Frequency: $f_{HH}=1/(2\pi R_9\cdot C_5)$
   In one of the application cases shown at right,
   $f_{HH}=11.7kHz$
   Gain at 20kHz is around 6 dB.



4. Control of boost volume in low sound band

The bost is controlled by bandpass filter by LPF/HPF which takes out low sound band of IN(A) and IN(B), by gain control circuit and the circuit generating the control signal and by headroom control circuit. As the band and gain of the above filter are set up by the external C & R, low sound amplification effect is adjusted by external constant.

The foolwings are referenced to when adjusting.

(1) LPF cutoff frequency to be set up by R1, internal resistor and C1, external capacitor.

Cutoff frequency: $F_{L1}=1/(2\pi R_1/2\cdot C_1)$

(2) HPF cutoff frequency and gain to be set up by:

Internal resistor, R2 & R3, and external resistor, R4, and external capacitor, C2.

Gain: $G=1+R_2/(R_3+R_4+1/j\omega C_2)$

Cutoff Frequency: $f_{H1}=1/\{2\pi\cdot(R_3+R_4)\cdot C_2\}$

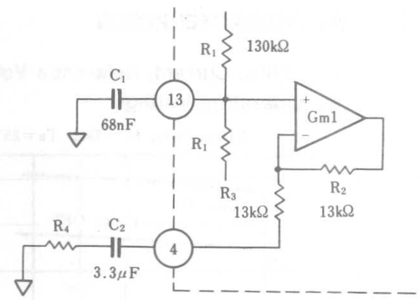
(3) Cutoff frequency and gain of the amplifier with weighting function

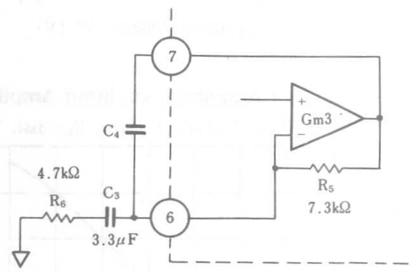
They are set up by internal resistor, R5, external resistor, R6 and external capacitor, C3 as shown in the following equations.

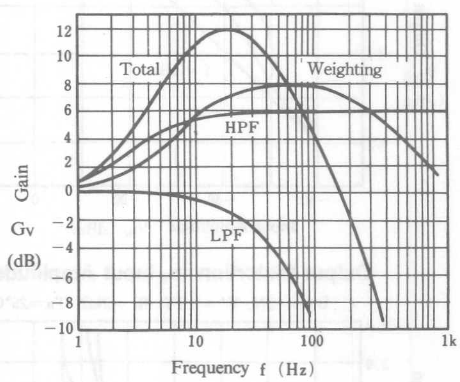
Gain: $G=1+jwC_3\cdot R_5/(1+jwC_3\cdot R_6)/(1+jwC_4\cdot R_5)$

Cutoff Frequency: $F_{L2}=1/(2\pi\cdot R_6\cdot C_3)$

$F_{H2}=1/(2\pi\cdot R_5\cdot C_4)$



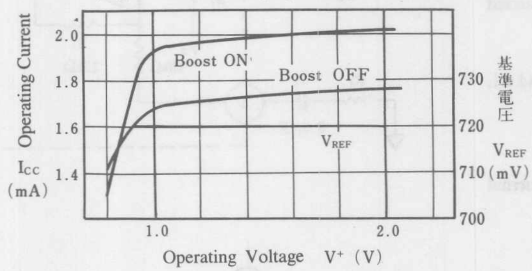




■ TYPICAL CHARACTERISTICS

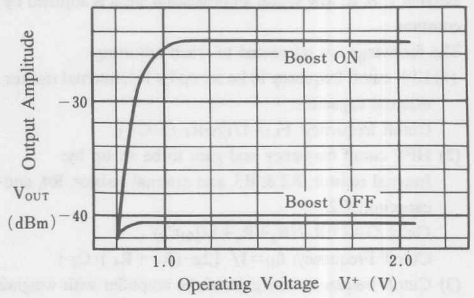
Operating Current, Reference Voltage vs. Operating Voltage

($V_{IN}=-18dBm/1kHz$, $R_L=3k\Omega$, $Ta=25°C$)



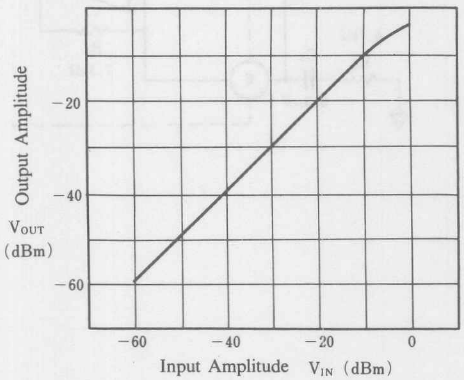
Output Amplitude vs. Operating Voltage

($V_{IN}=-40dBm/50Hz$, $R_L=3k\Omega$, $Ta=25°C$)



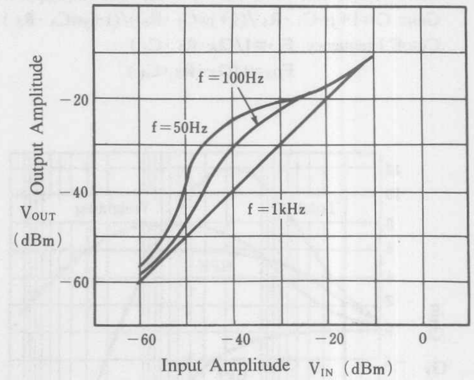
Output Amplitude vs. Input Amplitude

(Boost OFF, $V^+=1.1V$, $f=1kHz$, $R_L=3k\Omega$, $Ta=25°C$)



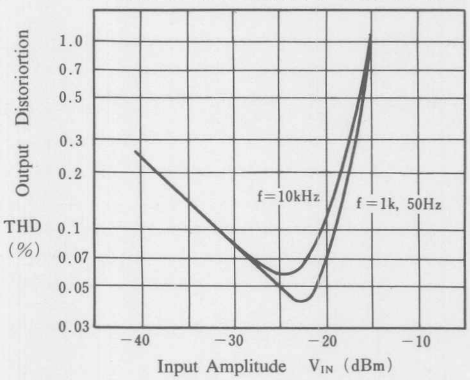
Output Amplitude vs. Input Amplitude

(Boost ON, $V^+=1.1V$, $R_L=3k\Omega$, $Ta=25°C$)



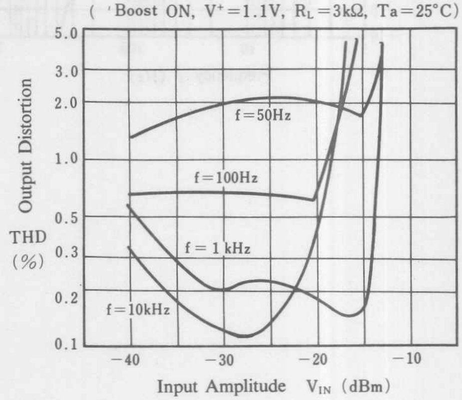
Output Distortion vs. Input Amplitude

(Boost OFF, $V^+=1.1V$, $R_L=3k\Omega$, $Ta=25°C$)

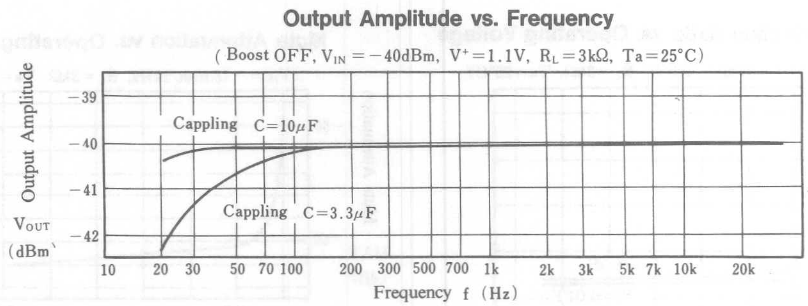


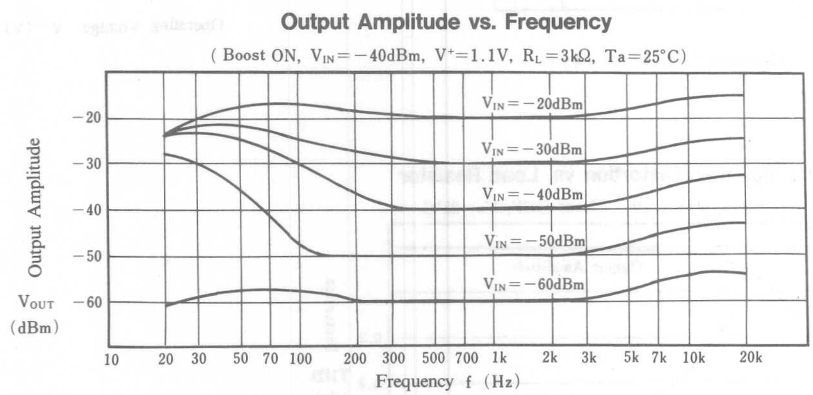
Output Distortion vs. Input Amplitude

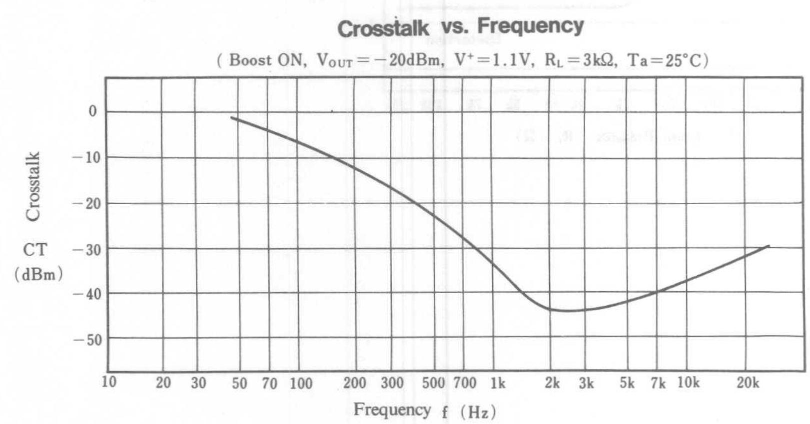
(Boost ON, $V^+=1.1V$, $R_L=3k\Omega$, $Ta=25°C$)



■ TYPICAL CHARACTERISTICS



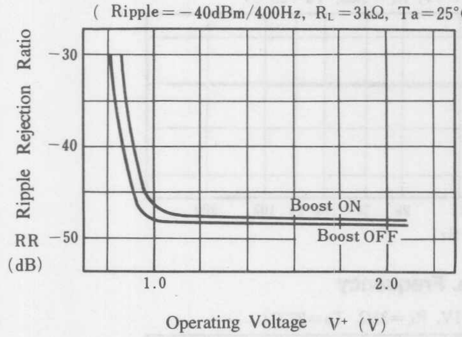




■ TYPICAL CHARACTERISTICS

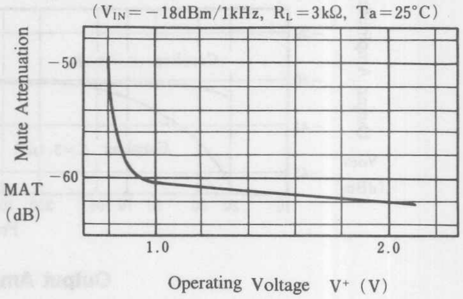
Ripple Rejection Ratio vs. Operating Voltage

(Ripple = −40dBm/400Hz, R_L = 3kΩ, Ta = 25°C)



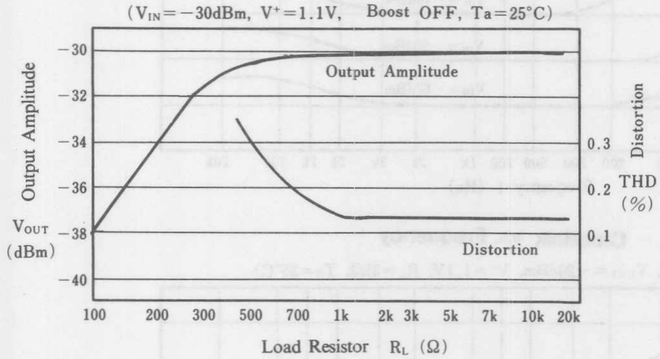
Mute Attenuation vs. Operating Voltage

(V_{IN} = −18dBm/1kHz, R_L = 3kΩ, Ta = 25°C)

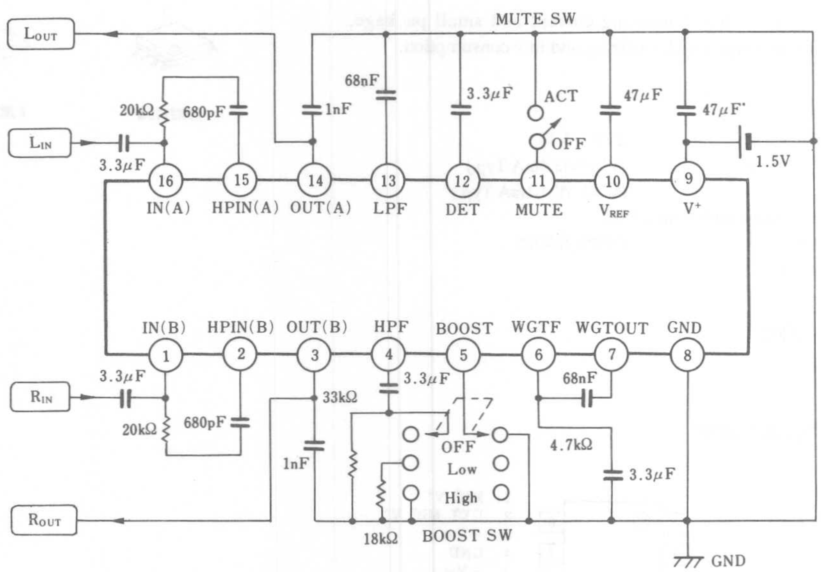


Output Amplitude, Distortion vs. Load Resistor

(V_{IN} = −30dBm, V^+ = 1.1V, Boost OFF, Ta = 25°C)



■ APPLICATION CIRCUIT



■ GENERAL DESCRIPTION

NJM2110 is a monaural microphone amplifier for video camera. It can operate from 2.7V.

The performance is low Operating current and small package, therefore it is easy to design the downsizing and low consumption.

■ PACKAGE OUTLINE

NJM2110M NJM2110V

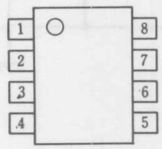
■ FEATURES

- Operating Voltage 2.7V~5.3V
- Low Operating Current (V^+=5V:3.5mA Typ.)
  (V^+=3.3V:1.1mA Typ.)
- Short Circuit Protection for External MIC.
- Package Outline DMP8, SSOP8
- Bipolar Technology

■ APPLICATION

- Video Camera

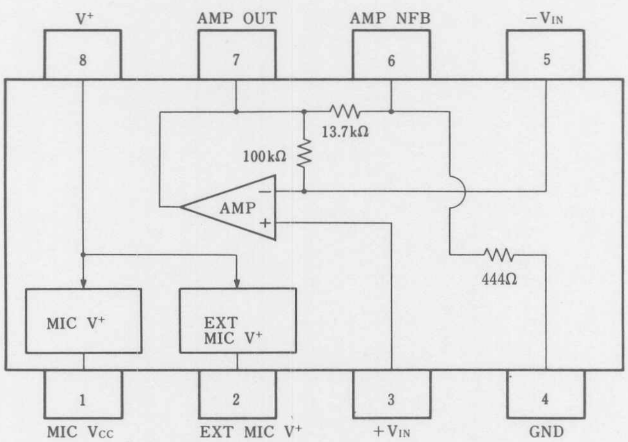
■ PIN CONFIGURATION



1. MIC V^+
2. EXT MIC V^+
3. $+V_{IN}$
4. GND
5. $-V_{IN}$
6. AMP NFB
7. AMP OUT
8. V^+

NJM2110M
NJM2110V

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

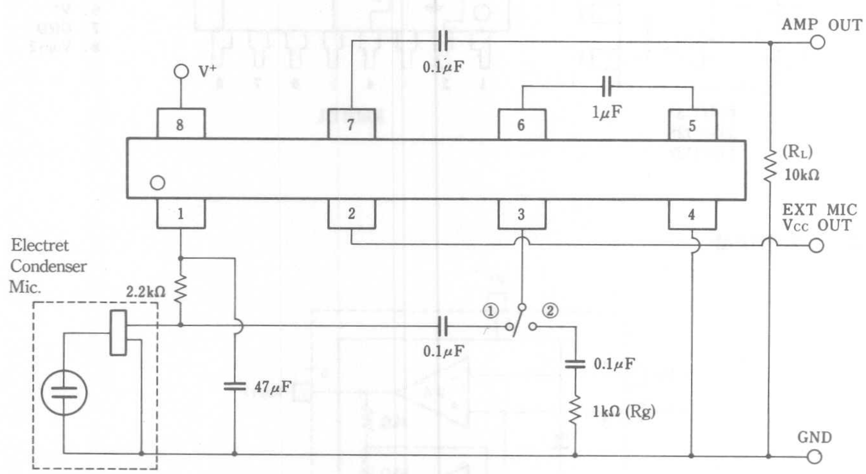
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	7.0	V
Power Dissipation	P_D	(SSOP8) 250	mW
		(DMP8) 300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current 1	I_{CC} 1		—	3.5	4.5	mA
Operating Current 2	I_{CC} 2	V^+= 3.3V	—	1.1	2.0	mA
Transfer Gain	Gv	f=1kHz	27	28	29	dB
Total Harmonic Distortion	THD	f=1kHz, Vo=300mV_{rms}, R_L=10kΩ	—	0.05	0.2	%
Maximum Output Voltage	V_{om}	f=1kHz, V^+=2.7V, THD=1%, R_L=10kΩ	2.0	2.5	—	V_{P-P}
Output Noise Voltage	V_{no}	R_g=1kΩ, C=0.1μF, A−Weight	—	30	42	μVrms
Input Resistance Gain	Zin	f=1kHz	—	110	—	kΩ
Output Resistance	Zo	f=1kHz	—	10	—	Ω
MIC Output Supply Voltage 1	MIC_O 1		2.0	2.35	2.7	V
MIC Output Supply Voltage 2	MIC_O 2	V^+=2.7V	2.0	2.25	2.5	V
External Output Supply Voltage	EXT_{out}	Io=25mA	4.0	—	—	V
Output Short Circuit Current	Ios	EXT_O=0V	—	—	30	mA

■ TEST CIRCUIT



※SW②:Output Noise Voltage TEST

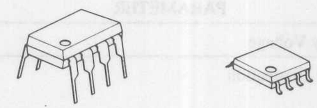
LOW VOLTAGE AUDIO POWER AMPLIFIER

■ GENERAL DESCRIPTION

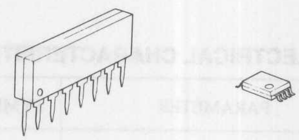
The NJM2113 is a audio power amplifier desined for telephone applications, such as in speakerphones.

Coupling capacitors to the speaker are not required, as it has differential speaker outputs. The closed loop gain is set with two external resistors. A CD pin permit powering down with muting the input signal.

■ PACKAGE OUTLINE



NJM2113D NJM2113M



NJM2113L NJM2113V

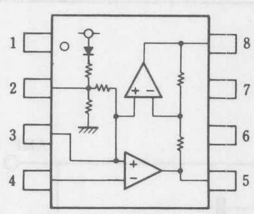
■ FEATURES

- Wide Operating Voltage (2~16V)
- Low Operating Current (2.7mA Typ.)
- CD Input to Power Down the IC with Mute
- Low Power-Down Operating Current (72 μA Typ.)
- Output Power Exceeds 250mW (V^+=6V, R_L=32Ω)
- Gain Adjustable (G_{VD}=0~43dB, Voice Band)
- Package Outline DMP8,DMP8, SIP8, SSOP8
- Bipolar Technology

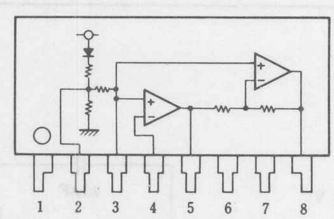
■ RECOMMENDED OPERATING CONDITIONS

- Load Impedance R_L 8~200Ω
- Differential Gain G_{VD} 0~43dB (5kHz bandwidth)
- Input Voltage at CD V_{CD} 0~V^+ Vdc

■ PIN CONFIGURATION



NJM2113D
NJM2113M
NJM2113V

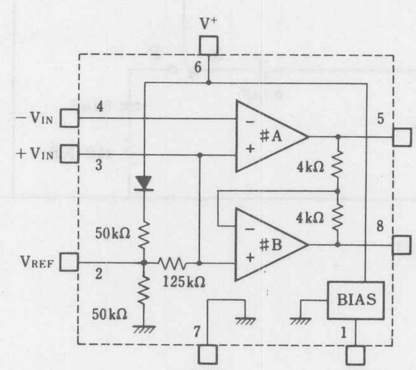


NJM2113L

Pin Function

1. CD
2. V_{REF}
3. $+V_{IN}$
4. $-V_{IN}$
5. $V_{OUT}1$
6. V^+
7. GND
8. $V_{OUT}2$

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+18	V
Output Peak Current	I_{OP}	±250	mA
Input Voltage Range	V_{IN}	(1~4pin) −0.3 to V^++0.3	V
		(5,8pin) −0.3 to V^++0.3(when Power-Down)	V
Power Dissipation	P_D	(DIP8) 500	mW
		(SIP8) 800	mW
		(DMP8) 500 (note 1)	mW
		(SSOP8) 360 (note 1)	mW
Operating Temperature Range	T_{opr}	−20~+75	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

(note 1) At on PC bosrd

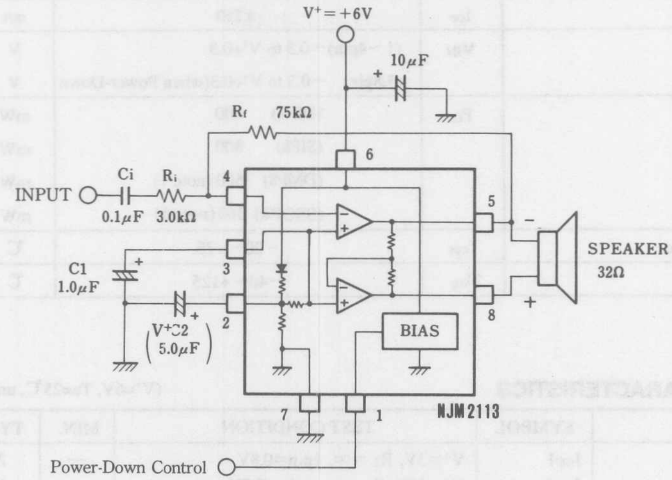
■ ELECTRICAL CHARACTERISTICS

(V^+=6V, Ta=25℃, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	$I_{CC}1$	V^+=3V, R_L=∞, 1pin=0.8V	—	2.7	4.0	mA
(no signal)	$I_{CC}2$	V^+=16V, R_L=∞, 1pin=0.8V	—	3.4	5.0	mA
	I_{CCD}	V^+=3V, R_L=∞, 1pin=2V	—	72	100	μA
Open Loop Gain	A_V1	Amplifier#A, f<100Hz	77	83	—	dB
Closed Loop Gain	A_V2	Amplifier#B, f=1kHz, R_L=32Ω	−0.35	0	+0.35	dB
Output Power	P_O1	V^+=3V, R_L=16Ω, THD≦10%	55	—	—	mW
(note2)	P_O2	V^+=6V, R_L=32Ω, THD≦10%	250	—	—	mW
	P_O3	V^+=12V, R_L=100Ω, THD≦10%(note3)	400	—	—	mW
Total Harmonic Distortion	THD1	V^+=6V, R_L=32Ω, P_O=125mW, G_{VD}=34dB	—	0.5	1.0	%
(f=1kHz)	THD2	V^+≧3V, R_L=8Ω, P_O=20mW, G_{VD}=12dB	—	0.5	—	%
	THD3	V^+≧12V, R_L=32Ω, P_O=200mW, G_{VD}=34dB	—	0.6	—	%
Power Supply Rejection Ratio	PSRR1	C1=∞, C2=0.01μF, DC	50	—	—	dB
(V^+=6V, ΔV^+=3V)	PSRR2	C1=0.1μF, C2=0, f=1kHz	—	12	—	dB
	PSRR3	C1=1μF, C2=5μF, f=1kHz	—	52	—	dB
Mute Attenuation	MAT	f=1kHz~20kHz, 1pin=2V	—	70	—	dB
Output Voltage	V_O1	V^+=3V, R_L=16Ω	1.00	1.18	1.25	V
(R_f=75kΩ, DC)	V_O2	V^+=6V	—	2.68	—	V
	V_O3	V^+=12V	—	5.71	—	V
Output High Level	V_{OH}	I_{OUT}=-75mA, V^+=2~16V	—	V^+−1.1	—	V
Output Low Level	V_{OL}	I_{OUT}=75mA, V^+=2~16V	—	0.21	—	V
Output DC Offset	ΔV_O	R_f=75kΩ, R_L=32Ω, 5pin-8pin	−30	0	+30	mV
Input Bias Current	I_B	4pin	—	−30	−200	nA
Equivalent Resistance	R_{+IN}	3pin	100	150	220	kΩ
	R_{REF}	2pin	18	25	40	kΩ
CD Input Voltage H	V_{CDH}	1pin	2.0	—	V^+	V
CD Input Voltage L	V_{CDL}	1pin	0.0	—	0.8	V
CD Input Resistance	R_{CD}	V_{CD}=16V, 1pin	50	75	175	kΩ

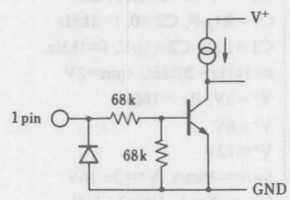
(note2) NJM2113M, NJM2113V:At on PC Board
(note3) Not specified for NJM2113V

■ APPLICATION CIRCUIT



Notice: 1. CD——A logic "Low" (<0.8V) sets normal operation.
A logic "High" (>2.0V) sets the power down mode.

2. Power supply rejection is provided by C1 and C2.
C2 is unnecessary, if C1 is sufficient capacitances.
3. C1 and C2 also effect the turn-on time of the circuit at power-up.
4. Equivalent Circuit of CD is as in the following diagram.



Equivalent Circuit of CD

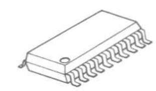
5. Normally a snubber is not needed at the output of the NJM2113, un-like many other audio amplifiers (NJM2073 etc.). However the PC board layout, stray capacitances, and the manner in which the speaker wires configured, may dictate otherwise.

RF AMPLIFIER FOR CD PLAYER

■ GENERAL DESCRIPTION

NJM2117 is designed for CD player, which contains RF amplifier for 3 spot system optical PICK-UP output, FOCUS error amplifier and APC circuit.

■ PACKAGE OUTLINE



NJM2117V

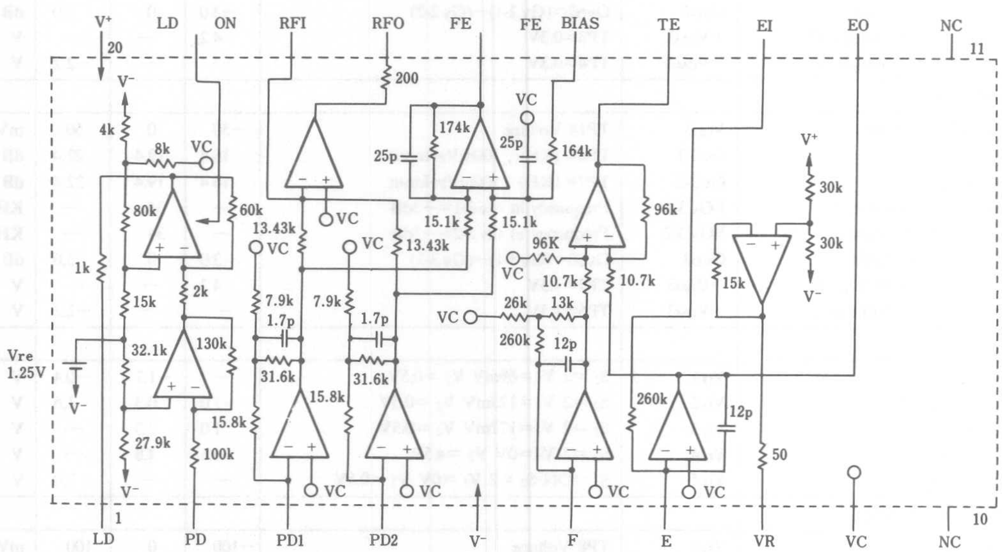
■ FEATURES

- Dual Supply ±5V Operation
- Single Supply +5V Operation Available
- Package Outline SSOP20
- Bipolar Technology

■ PIN FUNCTION

1. LD	20. V+
2. PD	19. LD ON
3. PD1	18. RF1
4. PD2	17. RFO
5. V-	16. FE
6. F	15. FE BIAS
7. E	14. TE
8. VR	13. EI
9. VC	12. EO
10. NC	11. NC

■ BLOCK DIAGRAM



NJM2117V

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+/V^-	±6	V
Power Dissipation	P_D	(SSOP8) 300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+/V^-=±5.0V, Ta=25℃)

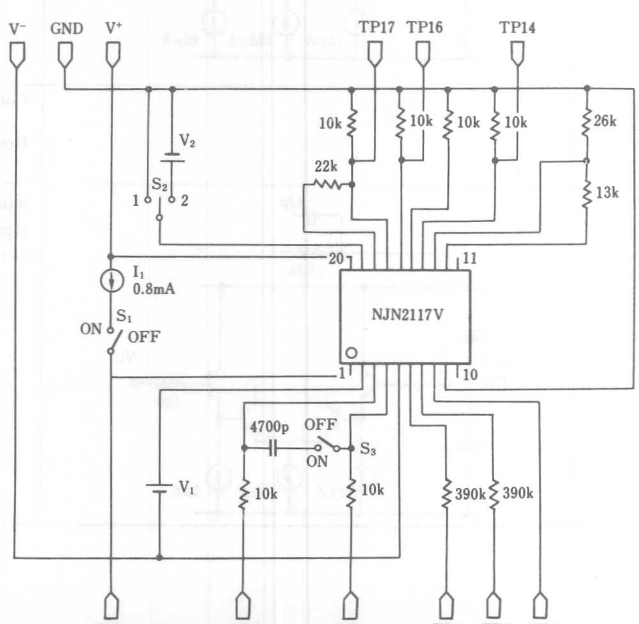
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	20pin	—	8.0	12.0	mA
Operating Current	I_{EE}	5pin	−12.0	−8.0	—	mA
〈RF Amplifier〉						
Output Offset Voltage	$V_{OO}1$	TP17 Voltage	−50	—	50	mV
Voltage Gain	G_V1	TP3/4=2KHz, 30mV$_{PP}$INPUT	28.2	31.2	34.2	dB
Frequency Characteristic	FG_V1	Frequency at G_V1=−3dB	1.50	3.75	—	MHZ
Maximum Output Voltage H	$+V_{OM}1$	TP3=0.6V	3.5	—	—	V
Maximum Output Voltage L	$-V_{OM}1$	TP3=−0.6V	—	—	−0.3	V
〈FE Amplifier〉						
Output Offset Voltage	$V_{OO}2$	TP16 Voltage	−120	0	120	mV
Output Noise	V_{NOISE}	S3=ON TP16Noise (100KHZ LPF)	—	15	30	mV$_{rms}$
Voltage Gain 1	$G_V2\text{-}1$	TP3=1KHz, 10mV$_{PP}$Input	39.1	42.1	45.1	dB
Voltage Gain 2	$G_V2\text{-}2$	TP4=1KHz, 10mV$_{PP}$Input	39.1	42.1	45.1	dB
Frequency Characteristic 1	$FG_V2\text{-}1$	Frequency at $G_V2\text{-}1$=−3dB	—	27	—	KHZ
Frequency Characteristic 2	$FG_V2\text{-}2$	Frequency at $G_V2\text{-}2$=-3dB	—	27	—	KHZ
Difference Voltage Gain	$G_{VD}2$	$G_{VD}2$=($G_V2\text{-}1$)−($G_V2\text{-}2$)	−3.0	0	3.0	dB
Maximum Output Voltage H	$+V_{OM}2$	TP3=0.3V	4.2	—	—	V
Maximum Output Voltage L	$-V_{OM}2$	TP4=0.3V	—	—	−2.2	V
〈TE Amplifier〉						
Output Offset Voltage	$V_{OO}3$	TP14 Voltage	−50	0	50	mV
Voltage Gain 1	$G_V3\text{-}1$	TP6=1KHz, 100mV$_{PP}$Input	16.4	19.4	22.4	dB
Voltage Gain 2	$G_V3\text{-}2$	TP7=1KHz, 100mV$_{PP}$Input	16.4	19.4	22.4	dB
Frequency Characteristic 1	$FG_V3\text{-}1$	Frequency at $G_V3\text{-}1$=−3dB	—	34	—	KHZ
Frequency Characteristic 2	$FG_V3\text{-}2$	Frequency at $G_V3\text{-}2$=−3dB	—	34	—	KHZ
Difference Voltage Gain	$G_{VD}3$	$G_{VD}3$=($G_V3\text{-}1$)−($G_V3\text{-}2$)	−3.0	0	3.0	dB
Maximum Output Voltage H	$+V_{OM}3$	TP7=1.5V	4.2	—	—	V
Maximum Output Voltage L	$-V_{OM}3$	TP6=1.5V	—	—	−2.2	V
〈APC〉						
Output Voltage 1	V_O1	S_2=2 V1=69mV V_2=0.5V	—	−1.7	−0.4	V
Output Voltage 2	V_O2	S_2=2 V1=123mV V_2=0.5V	−1.0	0.3	1.6	V
Output Voltage 3	V_O3	S_2=2 V1=177mV V_2=0.5V	1.0	2.3	—	V
Output Voltage 4	V_O4	S_2=2 V1=0V V_2=4.5V	4.6	4.8	—	V
Output Voltage 5	V_O5	S_1=ON S_2=2 V_1=0V V_2=0.5V	—	—	2.0	V
〈Center Voltage Amp.〉						
Output Voltage 6	V_O6	TP8 Voltage	−100	0	100	mV

■ ELECTRICAL CHARACTERISTICS

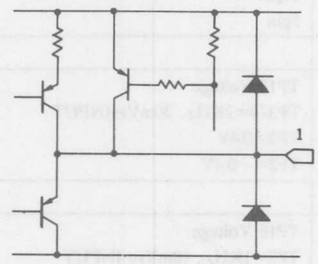
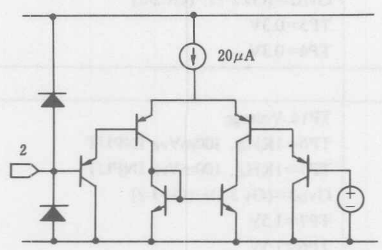
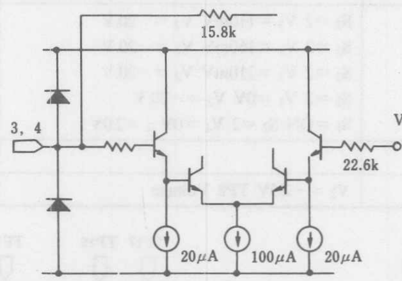
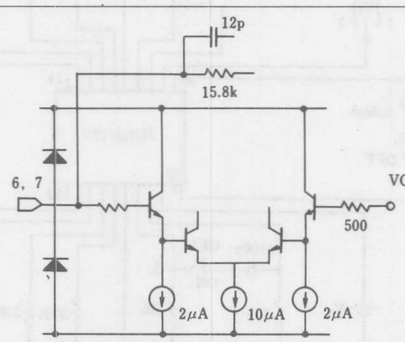
($V^+/V^-=\pm 2.5V$, Ta=25°C)

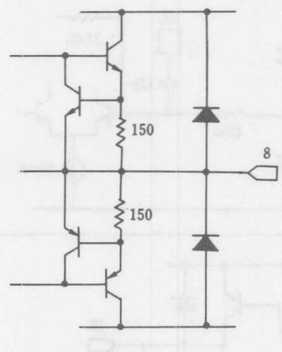
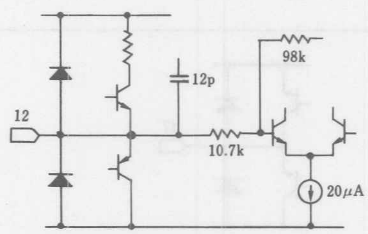
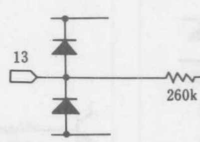
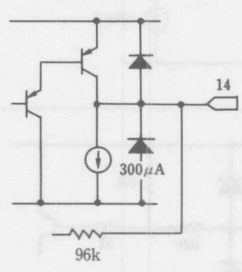
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	20pin	—	6.0	12.0	mA
Operating Current	I_{EE}	5pin	−12.0	−6.0	—	mA
〈**RF Amplifier**〉						
Output Offset Voltage	$V_{OO}1$	TP17 Voltage	−50	—	50	mV
Voltage Gain	$G_V 1$	TP3/4=2KHz, 30mV_{PP}INPUT	28.2	31.2	34.2	dB
Maximum Output Voltage H	$+V_{OM}1$	TP3=0.4V	$V^+-0.5$	—	—	V
Maximum Output Voltage L	$-V_{OM}1$	TP3=−0.4V	—	—	$V^-+2.2$	V
〈**FE Amplifier**〉						
Output Offset Voltage	$V_{OO}2$	TP16 Voltage	−120	0	120	mV
Voltage Gain 1	$G_V 2$-1	TP3=1KHz, 10mV_{PP} INPUT	39.1	42.1	45.1	dB
Voltage Gain 2	$G_V 2$-2	TP4=1KHz, 10mV_{PP} INPUT	39.1	42.1	45.1	dB
Difference Voltage Gain	$G_{VD}2$	$G_{VD}2$=(G_V 2-1)−(G_V 2-2)	−3.0	0	3.0	dB
Maximum Output Voltage H	$+V_{OM}2$	TP3=0.3V	$V^+-0.5$	—	—	V
Maximum Output Voltage L	$-V_{OM}2$	TP4=0.3V	—	—	$V^-+0.5$	V
〈**TE Amplifier**〉						
Output Offset Voltage	$V_{OO}3$	TP14 Voltage	−50	0	50	mV
Voltage Gain 1	$G_V 3$-1	TP6=1KHz, 100mV_{PP} INPUT	16.4	19.4	22.4	dB
Voltage Gain 2	$G_V 3$-2	TP7=1KHz, 100mV_{PP} INPUT	16.4	19.4	22.4	dB
Difference Voltage Gain	$G_{VD}3$	$G_{VD}3$=(G_V 3-1)−(G_V 3-2)	−3.0	0	3.0	dB
Maximum Output Voltage H	$+V_{OM}3$	TP7=1.5V	$V^+-0.5$	—	—	V
Maximum Output Voltage L	$-V_{OM}3$	TP6=1.5V	—	—	$V^-+0.5$	V
〈**APC**〉						
Output Voltage 1	$V_O 1$	S_2 =2 V_1 =110mV V_2 =−20.V	—	−1.6	−0.3	V
Output Voltage 2	$V_O 2$	S_2 =2 V_1 =160mV V_2 =−20.V	−1.1	0.2	1.5	V
Output Voltage 3	$V_O 3$	S_2 =2 V_1 =210mV V_2 =−20.V	0.8	2.1	—	V
Output Voltage 4	$V_O 4$	S_2 =2 V_1 =0V V_2 =−20.V	2.1	2.3	—	V
Output Voltage 5	$V_O 5$	S_1 =ON S_2 =2 V_1 =0V $_2$ =2.0V	—	—	1.0	V
〈**Center Voltage Amp.**〉						
Output Voltage 6	$V_O 6$	V_2 =−2.5V TP8 Voltage	−70	0	70	mV

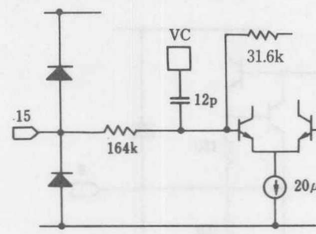
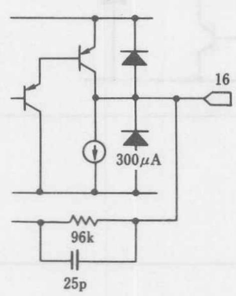
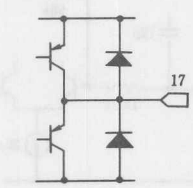
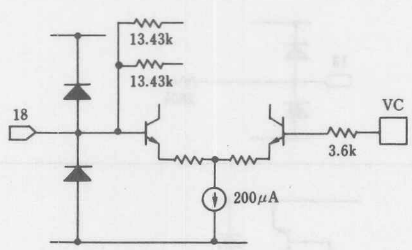
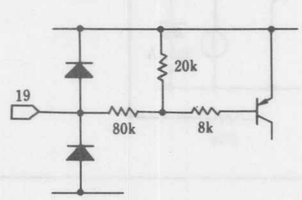
■ TEST CIRCUIT



■ TERMINAL EXPLANATION

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	TERMINAL EXPLANATION
1	LD		Output pin of APC AMP.
2	PD		Input pin of APC AMP.
3 4	PD1 PD2		Input pin of RF I-V AMP. Connect A+C pin, B+D pin of each photo-diode and current input.
5	V_{EE}		Connect minus supply. …(Two supply) Connect GND. …(Single supply)
6 7	F E		Input pin of TE I-V AMP. Connect E pin, F pin of each photo-diode and current input.

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	TERMINAL EXPLANATION
8	VR		Output pin of direct current $<(V_{CC}+V_{EE})/2>$.
9	VC		Input pin of internal center point voltage. Connect GND.······(±5V) Connect VR pin. ······(Single supply)
12	EO		Output pin for monitor of I-V AMP E.
13	EI		Gain adjustment pin of I-V AMP E.
14	TE		Output pin of TRACKING ERROR AMP. Output of E-F signal.

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	TERMINAL EXPLANATION
15	FE-BIAS		Bias adjustment pin of FOCUS ERROR AMP. (Non-inverting side)
16	FE		Output pin FOCUS ERROR AMP.
17	RFO		Output pin RF AMP.
18	RFI		Input pin of RF AMP. (Inverting side) Establish Gain of RF AMP by resistor between RFI pin and RFO pin.
19	$\overline{\text{LD ON}}$		Change-over pin(on/0ff) of APC AMP. ON···GND/OFF···V_{CC}
20	V_{CC}		Connect plus supply. ···························(Two supply) Connect Vcc. ·······················(Single supply)

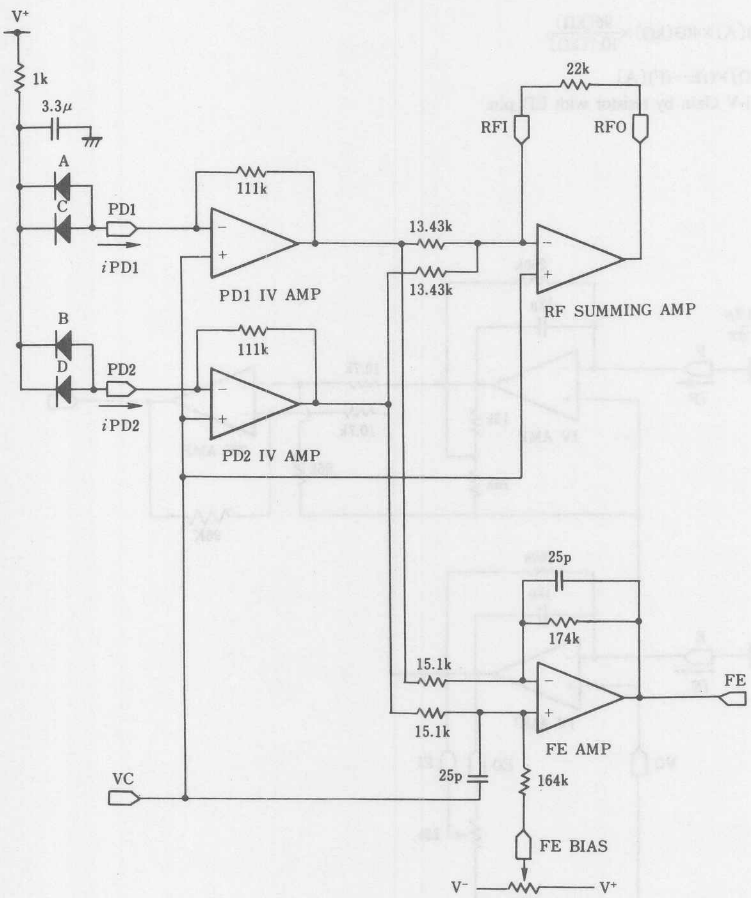
■ RF AMP

RFO-OUTPUT

$$V_{RFO}=(iPD1+iPD2)[A]\times 111[k\Omega]\times\frac{22[k\Omega]}{13.43[k\Omega]}$$

$$=181.8[k\Omega]\times(iPD1+iPD2)[A]$$

Establish Gain of RF AMP by resistor (22kΩ) between RFI pin and RFO pin.



FE AMP

FE OUTPUT

$$V_{FE} = (iPD1 - iPD2)[A] \times 111[k\Omega] \times \frac{174[k\Omega]}{15.1\ [k\Omega]}$$

$$= 1279[k\Omega] \times (iPD1 - iPD2)[A]$$

It is possible to controll FE Output Offset by variable resistor with FE BIAS pin.

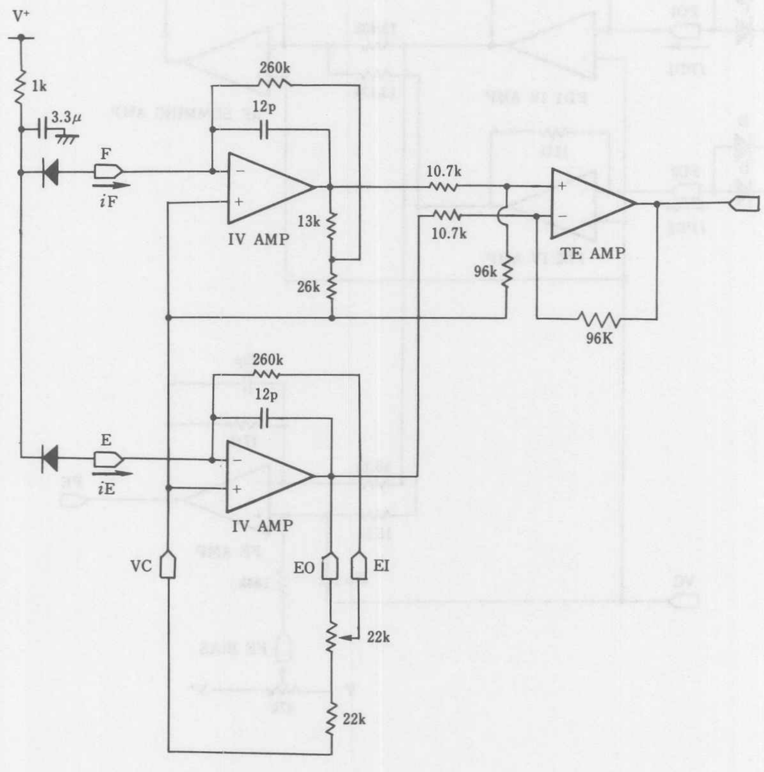
TE AMP

TE OUTPUT

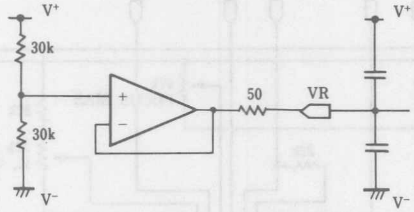
$$V_{TE} = (iE - iF)[A] \times 403[k\Omega] \times \frac{96[k\Omega]}{10.7[k\Omega]}$$

$$= 3616\ [k\Omega] \times (iE - iF)[A]$$

It is possible to trim 1-V Gain by resistor with ED pin.

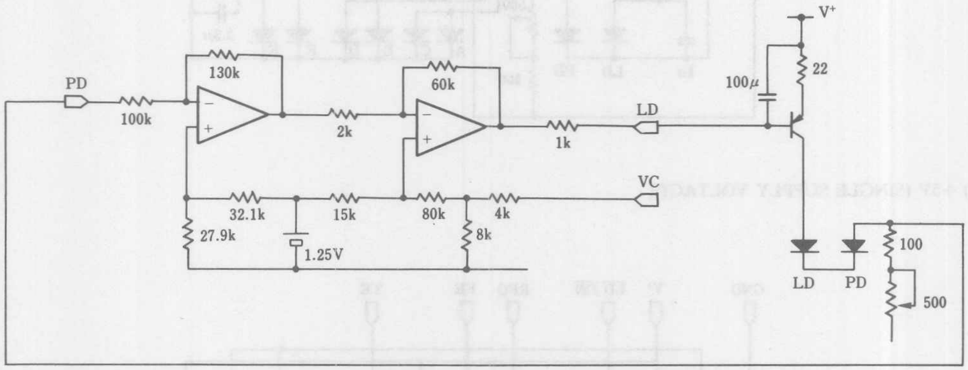


CENTER VOLTAGE GENERATION CIRCUIT



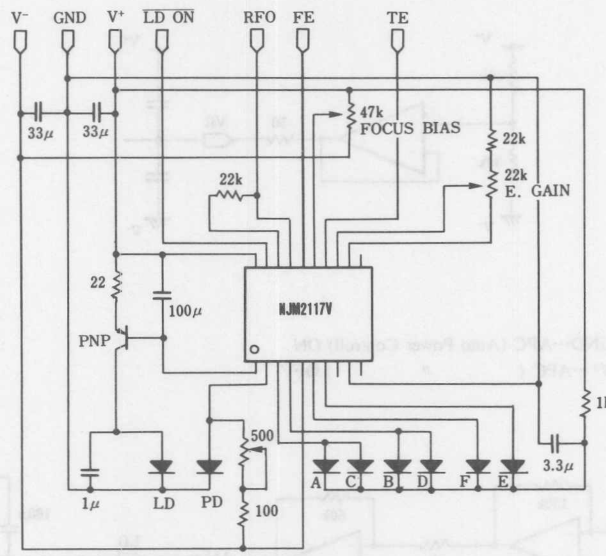
APC CIRCUIT

LD ON pin: connect to GND···APC (Auto Power Controll) ON
connect to V+···APC (〃) OFF

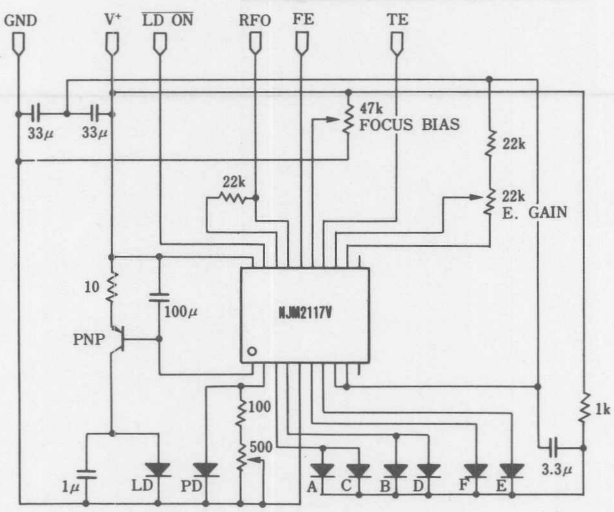


■ TYPICAL APPLICATION

1) ±5V (TWO SUPPLY VOLTAGE)



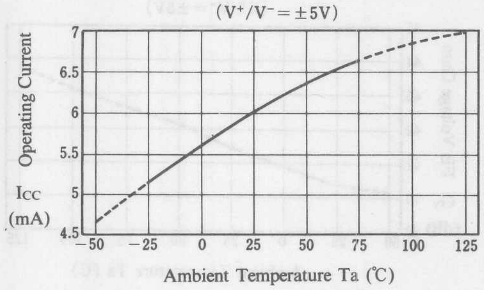
2) +5V (SINGLE SUPPLY VOLTAGE)



■ TYPICAL CHARACTERISTICS

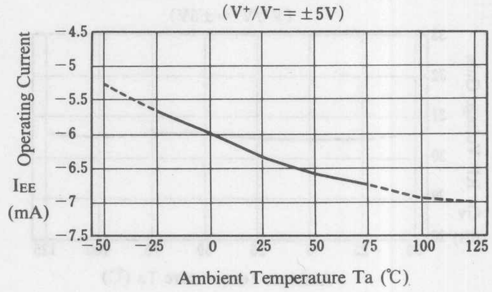
Operating Current(Icc)vs. Temperature

($V^+/V^- = \pm 5V$)



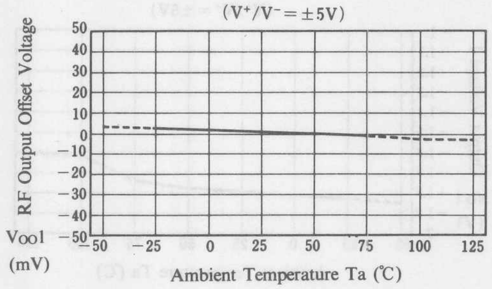
Operating Current (IEE) vs. Temperature

($V^+/V^- = \pm 5V$)



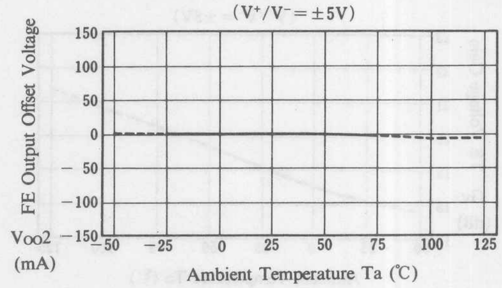
RF Output Offset Voltage vs. Temperature

($V^+/V^- = \pm 5V$)



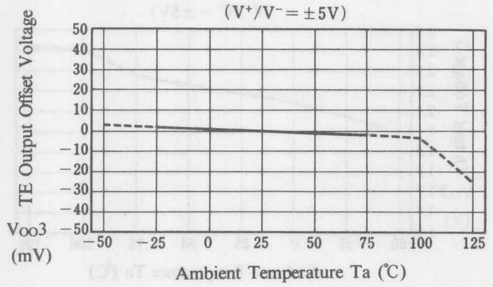
FE Output Offset Voltage vs. Temperature

($V^+/V^- = \pm 5V$)



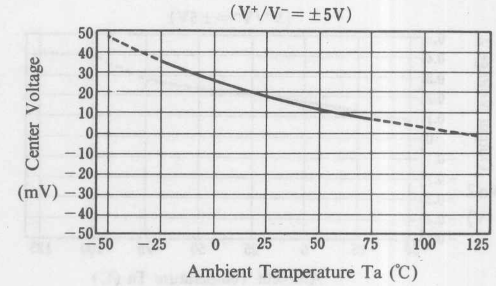
TE Output Offset Voltage vs. Temperature

($V^+/V^- = \pm 5V$)



Center Voltage vs. Temperature

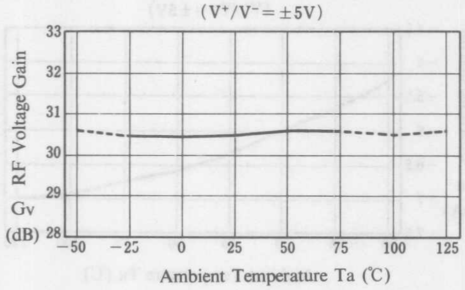
($V^+/V^- = \pm 5V$)



■ TYPICAL CHARACTERISTICS

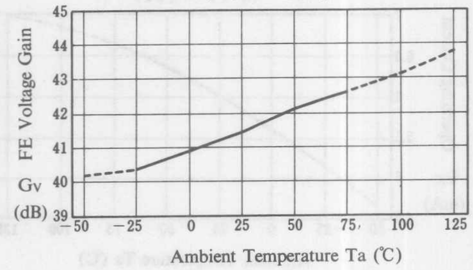
RF Voltage Gain vs. Temperature

(V+/V− = ±5V)



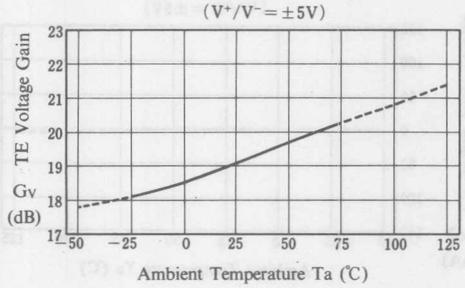
FE Voltage Gain vs. Temperature

(V+/V− = ±5V)



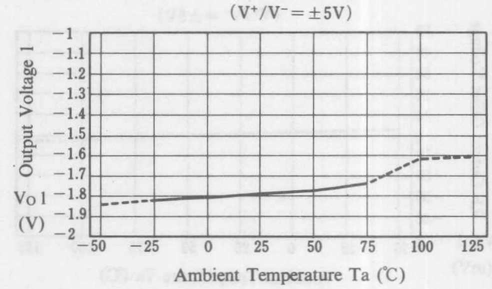
TE Voltage Gain vs. Temperature

(V+/V− = ±5V)



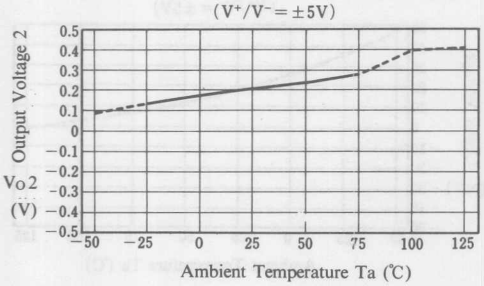
APC Vol vs. Temperature

(V+/V− = ±5V)



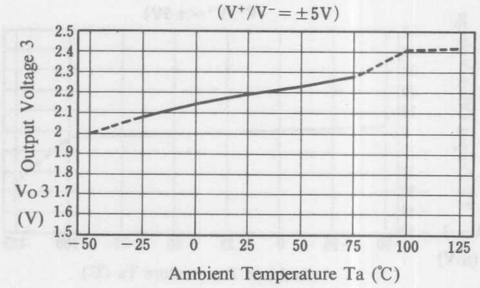
APC Vo2 vs. Temperature

(V+/V− = ±5V)



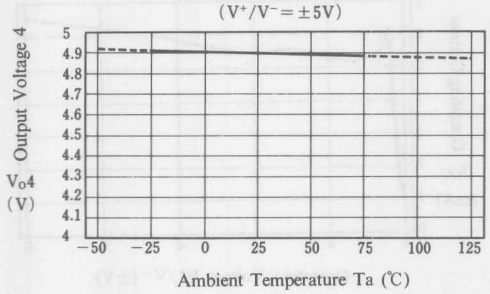
APC Vo3 vs. Temperature

(V+/V− = ±5V)

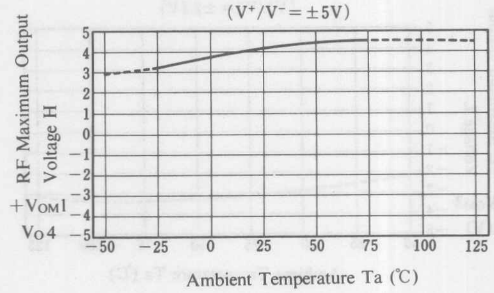


■ TYPICAL CHARACTERISTICS

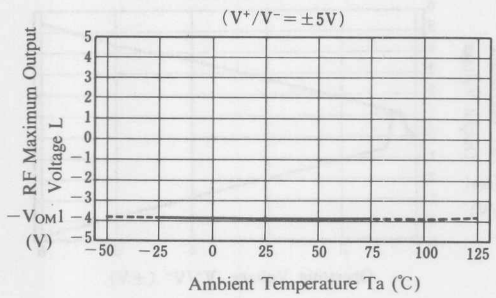
APC Vo4 vs. Temperature



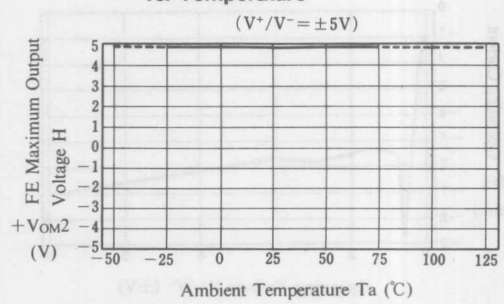
RF Maximum Output Voltage H vs. Temperature



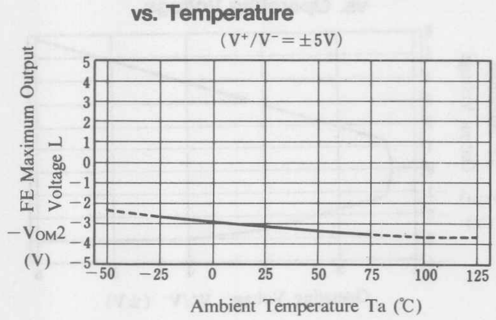
RF Maximum Output Voltage L vs. Temperature



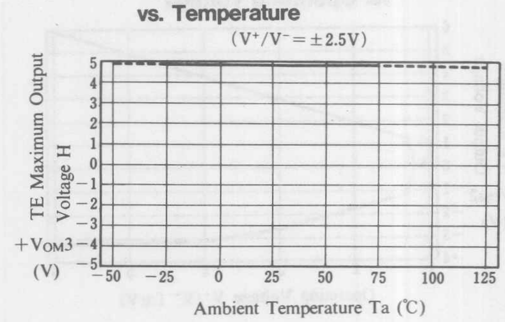
FE Maximum Output Voltage H vs. Temperature



FE Maximum Output Voltage L vs. Temperature

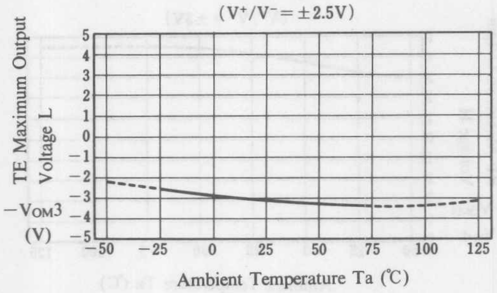


TE Maximum Output Voltage H vs. Temperature

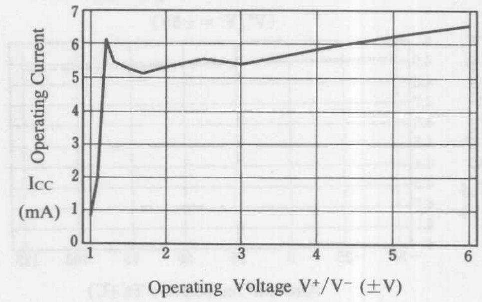


■ TYPICAL CHARACTERISTICS

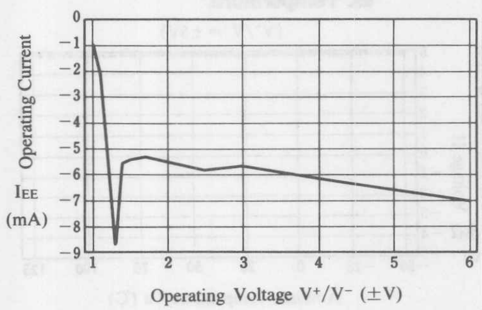
TE Maximum Output Voltage L vs. Temperature



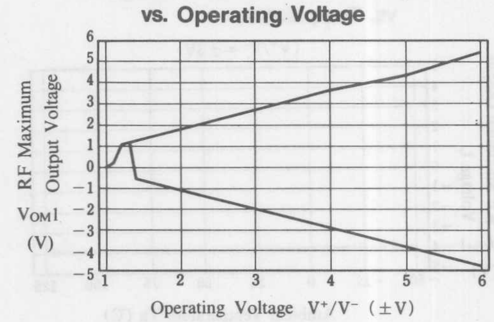
Operating Current(Icc) vs. Operating Voltage



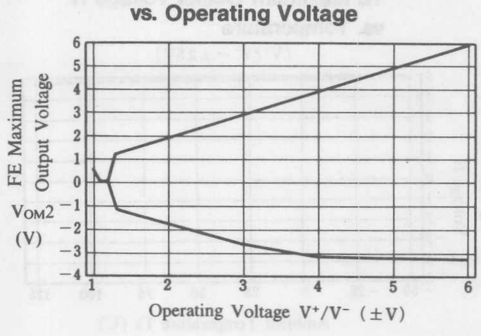
Operating Current(IEE) vs. Operating Voltage



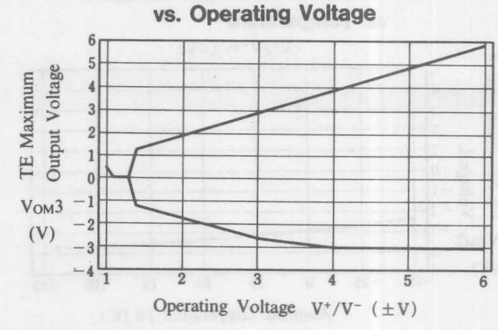
RF Maximum Output Voltage vs. Operating Voltage



FE Maximum Output Voltage vs. Operating Voltage

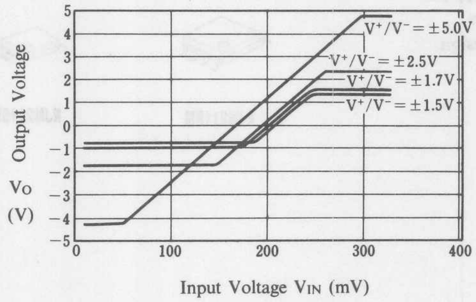


TE Maximum Output Voltage vs. Operating Voltage



■ TYPICAL CHARACTERISTICS

APC Input vs. Output Voltage



MONAURAL MICROPHONE AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2118 is a monaural microphone amplifier with current limit.

The low operating current and 3V or 5V operation are easy apply to portable items such as camcorder, microphone module and others.

The very small package of SSOP8 makes downsized PCB design.

■ PACKAGE OUTLINE

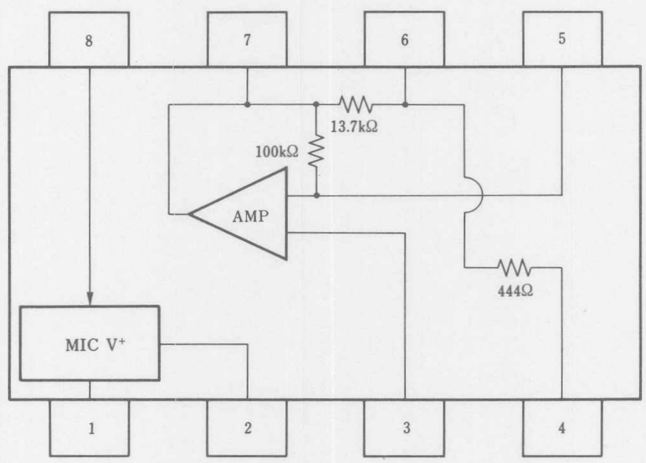
NJM2118M

NJM2118V

■ FEATURES

- Operating Voltage (+2.7V ~ +5.3V)
- Low Operating Current (1.0mA typ.)
- Low Noise (30 μVrms typ.)
- Bipolar Technology
- Package Outline DMP8, SSOP8

■ PIN CONFIGURATION



NJM2118M
NJM2118V

PIN FUNCTION
1 : MIC V+
2 : C-NOISE
3 : $+V_{IN}$
4 : GND
5 : $-V_{IN}$
6 : AMP NFB
7 : AMP OUT
8 : V+

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

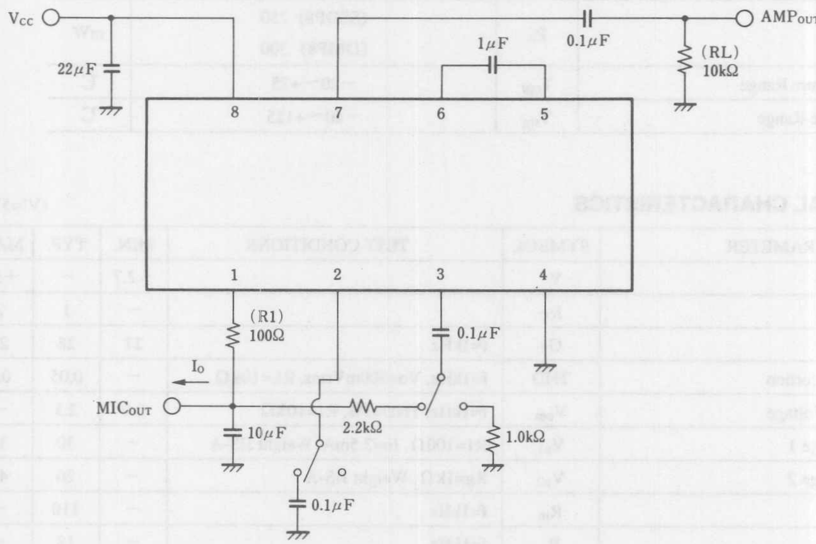
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+7	V
Power Dissipation	P_D	(SSOP8) 250 (DMP8) 300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		+2.7	−	+5.0	V
Operating Current	I_{CC}		−	1	2	mA
Voltage Gain	G_V	f=1kHz	27	28	29	dB
Total Harmonic Distortion	THD	f=1kHz, Vo=300mVrms, RL=10kΩ	−	0.05	0.5	%
Maximum Output Voltage	V_{om}	f=1kHz, THD=1%, R1=10kΩ	2.0	2.5	−	Vpp
Output Noise Voltage 1	V_{n1}	R1=100Ω, Io=2.5mA, Weight JIS-A	−	30	35	μVrms
Output Noise Voltage 2	V_{n2}	Rg=1kΩ, Weight JIS-A	−	20	42	μVrms
Input Impedance	R_{in}	f=1kHz	−	110	−	kΩ
Output Impedance	R_o	f=1kHz	−	18	−	Ω
Mic Output Supply Voltage 1	MI Cout1	Io=0mA	2.0	2.45	−	V
Mic Output Supply Voltage 2	MI Cout2	Io=2.5mA, R1=100Ω	2.0	2.15	−	V

■ TEST CIRCUIT



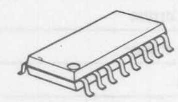
PRE & POWER AMPLIFIER WITH ALC

■ GENERAL DESCRIPTION

NJM2128 is a pre & power amplifier with ALC for micro and compact cassette recorders. It contains pre-amplifier, ALC circuit, power amplifiers, and ripple filter.

The pre-amplifier amplifies the signal come from magnetic head. The ALC circuit limits the input signal to optimize level in recording. The power amplifiers drive a speaker in play back and the magnetic head in recording. The ripple filter stabilizing the supply voltage to the internal pre-amplifier and an external condenser microphone.

■ PACKAGE OUTLINE

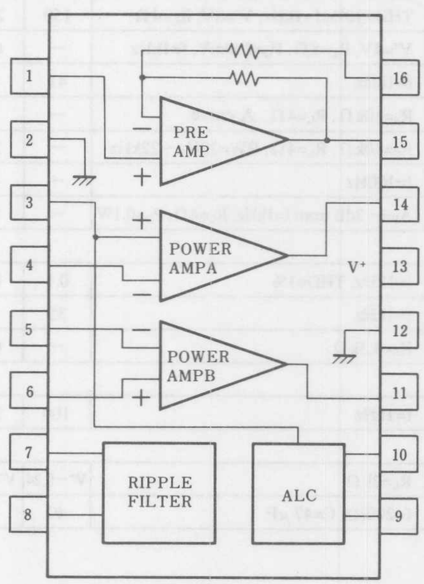


NJM2128M

■ FEATURES

- Operating Voltage 1.8V~7.0V
- Automatic Level Control (ALC) Limit Level=100mVrms $_{typ.}$(f=1kHz)
- Ripple Filter R.R. (Ripple Rejection)=47dB $_{typ.}$(f=200Hz, C=47 μF)
- Bipolar Technology
- Package Outline DMP16

■ PIN CONFIGURATION



NJM2128M

PIN FUNCTION
1. PRE+IN
2. SGND
3. POWER+INA
4. POWER−INA
5. POWER−INB
6. POWER+INB
7. RFOUT
8. RFIN
9. ALCIN
10. TC
11. POWER OUT B
12. POWER GND
13. V+
14. POWER OUT A
15. PREOUT
16. PRE−IN

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+7.0	V
PA Output Peak Current	I_{op}	1	A
PA Intput Voltage Range	V_{IN}	±0.4	V
Power Dissipation	P_D	(M-Type) 300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

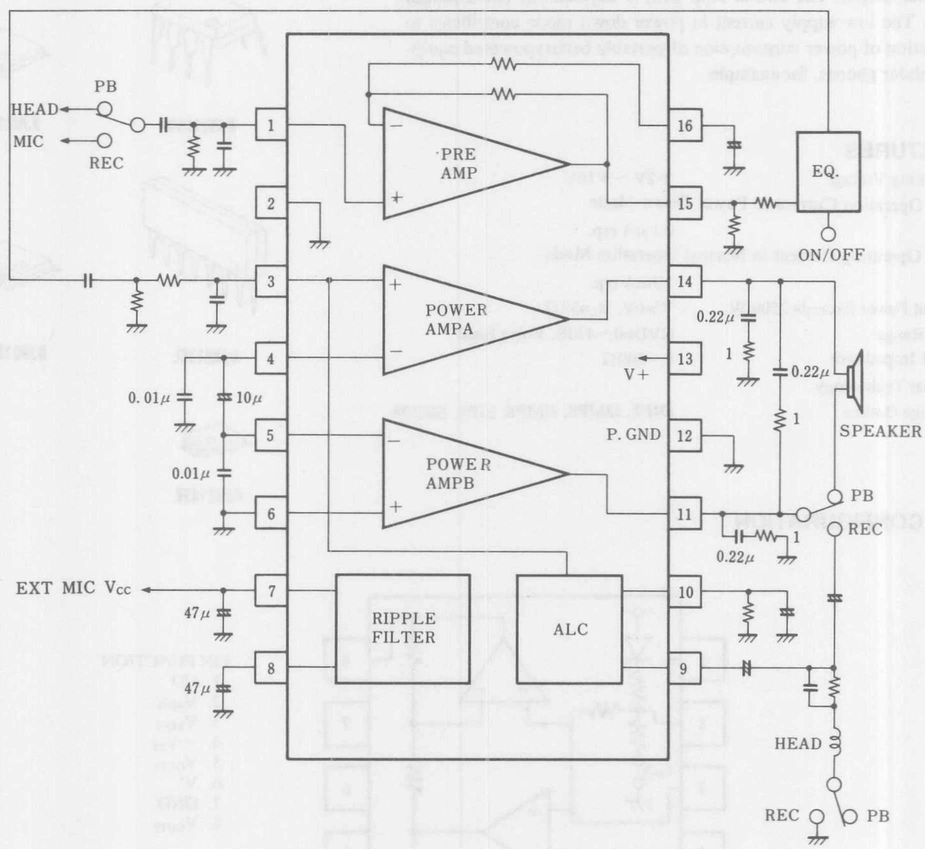
■ ELECTRICAL CHARACTERISTICS

(V^+=3V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		1.8	3.0	6.0	V
Operating Current	I_{CC}	$R_L=\infty$	−	9	14	mA
Power Amp						
Input Bias Current	I_B		−	140	−	nA
Output Offset	$\triangle V_O$	$R_L=8\Omega$	−	0	50	mV
Output Power	Po	THD=10%, f=1kHz, V^+=4V, $R_L=8\Omega$	300	400	−	mW
(Note1)	Po	THD=10%, f=1kHz, V^+=3V, $R_L=4\Omega$	150	220	−	mW
T.H.D.	THD	V^+=4V, $R_L=8\Omega$, P_O=200mV, f=1kHz	−	0.2	−	%
Close Loop V-Gain	A_{V1}	f=1kHz	41	44	47	dB
Equivalent Input Noise Voltage	V_{N1}	$R_S=10k\Omega$, $R_L=4\Omega$, A curve	−	2	−	μVrms
	V_{N2}	$R_S=10k\Omega$, $R_L=4\Omega$, BW=22Hz～22kHz	−	2.5	−	μVrms
Ripple Rejection	RR	f=100Hz	−	47	−	dB
Cut off Frequency	f_H	A_V=−3dB from f=1kHz, $R_L=4\Omega$, P_O=0.1W	−	80	−	kHz
Pre Amp						
Output Voltage	V_O	f=1kHz, THD=1%	0.1	0.2	−	Vrms
Voltage Gain	Av	f=1kHz	35	38	41	dB
Output V-Gain	V_{NO}	$R_S=3.3k\Omega$	−	0.1	0.4	mVrms
ALC						
Limit Level	ALC	f=1kHz	100	200	300	mVrms
Ripple Filter						
Output Voltage	V_O	$R_L=2k\Omega$	V^+−0.24	V^+−0.2	V^+−0.16	V
Ripple Rejection	RR	f=200Hz, C=47μF	40	47	54	dB

(Note 1) at on PC Board

■ TYPICAL APPLICATIONS

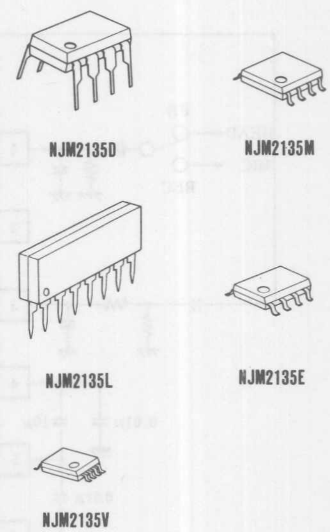


LOW VOLTAGE AUDIO POWER AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2135 is a Low voltage audio power amplifier for speaker drivers. No external coupling capacitors are reguired because of the differential output. The closed loop gain is adjusted by two external resistors. The low supply current in power down mode contributes to the reduction of power consumption of portable batterypowered equipment, cellular phones, for example.

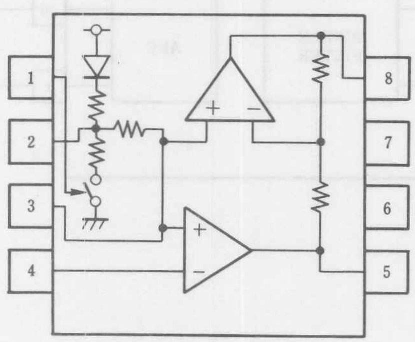
■ PACKAGE OUTLINE



■ FEATURES

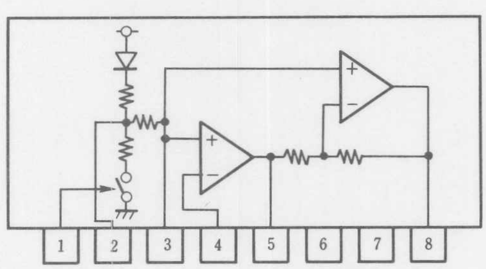
- Operating Voltage — $+2V \sim +16V$
- Low Operating Current in Power Down Mode — $0.1\mu A$ typ.
- Low Operating Current in Normal Operation Mode — 2.7mA typ.
- Output Power Exceeds 250mW — $V^+=6V$, $R_L=32\Omega$
- Gain Range — GVD=$0\sim43$dB, Voice Band
- Load Impedance — $8\sim200\Omega$
- Bipolar Technology
- Package Outline — DIP8, DMP8, EMP8, SIP8, SSOP8

■ PIN CONFIGURATION



NJM2135D
NJM2135M
NJM2135E
NJM2135V

PIN FUNCTION
1. CD
2. V_{REF1}
3. V_{REF2}
4. $-V_{IN}$
5. V_{OUT1}
6. V^+
7. GND
8. V_{OUT2}



NJM2135L

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+2.0～+16	V
Output Peak Current	I_{op}	±250	mA
Maximum Input Voltage	V_{IN}(1-4pin)	−0.3, V^++0.3	V
	V_{IN}(5-8pin)	−0.3, V^++0.3 (In power down)	V
Power Dissipation	P_D	(DIP-8) 500 (SIP-8) 800 (DMP-8) 500 (EMP-8) 500(note1) (SSOP-8) 360(note1)	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

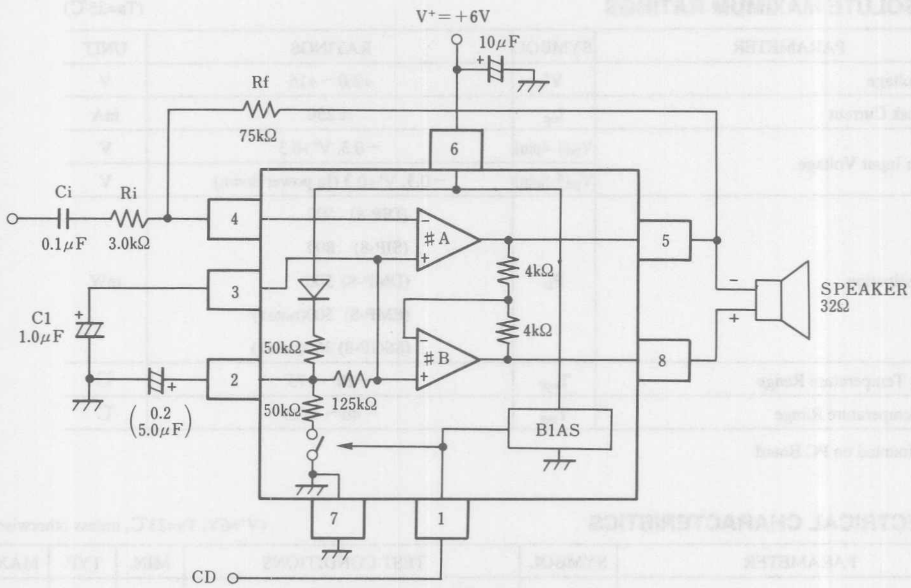
(note) Mounted on PC Board

■ ELECTRICAL CHARACTERISTICS

(V^+=6V, Ta=25℃, unless otherwise specified)

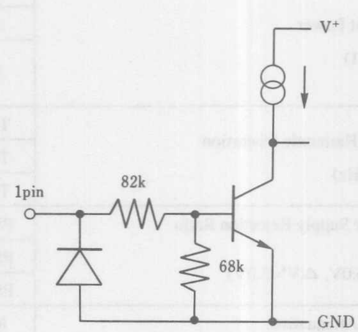
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC1}	V^+=3V, R_L=∞, 1pin=2.0V		2.7	4.0	mA
(NO SIGNAL)	I_{CC2}	V^+=16.0V, R_L=∞, 1pin=2.0V		3.4	5.0	mA
(At Power Down Mode)	I_{CCD}	V^+=3.0V, R_L=∞, 1pin=0.8V		0.1	1.0	μA
Open Loop Gain	AV1	AMP#A, f<100Hz	77	83		dB
Closed Loop Gain	AV2	AMP#B, f=1kHz, R_L=32Ω	−0.35		+0.35	dB
Output Power	Po1	V^+=3.0V, R_L=16Ω, THD≦10%	55			mW
(Note1)	Po2	V^+=6.0V, R_L=32Ω, THD≦10%	250			mW
	Po3	V^+=12.0V, R_L=100Ω, THD≦10% (Note2)	400			mW
Total Harmonic Distortion	THD1	V^+=6V, R_L=32Ω, Po=125mW, G_{VD}=34dB		0.5	1.0	%
(f=1kHz)	THD2	V^+≧3V, R_L=8Ω, Po=20mW, G_{VD}=12dB		0.5		%
	THD3	V^+≧12V, R_L=32Ω, Po=200mW, G_{VD}=34dB		0.6		%
Power Supply Rejection Ratio	PSRR1	C1=∞, C2=0.01μF, DC	50			dB
(V^+=6.0V, △V^+=3.0V)	PSRR2	C1=0.1μF, C2=0, f=1kHz		12		dB
	PSRR3	C1=1.0μF, C2=5.0μF, f=1kHz		52		dB
Mute Attenuation	MAT	f=1kHz～20kHz, 1pin=2.0V		70		dB
Output Voltage	Vo1	V^+=3.0V, R_L=16Ω	1.00	1.15	1.25	V
(R_f=75kΩ, DC)	Vo2	V^+=6.0V		2.55		V
	Vo3	V^+=12.0V		5.45		V
Output High Level	V_{OH}	I_{OUT}=−75mA, V^+=2.0～16.0V		V^+−1.1		V
Output Low Level	V_{OL}	I_{OUT}=75mA, V^+=2.0～16.0V		0.21		V
Output DC Offset	△Vo	R_f=75kΩ, R_L=32Ω, 5pin−8pin	−30	0	+30	mV
Input Bias Current	I_B	4pin		−30	−200	nA
Equivalent Resistance	R_{+IN}	3pin	100	150	220	kΩ
	R_{REF}	2pin	18	25	40	kΩ
CD Input Voltage H	V_{CDH}	1pin	2.0		V^+	V
CD Input Voltage L	V_{CDL}	1pin	0.0		0.8	V
CD Input Resistance	R_{CD}	V^+=V_{CD}=16.0V, 1pin	50	90	175	kΩ

(note1) NJM2135M, NJM2135E, NJM2135V : Mounted on Pc board
(note2) NJM2135V is excluded



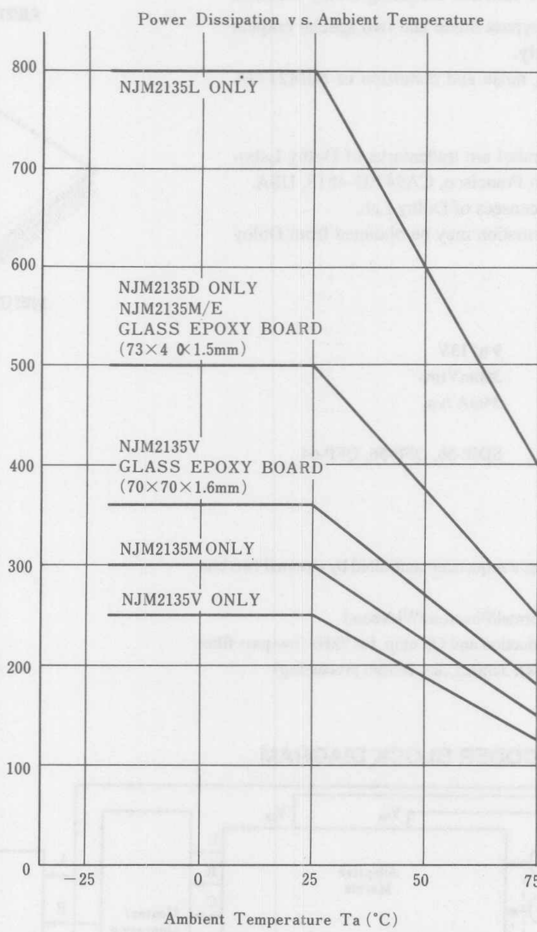
(note)

1. The NJM2135 is active mode during the CD terminal is High level (>2.0V) and it is stand-by mode during the CD terminal is Low level (<0.8V).
2. C1 and C2 improve power supply rejection ratio. In case of C1 is enough large, C2 is unnecessary.
3. Please note that the C1 and C2 make slow power rise up to the NJM2135 regardless the external power supply condition.
4. Input current flow on the internal resistor shown in the equivalent circuit of CD terminal.
5. No sunbber resistor and capacitor are required are required normally. But the snubber resistor and capacitor are required if the NJM2135 oscillates by condition of PCB layout, stray capacitor and speaker wire length.
6. When the NJM2135 change the mode to active or stand-by the CD terminal ON/OFF, the actual operation takes some delay by the charge and discharge of C1,C2.
7. When the power turns on in stand-by mode, the NJM2135 operates during charging time of C1 and C2.
8. If the supply voltage fluctuate large during the stand-by mode, the mode of active and stand-by of NJM2135 becomes unstable.



■ **POWER DISSIPATION**

The allowable power is restricted by the ambiemt temperature. Characterestics of the allowable power (PD:Powe Dissipation) against ambient temperature is indicated below.



DOLBY PRO LOGIC SURROUND DECODER

■ GENERAL DESCRIPTION

The NJM2177 is a higher level integration and high quality audio performance monolithic IC designed for use in Dolby Pro Logic Surround System. The NJM2177 provides all the necessary function for a complete Pro Logic processor except time delay; Automatic input balance, noise sepuencer, adaptibve matrix, center mode control, and modified B-type noise reduction all on chip.

In addition to Dolby Pro Logic function including Dolby 3-stereo, this device provides two channel bypass mode and two special outputs used for other surround conbeniently.

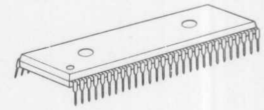
At two channel by pass mode, noise and distortion of NJM2177A are lower than that of NJM2177

(note) Dolby and the double-D symbol are trademarks of Dolby Laboratories Licensing Corporation. San Francisco, CA94103-4813, USA.

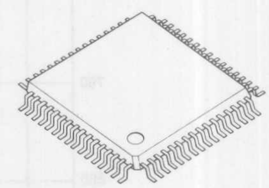
This device available only to licensees of Dolby Lab.

Licensing and application information may be obtained from Dolby Lab.

■ PACKAGE OUTLINE



NJM2177L/2177AL



NJM2177FB3/2177AFB3

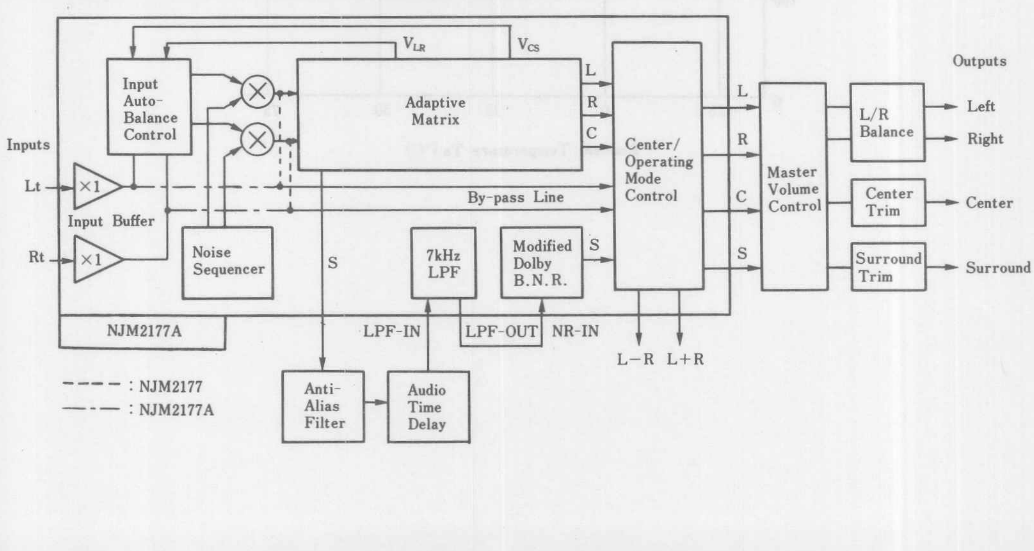
■ FEATURES

- Operating Voltage — 9 to 13V
- Dolby operating level — 300mVrms
- Lower Operating Current — 34mA typ.
- Internal mode control switches
- Package — SDIP-56, QFP-56, QFP-64

■ FUNCTIONS

- Auto input balance and buffer
- Noise sequencer; a Noise generator, a sequencer controlled by external two bits
- Adaptive Matrix
- Center mode control; ON/OFF, Normal/Phantom/Wideband
- Modified Dolby B Type Noise Reduction and OP amp. for 7kHz low-pass filter
- Operating mode control; 4ch(L,C,R), 3ch(L,C,R), 2ch(no processing)
- L+R and L−R output

■ ACTIVE SURROUND DECODER BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(SDIP-56) 700	mW
		(QFP-56) 500	mW
		(QFP-64) 500	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V⁺=12V, 0dB Reference is 300mV/1kHz at C-OUT. Unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Overall						
Operating Voltage Range	V_{OP}		9.0	—	13.0	V
Operating Current	I_{CC}	No signal	—	34.0	40.0	mA
Reference Voltage	V_{ref}	No signal	—	4.0	—	V
Control SW input voltage						
2ch Mode	V_C-2ch	MODE-CNT PIN	0.0	—	0.8	V
3ch	V_C-3ch	MODE-CNT PIN	—	Open	—	
4ch	V_C-4ch	MODE-CNT PIN	3.8	—	7.0	V
Center on	V_C-con	CENTER-CNT PIN	2.4	—	7.0	V
Center off	V_C-coff	CENTER-CNT PIN	0.0	—	0.8	V
Noise Seq. on	V_C-nson	NOISE-CNT-E PIN	0.0	—	0.8	V
Noise Seq. off	V_C-nsoff	NOISE-CNT-E PIN	3.2	—	7.0	V
Noise Seq. channel select H	V_C-nssH	NOISE-CNT-A and NOISE-CNT-B PIN	3.2	—	7.0	V
Noise Seq. channel select L	V_C-nssL	NOISE-CNT-A and NOISE-CNT-B PIN	0.0	—	0.8	V
Modified B Noise Reduction (0dBd Reference is input leve at NR-IN when adjust to 300mV/100Hz at S-OUT)						
Voltage Gain	GV-BNR	V_{in}= 0dBd, f=100Hz	—	9.0	—	dB
Decode Responce 1	D_{ec1}	V_{in}=0dBd, f=1.0kHz	−1.6	−0.1	1.4	dB
2	D_{ec2}	V_{in}=−15dBd, f=1.4kHz	−3.0	−1.5	0.0	dB
3	D_{ec3}	V_{in}=−20dB, f=1.4kHz	−4.9	−3.4	−1.9	dB
4	D_{ec4}	V_{in}=40dBd, f=5.0kHz	−6.8	−5.3	−3.8	dB
T.H.D	THD-NR	V_{in}=0dBd, f=1.0kHz	—	0.07	—	%
Headroom	HR-NR	V⁺=9V AT T.H.D.=1%	15.0	17.0	—	dB
SN Ratio	SN-NR	Rg=0, weighted CCIR/ARM	76	82	—	dB
Noise sequencer						
OUTPUT Noise level	V_{no}		−15	−12.5	−10	dB
Output Noise Level Accuracy relative to Cch Lch Rch S'ch	ΔV_{no}		−0.5	0.0	0.5	dB
Adaptive Matrix						
Output Level Accuracy relative to Cch L,R,S'ch out	ΔVol		−0.5	0.0	0.5	dB
Matrix Rejection relative L,R,C,S'ch out	Mr		25.0	40.0	—	dB
T.H.D L,R,C,S'ch out	THD-AM		—	0.02	—	%
Headroom L,R,C,S'ch out	HR-AM	V⁺=9V at T.H.D=1%	15.0	15.7	—	dB
Signal to Noise Ratio L,R,C,S' ch out	SN-AM	Rg=0, weighted CCIR/ARM	78	83	—	dB
Auto Balance						
Capture Range	CPR		—	±5	—	dB
Error collection	CER		—	±4	—	dB
T.H.D Lt, Rt OUT	THD-AB		—	0.03	—	%
S/N Lt, Rt OUT	SN-AB	Rg=0, weighted CCIR/ARM	78	83	—	dB
Headroom Lt,Rt OUT	HR-AB	V⁺=9V at T.H.D=1%	15.0	17.0	—	dB
L+R & L-R OUTPUT						
Output Level Accuracy relative to Cch L+R, L−R ch	ΔVol-OP		—	0.0	—	dB
T.H.D	THD-OP		—	0.02	—	%
S/N	SN-OP	Rg=0, weighted CCIR/ARM	—	92	—	dB
Headroom	HR-OP	V_{CC}=9V at T.H.D=1%	—	17.0	—	dB

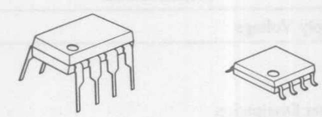
2-INPUT 1-OUTPUT AUDIO SWITCH

■ GENERAL DESCRIPTION

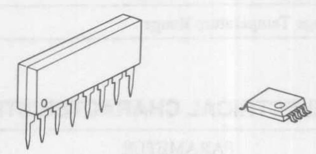
The NJM2520 is 58kΩ input impedance 2-input 1-output audio switch.

It contains two bias-type inputs and one buffer-type output.

■ PACKAGE OUTLINE



NJM2520D　NJM2520M

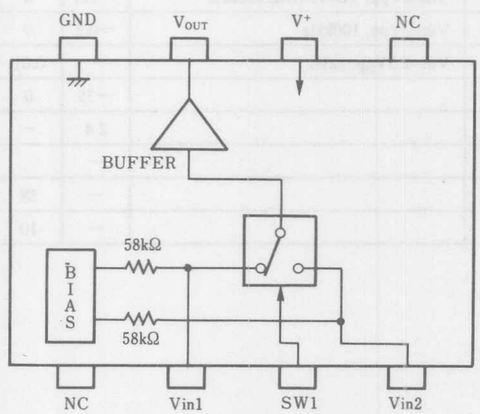


NJM2520L　NJM2520V

■ FEATURES

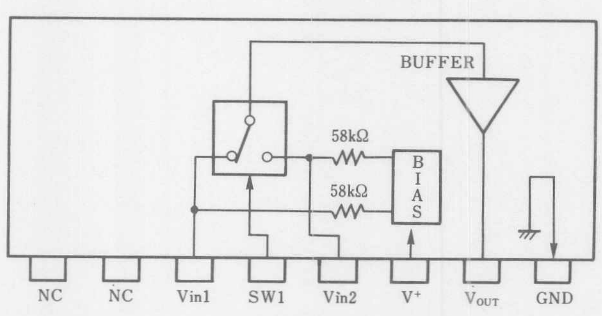
- Operating Voltage　+4.75V～+13V
- Crosstalk　(−70dB typ.)
- Input Impedance　(58kΩ typ.)
- 2-Input, 1-Output
- Bipolar Technology
- Package Outline　DIP8, DMP8, SIP8, SSOP8

■ PIN CONFIGURATION



NJM2520D
NJM2520M
NJM2520V

PIN FUNCTION
1. NC
2. Vin1
3. SW1
4. Vin2
5. NC
6. V^+
7. Vout
8. GND



NJM2520L

PIN FUNCTION
1. NC
2. NC
3. Vin1
4. SW1
5. Vin2
6. V^+
7. Vout
8. GND

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+15	V
Power Dissipation	P_D	(DIP-8) 500 (DMP-8) 300 (SIP-8) 800 (SSOP-8) 250	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		+4.7	−	+13.0	V
Operating Current	I_{CC}		−	8.5	11.0	mA
Frequency Characteristics	G_f	Vin=2Vpp, Vo=10MHz/100kHz	−1.0	0	+1.0	dB
Voltage Gain	G_V	Vin=2Vpp, 100kHz	−0.5	0	+0.5	dB
Total Harmonic Distortion	THD	Vin=2.5Vpp, 1kHz	−	0.01	−	%
Output Offset Voltage	V_{off}		−35	0	+35	mV
Switching Voltage	V_{CH}		2.4	−	−	V
	V_{CL}		−		0.8	V
Input Impedance	R_i		−	58	−	kΩ
Output Impedance	R_o		−	10	−	Ω

3-INPUT 1-OUTPUT AUDIO SWITCH

■ GENERAL DESCRIPTION

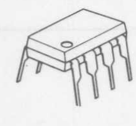
The NJM2521 is 58kΩ input impedance 3-input 1-output audio switch.

It contains two bias-type inputs and one buffer-type output.

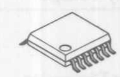
■ FEATURES

● Operating Voltage	+4.75V ~ +13V
● Crosstalk	(−70dB typ.)
● Input Impedance	(58kΩ typ.)
● 3-Input, 1-Output	
● Bipolar Technology	
● Package Outline	DIP8, DMP8, SIP8, SSOP8

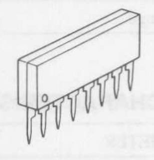
■ PACKAGE OUTLINE



NJM2521D



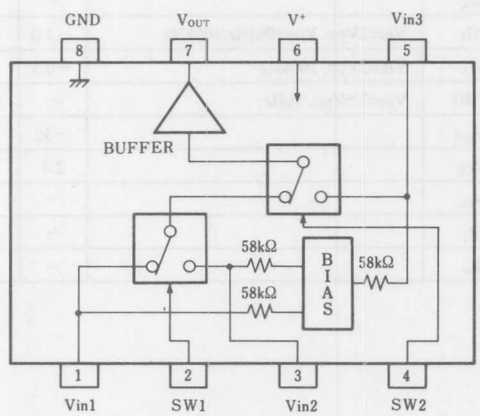
NJM2521M



NJM2521L

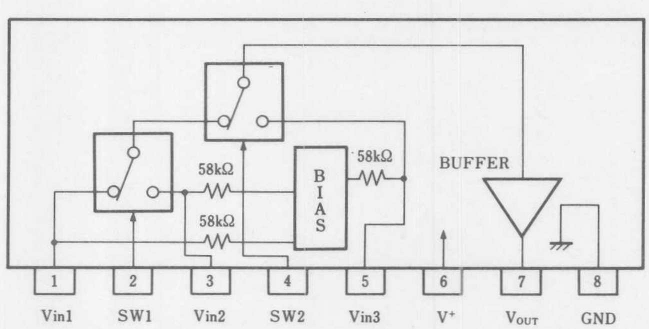
NJM2521V

■ PIN CONFIGURATION



NJM2521D
NJM2521M
NJM2521V

PIN FUNCTION
1. Vin1
2. SW1
3. Vin2
4. SW2
5. Vin3
6. V+
7. Vout
8. GND



NJM2521L

PIN FUNCTION
1. Vin1
2. SW1
3. Vin2
4. SW2
5. Vin3
6. V+
7. Vout
8. GND

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+15	V
Power Dissipation	P_D	(DIP-8) 500 (DMP-8) 300 (SIP-8) 800 (SSOP-8) 250	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		+4.75	−	+13.0	V
Operating Current	I_{CC}		−	11.0	14.5	mA
Frequency Characteristics	G_f	Vin=2Vpp, Vo=10MHz/100kHz	−1.0	0	+1.0	dB
Voltage Gain	G_V	Vin=2Vpp, 100kHz	−0.5	0	+0.5	dB
Total Harmonic Distortion	THD	Vin=2.5Vpp, 1kHz	−	0.03	−	%
Output Offset Voltage	V_{off}		−35	0	+35	mV
Switching Voltage	V_{CH}		2.4	−	−	V
	V_{CL}		−	−	0.8	V
Input Impedance	R_i		−	58	−	kΩ
Output Impedance	R_o		−	10	−	Ω

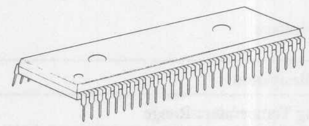
DOLBY PRO LOGIC SURROUND DECODER

■ GENERAL DESCRIPTION

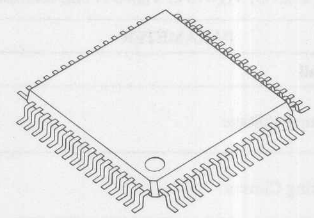
The NJW1102 is a Dolby Pro Logic Surround Decoder including modified Dolby B-Type noise reduction circuit, input auto-balance controller, noise sequenoer, adaptive matrix, center and surround channel level trimmers, serial data interface and others. All of internal status and the balance of surround speakers are controlled by serial data. It performs the complete Dolby Pro Logic Surround function and surround function, such as Hall, Matrix, Simulated and others combine with the digital delay NJU9702.

(Note) Dolby and the double-D symbol are trademakes of Dolby Laboratories Licensing Corporation, San Francisco, CA94103-4813, USA.
This device is available only to licensees of Dolby Lab.
Licensing and application infromation may be obtained from Dolby Lab.

■ PACKAGE OUTLINE



NJW1102L



NJW1102FG1

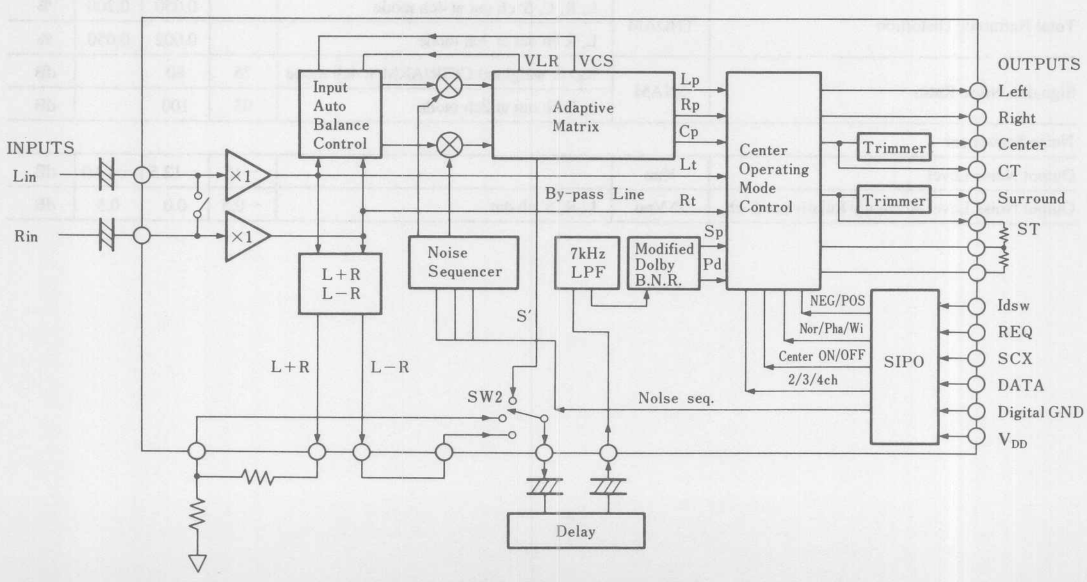
■ FEATURES

- Operating Voltage
  - Analog Block V_{CC}=9−13 or ±5V
  - Digital Block V_{DD}=5V
- Dolby Operating Level 300mVrms
- Center and Surround Channel Level Trimmers
  −15 to +15dB/ 1dB step (−15dB to 3dB/ 1dB step in Pro Logic Mode)
- Internal Mode Control Switch
- Bi-CMOS Technology
- Package Outline TQFP64

■ FUNCTIONS

- Input Auto-Balance
- Noise Generator And Sequencer
- Adaptive Matrix
- Pro Logic Surround Mode Conrtol : 4/3, Center ON/OFF, Normal/Phantom/Wideband
- 7kHz Low-pass Filter and Modified Dolby B Type Noise Reduction
- Center and Surround Channel Level Trimmer
- Other Surround Mode Control : S'Out Selector, Mixer And Mute Functions
- Serial Data Interface

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	13.0	V
	V_{DD}	6.5	V
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

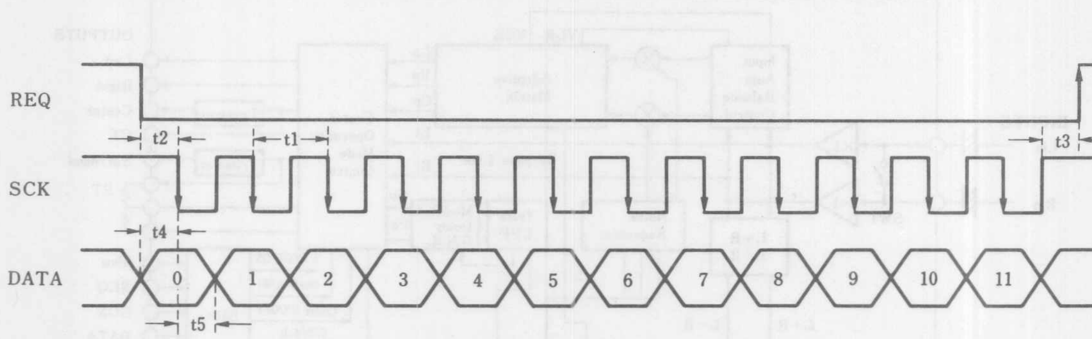
(Ta=25℃, V_{CC}=10V, V_{DD}=5V, 0dB reference is 300mVrms/1kHz at C-OUT with C ch trimmer being 0dB, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Overall						
Operating Voltage	V_{CC}		9	10	13	V
	V_{DD}		4.5	5.0	6.5	V
Operating Current	I_{CC}	No Signal		35	45	mA
	I_{DD}	No Signal		0.6	1.5	mA
Reference Voltage	Vref	No Signal	3.6	4.0	4.4	V
Threshold Voltage	Vthh	Digital Input High Level	$0.7V_{DD}$		V_{DD}	V
	Vthl	Digital Input Low Level	0.0		$0.3V_{DD}$	V
Input short switch						
Resistance at input short	Ron			150	500	Ω
Switch Crosstalk	SC	Vin=0dB, f=1kHz, Rm=600Ω		−100		dB
Input Auto Balance						
Capture Range	CPR			±5		dB
Error Correction	CER			±4		dB
Adaptive Matrix						
Output Level Accuracy Relative to C ch	△Vol	L, R, S' ch out	−0.5	0.0	0.5	dB
Matrix Rejection Relative	MR	L, R, C, S' ch out	25	40		dB
Headroom	HRAM	V_{CC}=9V at THD=1%	15	17		dB
Total Harmonic Distortion	THDAM	L, R, C, S' ch out at 4ch mode		0.050	0.200	%
		L, R ch out at 2ch mode		0.002	0.050	%
Signal to Noise Ratio	SNAM	Rg=0, weighted:CCIR/ARM at 4ch mode	75	80		dB
		L, R ch out at 2ch mode	93	100		dB
Noise Sequencer						
Output Noise Level	Vno		−15	−12.5	−10.0	dB
Output Noise Level Accuracy Relative to C ch	△Vno	L, R, S' ch out	−0.5	0.0	0.5	dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Modified Noise B Type Noise Reduction						
(0dBd reference is input level at NR-IN when S out is adjusted to 0dB (300mVrms/100Hz) with S ch trimmer level being 0dB)						
Voltage Gain	VGNR	Vin=0dBd, f=100Hz		9.5		dB
Decode Response 1	DEC1	Vin=0dBd, f=1.0kHz	−1.6	−0.1	1.4	dB
Decode Response 2	DEC2	Vin=−15dBd, f=1.4kHz	−3.0	−1.5	0.0	dB
Decode Response 3	DEC3	Vin=−20dBd, f=1.4kHz	−4.9	−3.4	−1.9	dB
Decode Response 4	DEC4	Vin=−40dBd, f=5.0kHz	−6.8	−5.3	3.8	dB
Total Harmonic Distortion	THDNR	Vin=0dBd, f=1kHz		0.070	0.300	%
Headroom	HRNR	Vin=9V at THD=1%	15	17		dB
Signal to Noise	SNNR	Rg=0, weighted : CCIR/ARM	73	78		dB
Other Surround						
Total Harmonic Distortion	THDOS	Vin=0dB, f=1kHz L+R, L−R Output		0.050	0.200	%
Headroom	HROS	V_{CC}=9V at THD=1% L+R, L−R Output	15	17		dB
Signal to Noise Ratio	SNOS	Rg=0, weighted : CCIR/ARM L+R, L−R Output	75	80		dB
Adder Gain	AG			0		dB
C.S Channel Trimmer						
Full Scale	FS	Digital Input=+15 or −15dB	+12	±15	±18	dB
Gain Accuracy at −6dB		Digital Input=−6dB	−7	−6	−5	dB
Non Linearity (Note 1)	NL	Digital Input=±1, 2, 4, 8dB	−0.5	0.0	0.5	dB
Control Timing						
SCK Clock Width	t1	SCK	50			μS
REQ Set-up Time	t2	REQ-SCK	25			μS
REQ Hold Time	t3	REQ-SCK	25			μS
Data Set-up Time	t4	SCK-DATA	25			μS
Data Hold Time	t5	SCK-DATA	25			μS

(Note 1) NL=A·B/D−C
A : Measured gain value in full scale
B : Digital input value
C : Measured gain value of digital input
D : Full scale value

(Note 2) Control Timing



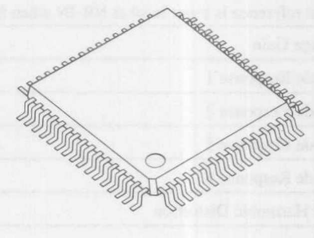
DOLBY PRO LOGIC SURROUND DECODER

■ GENERAL DESCRIPTION

The NJW1102A is a Dolby Pro Logic Surround Decoder including modified Dolby B-Type noise reduction circuit, input auto-balance controller, noise sequenoer, adaptive matrix, center and surround channel level trimmers, serial data interface and others. All of internal status and the balance of surround speakers are controlled by serial data. It performs the complete Dolby Pro Logic Surround function and surround function, such as Hall, Matrix, Simulated and others combine with the digital delay NJU9702.

(Note) Dolby and the double-D symbol are trademakes of Dolby Laboratories Licensing Corporation, San Francisco, CA94103-4813, USA.
This device is available only to licensees of Dolby Lab.
Licensing and application infromation may be obtained from Dolby Lab.

■ PACKAGE OUTLINE



NJW1102AF1

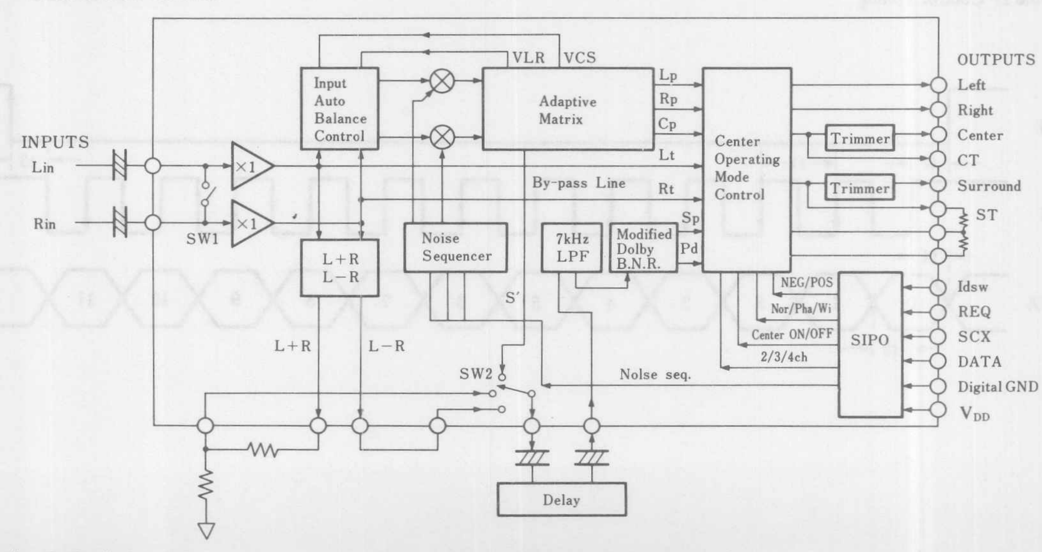
■ FEATURES

- Operating Voltage
  - Analog Block V_{CC}=9−13 or ±5V
  - Digital Block V_{DD}=5V
- Dolby Operating Level 300mVrms
- Center and Surround Channel Level Trimmers
  −31 to +0dB/ 1dB step (0dB=Dloby Level)
- Internal Mode Control Switch
- Bi-CMOS Technology
- Package Outline SDIP56, TQFP64

■ FUNCTIONS

- Input Auto-Balance
- Noise Generator And Sequencer
- Adaptive Matrix
- Pro Logic Surround Mode Conrtol : 4/3, Center ON/OFF, Normal/Phantom/Wideband
- 7kHz Low-pass Filter and Modified Dolby B Type Noise Reduction
- Center and Surround Channel Level Trimmer
- Other Surround Mode Control : S'Out Selector, Mixer And Mute Functions
- Serial Data Interface
- Optional Digital Outputs AUX1, AUX2

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	13.0	V
	V_{DD}	6.5	V
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

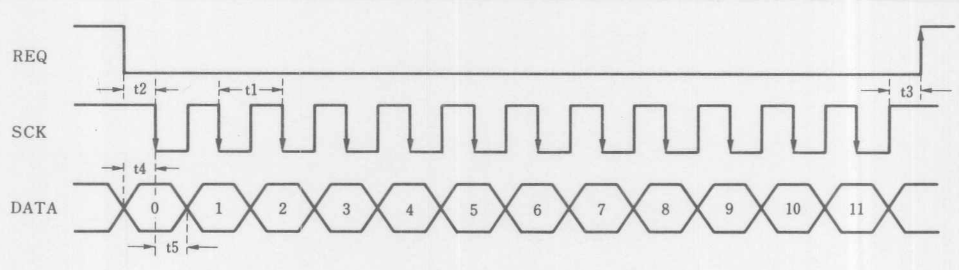
(Ta=25℃, V_{CC}=10V, V_{DD}=5V, 0dB reference is 300mVrms/1kHz at C-OUT with C ch trimmer being 0dB, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Overall						
Operating Voltage	V_{CC}		9	10	13	V
	V_{DD}		4.5	5.0	6.5	V
Operating Current	I_{CC}	No Signal		35	45	mA
	I_{DD}	No Signal		0.6	1.5	mA
Reference Voltage	Vref	No Signal	3.6	4.0	4.4	V
Threshold Voltage	Vthh	Digital Input High Level	$0.7V_{DD}$		V_{DD}	V
	Vthl	Digital Input Low Level	0.0		$0.3V_{DD}$	V
Input Auto Balance						
Capture Range	CPR			±5		dB
Error Correction	CER			±4		dB
Adaptive Matrix						
Output Level Accuracy Relative to C ch	△Vol	L, R, S' ch out	−0.5	0.0	0.5	dB
Matrix Rejection Relative	MR	L, R, C, S' ch out	25	40		dB
Headroom	HRAM	V_{CC}=9V at THD=1%	15	17		dB
Total Harmonic Distortion	THDAM	L, R, C, S' ch out at 4ch mode		0.050	0.200	%
		L, R ch out at 2ch mode		0.002	0.050	%
Signal to Noise Ratio	SNAM	Rg=0, weighted:CCIR/ARM at 4ch mode	75	80		dB
		L, R ch out at 2ch mode	93	100		dB
Noise Sequencer						
Output Noise Level	Vno		−15	−12.5	−10.0	dB
Output Noise Level Output Noise Level Accuracy Relative to C ch	△Vno	L, R, S' ch out	−0.5	0.0	0.5	dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Modified Noise B Type Noise Reduction						
(0dBd reference is input level at NR-IN when S out is adjusted to 0dB (300mVrms/100Hz) with S ch trimmer level being 0dB)						
Voltage Gain	VGNR	Vin=0dBd, f=100Hz		9.0		dB
Decode Response 1	DEC1	Vin=0dBd, f=1.0kHz	−1.6	−0.1	1.4	dB
Decode Response 2	DEC2	Vin=−15dBd, f=1.4kHz	−3.0	−1.5	0.0	dB
Decode Response 3	DEC3	Vin=−20dBd, f=1.4kHz	−4.9	−3.4	−1.9	dB
Decode Response 4	DEC4	Vin=−40dBd, f=5.0kHz	−6.8	−5.3	3.8	dB
Total Harmonic Distortion	THDNR	Vin=0dBd, f=1kHz		0.070	0.300	%
Headroom	HRNR	Vin=9V at THD=1%	15	17		dB
Signal to Noise	SNNR	Rg=0, weighted : CCIR/ARM	73	78		dB
Other Surround						
Total Harmonic Distortion	THDOS	Vin=0dBd, f=1kHz L+R, L−R Output		0.050	0.200	%
Headroom	HROS	V_{CC}=9V at THD=1% L+R, L−R Output	15	17		dB
Signal to Noise	SNOS	Rg=0, weighted : CCIR/ARM L+R, L−R Output	75	80		dB
Adder Gain	AG			0		dB
C.S Channel Trimmer						
Full Scale	FS	Digital Input= −31dB	−34	−31	−28	dB
Non Linearity (Note 1)	NL	Digital Input=−1, −2, −4, −8, −16dB	−0.5	0.0	0.5	dB
Optional Digital Output (AUX1, AUX2)						
Low Level Voltage	VOL	Sink Current=0.8mA, V_{DD}=5V		0.6	1.0	V
High Level Voltage	VOH	Source Current=0.5mA, V_{DD}=5V	3.5	4.0		V
Control Timing						
SCK Clock Width	t1	SCK	50			μS
REQ Set-up Time	t2	REQ-SCK	25			μS
REQ Hold Time	t3	REQ-SCK	25			μS
Data Set-up Time	t4	SCK-DATA	25			μS
Data Hold Time	t5	SCK-DATA	25			μS

(Note 1) NL=A·B/D−C
A : Measured gain value in full scale
B : Digital input value
C : Measured gain value of digital input
D : Full scale value

(Note 2) Control Timing



SINGLE CHIP DIGITAL DELAY IC

■ GENERAL DESCRIPTION

NJU9702 is a single chip digital delay LSI designed for Dolby Prologic or other types surround processor.

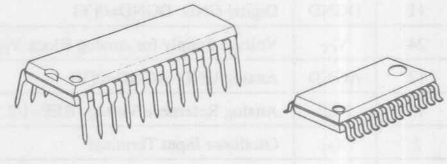
It consists of 16k SRAM, input/output filter, A/D D/A converters and control logic.

The A/D and D/A converter is using a ADM (Adaptive Delta Modulation) method. Consequntly, it is realized low noise and low distortion.

The delay time can select from 64 mode of 0.5ms to 32.8ms in 0.5ms step, according to the application.

Furthermore, the NJU9702 has a sleep mode, mute function, and power on initialization function which perform low current consumption in the sleep mode, muting on/off control and power on initialization.

■ PACKAGE OUTLINE

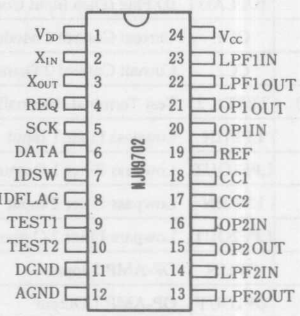


NJU9702D NJU9702G

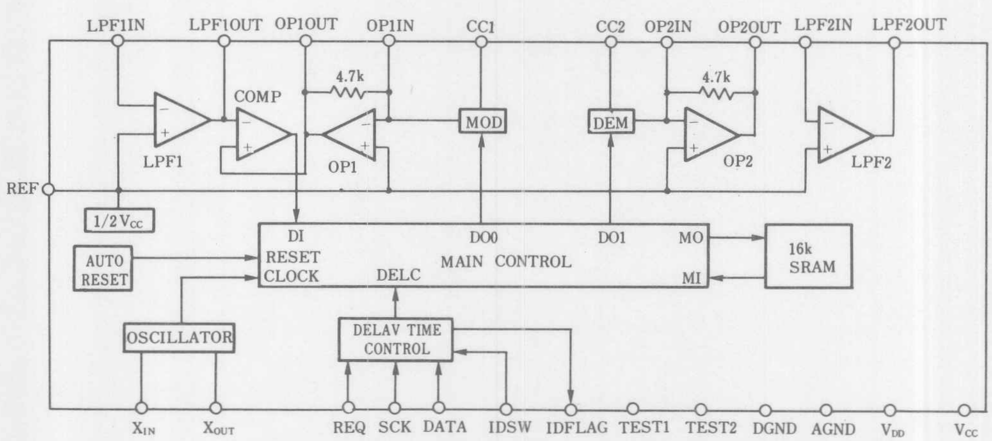
■ FEATURES

- ADM (Adaptive Delta Modulation) Method A/D and D/A Converter
- Low Noise and Low Distortion (No=95[dBV] TYP., THD=0.2[%] TYP.)
- 64 Delay Time Modes From 0.5ms To 32.8ms In 0.5ms step
- Low Current Consumption In Sleep Mode
- Input/Output Filter Built-in (Required External CR)
- A/D, D/A Converter Built-in (Required External CR)
- 16K SRAM (Internal)
- Power on initialization
- Oscillation Circuit
- Package Outline DIP24, SOP24
- C-MOS Technology

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

<table>
<tr><th>NO.</th><th>SYMBOL</th><th colspan="3">FUNCTIONS</th></tr>
<tr><td>1</td><td>V_{DD}</td><td colspan="3">Voltage Supply for Digital Block V_{DD}=5[V]</td></tr>
<tr><td>11</td><td>DGND</td><td colspan="3">Digital GND DGND=0[V]</td></tr>
<tr><td>24</td><td>V_{CC}</td><td colspan="3">Voltage Supply for Analog Block V_{CC}=5[V]</td></tr>
<tr><td>12</td><td>AGND</td><td colspan="3">Analog GND AGND=0[V]</td></tr>
<tr><td>19</td><td>REF</td><td colspan="3">Analog Refernece Voltage REF=1/2 · V_{CC}</td></tr>
<tr><td>2</td><td>X_{IN}</td><td colspan="3">Oscillator Input Terminal</td></tr>
<tr><td>3</td><td>X_{out}</td><td>Oscillator Output Terminal</td><td colspan="2" rowspan="2">Connects to 2MHz ceramic Oscillator</td></tr>
<tr><td>4</td><td>REQ</td><td>Data Request Input Terminal</td></tr>
<tr><td>5</td><td>SCK</td><td colspan="3">Serial Data Shift Clock Input Terminal</td></tr>
<tr><td>6</td><td>DATA</td><td colspan="3">Serial Data Input Terminal</td></tr>
<tr><td>7</td><td>IDSW</td><td colspan="3">ID Switch (ID Code When Connect to the Common Bus)</td></tr>
<tr><td>8</td><td>IDFLAG</td><td colspan="3">ID Flag (Data Input Confirmation and Serial Data Output)</td></tr>
<tr><td>18</td><td>CC1</td><td>Current Control 1 Modulator</td><td colspan="2" rowspan="2">ADM Controller</td></tr>
<tr><td>17</td><td>CC2</td><td>Current Control 2 Demodulator</td></tr>
<tr><td>9, 10</td><td>TEST1, 2</td><td colspan="3">Test Terminal (Normally Connects to the GND)</td></tr>
<tr><td>23</td><td>LPF1IN</td><td>Lowpass Filter 1 Input</td><td rowspan="2">Input Side</td><td rowspan="4">Constitute a Lowpass Filter with external C and R.</td></tr>
<tr><td>22</td><td>LPF1OUT</td><td>Lowpass Filter 1 Output</td></tr>
<tr><td>14</td><td>LPF2IN</td><td>Lowpass Filter 2 Input</td><td rowspan="2">Output Side</td></tr>
<tr><td>13</td><td>LPF2OUT</td><td>Lowpass Filter 2 Output</td></tr>
<tr><td>20</td><td>OP1IN</td><td>OP-AMP 1 Input</td><td rowspan="2">Input Side</td><td rowspan="4">Constitute a Integrator with external C.</td></tr>
<tr><td>21</td><td>OP1OUT</td><td>OP-AMP 1 Output</td></tr>
<tr><td>16</td><td>OP2IN</td><td>OP-AMP 2 Input</td><td rowspan="2">Output Side</td></tr>
<tr><td>15</td><td>OP2OUT</td><td>OP-AMP 2 Output</td></tr>
</table>

■ FUNCTION DESCRIPTION

The sampling frequency (fs) is 500KHz when master clock frequency is 2MHz.

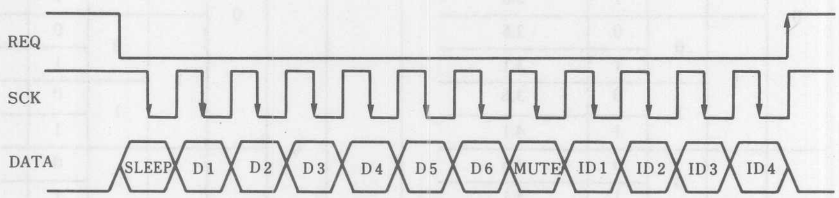
1)Data Format and Setting

The delay time is set by serial data.

The serial data is written into the NJU9702 sincronized by falling edge of shift clock (SCK) and the last 12 bit is effective before the data request (REQ) rising edge.

The time chart of serial data input is shown as fallows.

In order to avoid the shock noise output at the delay time setting, mute function using is recommended.



(note1)

When the corresponding DATA of ID code (refer 5) input to the NJU9702 during the REQ signal is " High", the DATA changed because of the NJU9702 always loading the latest 12-bit data.

Therefore following three operation methods are required when serial data input.

a)Fix the DATA terminal to " High" or "Low" except data setting period.

b)Fix the REQ terminal to "Low" except data setting period.

c)Fix the SCK terminal to " High" or "Low" after 12-bit data input.

(note2)

To use the mute after setting the delay time to avoided the shock noise.

2)Sleep Mode Setting

The sleep mode can be set by writing the code "1" (H level) to the Sleep bit of the serial data.

The sleep mode performs ① output muting, ② stop the internal clock, ③ stop the memory operation and put a low current consumption mode. Normally, this Sleep bit must be "0" (L level).

In order to avoid the shock noise output when the sleep mode released, mute function using is recommended.

SLEEP	MODE	FUNCTIONS
0	NORMAL	Normal operation
1	SLEEP	①Output Muting ② Stop the Internal Clock ③ Stop the Memory Operation

3)Delay Time Setting

64 kind of delay time from 0.5ms to 32.8ms in 0.5ms is set by D1 to D6 of the serial data.

D6	D5	D4	D3	D2	D1	Delay T.
0	0	0	0	0	0	0.5
					1	1.0
				1	0	1.5
					1	2.0
			1	0	0	2.6
					1	3.1
				1	0	3.6
					1	4.1
		1	0	0	0	4.6
					1	5.1
				1	0	5.6
					1	6.1
			1	0	0	6.7
					1	7.2
				1	0	7.7
					1	8.2
	1	0	0	0	0	8.7
					1	9.2
				1	0	9.7
					1	10.2
			1	0	0	10.8
					1	11.3
				1	0	11.8
					1	12.3
		1	0	0	0	12.8
					1	13.3
				1	0	13.8
					1	14.3
			1	0	0	14.8
					1	15.4
				1	0	15.9
					1	16.4
1	0	0	0	0	0	16.9
					1	17.4
				1	0	17.9
					1	18.4
			1	0	0	18.9
					1	19.5
				1	0	20.0
					1	20.5
		1	0	0	0	21.0
					1	21.5
				1	0	22.0
					1	22.5
			1	0	0	23.0
					1	23.6
				1	0	24.1
					1	24.6
	1	0	0	0	0	25.1
					1	25.6
				1	0	26.1
					1	26.6
			1	0	0	27.1
					1	27.6
				1	0	28.2
					1	28.7
		1	0	0	0	29.2
					1	29.7
				1	0	30.2
					1	30.7
			1	0	0	31.2
					1	31.7
				1	0	32.3
					1	32.8

4)Mute Setting

The mute mode can be set by writing the code "1" (H level) to the Mute bit of the serial data. Normally, this Mute bit must be "0" (L level).

MUTE	MODE	FUNCTIONS
0	NORMAL	Normal operation
1	SLEEP	Output Muting

5)ID Code Setting

The access froms the controller (CPU) is recognized the ID code input. It is useful when the NJU9702 connect the common bus togather with other LSI (s). The IDSW can select the prefixed ID code. If the other LSI using the ID code system and setting the same code already, please select other code by using this SW (IDSW).

CONDITIONS	CODE SELECTION TERM.	ID CODE			
	IDSW	ID1	ID2	ID3	ID4
1	0	0	0	1	0
2	1	0	0	1	1

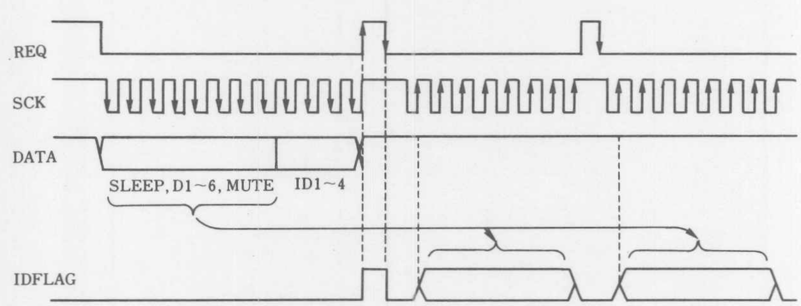
(note) ID code input except mentiond above, the NJU9702 can not be receive any data. In this case, the NJU9702 stil keeping the condition input before.

6)IDFLAG

IDFLAG is terminal to check the setting of delay time and the setting conditions.

When the serial data is received by the NJU9702, the IDFLAG terminal output "H" level for controller (CPU)'s confermation.

After serial data writting, except the ID code (Sleep, D1 to D6, and Mute) can read out for checking. When the read out, ① set the "L" level of the request signal (REQ), ② input the clock signal are required, The data is output syncronized by the rising edge of the clock signal. The ID code can not read out even if over 8 clock input.

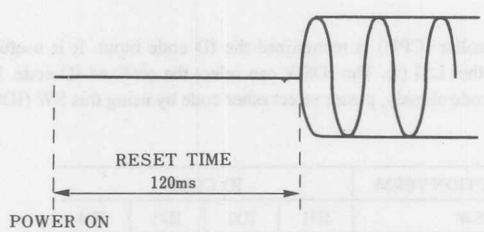


7)Reset Function

NJU9702 performs power-on-initialization when turn on the power. After 120ms pased the turn at the condition of V_{CC}=5V, Capacitor connecting to the REF terminal=4.7 μF, it is released automatically. The 20.0ms delay time is set by the power-on-initialization.

The reset period of NJU9702 depends on an on-chip resistance "R" and a capacitor connected REF terminal. Next expression can compute the reset time.

Reset Time=2.5×C (μF)



Condition : V_{CC}=5V, C=4.7 μF (REF terminal)

(REMARKS)

The NJU9702 needs to work a MUTE function for interruption that shock noise occurs when RESET is released.

The NJU9702 needs to supply a power to V_{DD} in adavance or at the mean time with other power source V_{CC}. If a power supplying sequence is not performed correctly, then power-on-initialization dose not work correctly.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	6.5	V
	V_{CC}	6.5	V
Operating Current	I_{CC}	100	mA
Power Dissipation	P_D	500	mV
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

(note) V_{DD} should be rise up before V_{CC} or same time. Otherwise power-on-initialization may not be operate corectly.

■ RECOMMENDED OPERATING CONDITIONS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_{DD}		4.5	5.0	5.5	V
	V_{CC}		4.5	5.0	5.5	V
Clock Frequency	f_{ck}			2.0		MHz
Input Voltage "H"	V_{IH}		$0.7V_{DD}$		V_{DD}	V
Input Voltage "L"	V_{IL}		0	−	$0.3V_{DD}$	V
Sirial Clock	f_{sck}		−	−	4.0	MHz

■ ELECTRICAL CHARACTERISTICS

(V_{DD}=V_{CC}=5V,f=1kHz, V_O=200mVrms, Ta=25℃)

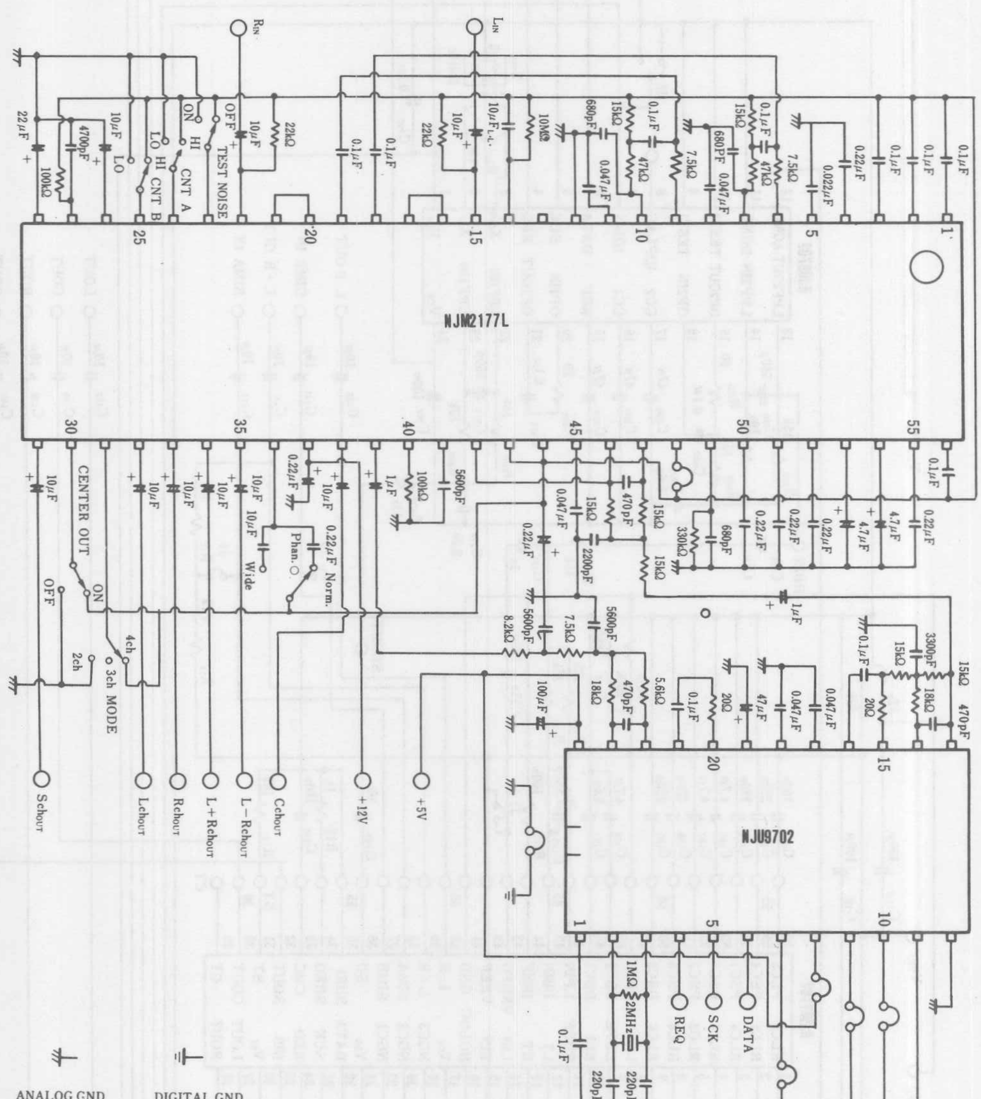
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	No Signal	−	16	35	mA
Voltage Gain	G_V	R_L=47KΩ	−3.5	−0.5	2.5	dB
Max. Output Voltage	Vo_{max}	THD=10%	0.7	1	−	Vrms
Output Distortion	THD	30kHz LPF	−	0.2	1.0	%
Output Noise Voltage	No	DIN-AUDIO	−	−95	−75	dBV
Supply Voltage Rejc. Ratio	SVRR	V_{CC}=20dBV, f=100Hz	−	−40	−25	dB
Frequency Characteristics	f	−3dB, V_O=100mVrms	−	7	−	kHz

■ SERIAL DATA TIMING

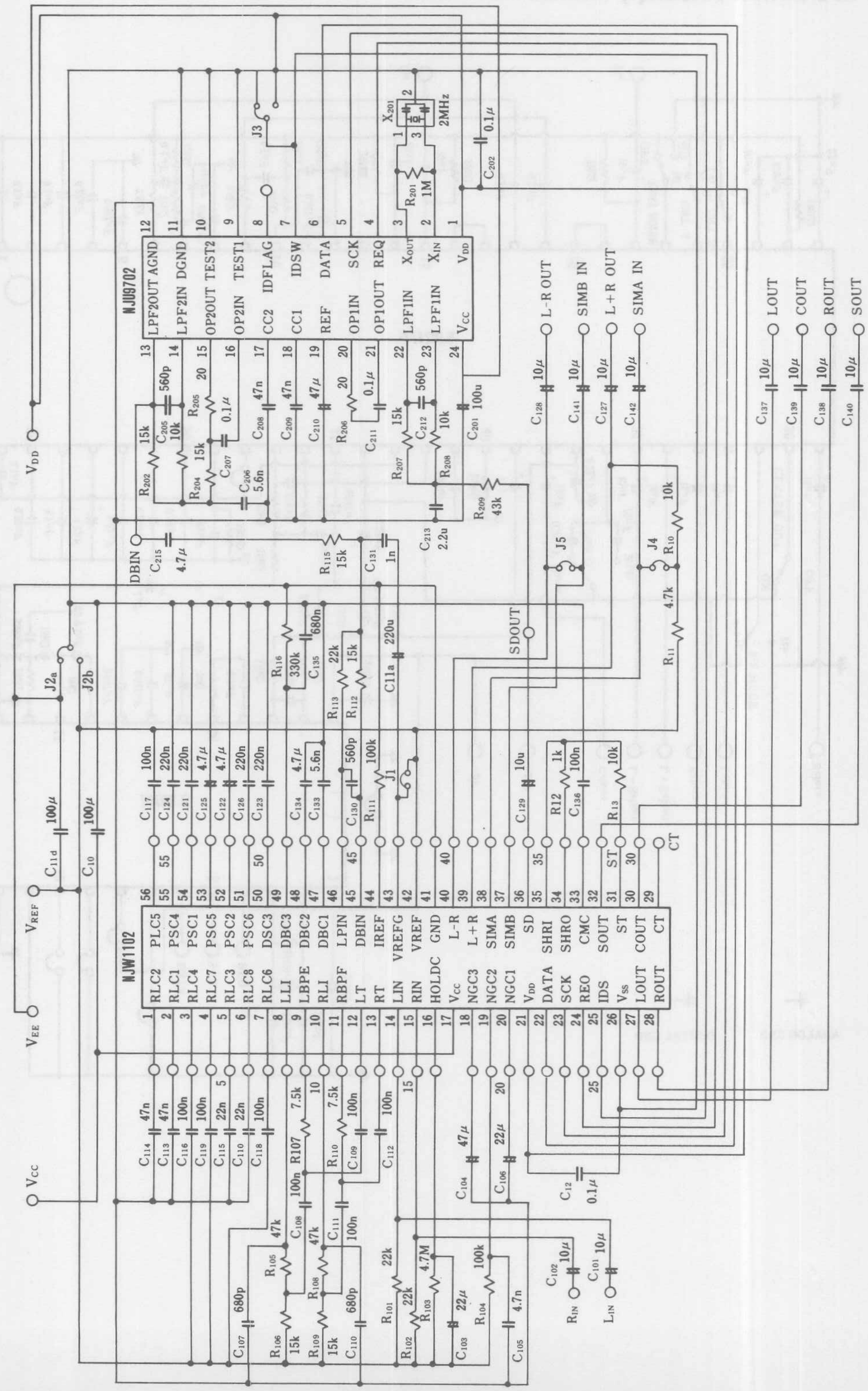
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
SCK Clock Width	t1	250	—	—	ns
SCK Duty	ds	40	50	60	%
Data Set-up Time	t2	100	t1/2	—	ns
Data Hold Time	t3	100	t1/2	—	ns
REQ Hold Time	t4	100	—	—	ns
REQ "H" Pulse Width	t5	100	—	—	ns
SCK Set-up Time	t6	100	—	—	ns

■ TIMING CHART

■ **APLICATION CIRCUIT(1)** (Combined with NJM2177)



■ APLICATION CIRCUIT(2) (Combined with NJW1102)



VIDEO

5

NJRC		EQUVALENT PRODUCTS BY OTHER COMPANIES		
FUNCTIONS	TYPES	MITSUMI	ROHM	OTHERS
VIDEO AMPLIFIER	NJM592D			NE592N14
	NJM592M			NE592DH
	NJM592D8			NE592N8
	NJM592M8			NE592DE
	NJM2267D			
	NJM2267M			
	NJM2267V			
	NJM2268D			
	NJM2268M			
	NJM2268V			
VIDEO SWITCH	NJM2233BD	LVA521D		
	NJM2233BM	LVA521F		
	NJM2233BL	LVA521S *[1]	BA7001	
	NJM2234D	LVA522D		
	NJM2234M	LVA522F		
	NJM2234L	LVA522S *[1]		
	NJM2235D	LVA523D		
	NJM2235M	LVA523F		
	NJM2235L	LVA523S *[1]		
	NJM2243D	LVA524D		
	NJM2243M	LVA524F		
	NJM2243L	LVA524S *[1]		
	NJM2244D	LVA525D		
	NJM2244M	LVA525F		
	NJM2244L	LVA525S *[1]		
	NJM2245D	LVA526D		
	NJM2245M	LVA526F	BN7611N	
	NJM2245L	LVA526S *[1]		
	NJM2246D			
	NJM2246M		BA7611AN	
	NJM2246L		BA7021	
	NJM2273S		BA7602	
	NJM2279D		BA7602F	
	NJM2279M		BA7609	
	NJM2283D		BA7609F	
	NJM2283M		BA7607	
	NJM2284D		BA7607F	
	NJM2284M		BA7603	
	NJM2285D		BA7603F	
	NJM2285M			
	NJM2286D			
	NJM2286M			
	NJM2293D			
	NJM2293M			
	NJM2503D			
	NJM2503M			
	NJM2506D			
	NJM2506M			
	NJM2508D			
	NJM2508M			
	NJM2533D	LVA521D		
	NJM2533M	LVA521F		
	NJM2533L	LVA521S *[1]	BA7001	
	NJM2533V			
	NJM2534D	LVA522D		
	NJM2534M	LVA522F		
	NJM2534L	LVA522S *[1]		
	NJM2534V			
	NJM2535D	LVA523D		
	NJM2535M	LVA523F		
	NJM2535L	LVA523S *[1]		
	NJM2535V			
MODULATOR	NJM1372AD			MC1372
	NJM2208D			

NJRC			EQUVALENT PRODUCTS BY OTHER COMPANIES		
FUNCTIONS		TYPES	MITSUMI	ROHM	OTHERS
FREQUENCY MULTIPLIER		NJM2228D NJM2228M NJM2228S NJM2238D NJM2238M NJM2238S NJM2240D NJM2240M NJM2240S			
SUPER INPORSER		NJM2247AM NJM2247BM NJM2248D NJM2248M NJM2248L NJM2249D NJM2249M NJM2249L NJM2256M NJM2262M NJM2263D NJM2263M NJM2263L NJM2264D NJM2264M NJM2264L NJM2265D NJM2265M NJM2265L NJM2266D NJM2266M NJM2266L NJM2509V			
SYNCHRONOUS SIGNAL		NJM2220S NJM2229M NJM2229S NJM2230M NJM2257D NJM2257M			
OTHERS	ADDER	NJM2207D NJM2207M NJM2207S NJM2217D NJM2217L			
	NOISE REDUCER	NJM2210D NJM2210M NJM2224M			
	ON SCREEN DISPLAY	NJM2214L NJM2252L			
	AUTO IRIS	NJM2225M NJM2225S			
	PICTURE ENHANCER	NJM2209M NJM2209S			
	HUE TINP CONTROLLER	NJM2255D			
	EQUALIZER	NJM2258L			

VIDEO AMPLIFIER

■ GENERAL DESCRIPTION

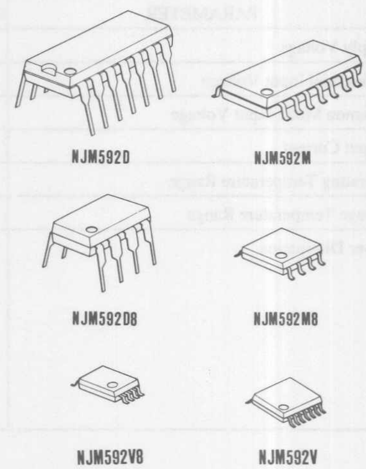
The NJM592 is a video amplifier of differential input and differential output.

The NJM592 is suitable for a preamplifier of memory equipment and video and pulse signal amplifier.

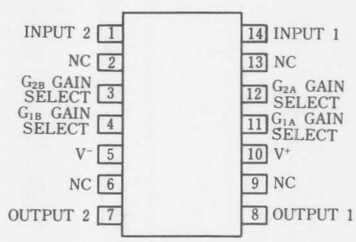
■ FEATURES

- Operating Voltage (±3V∼±8V)
- Wide Fregueney Range (40MHz, 90MHz typ.)
- Differential Input, Differential Output.
- With Gain Select Terminal
- Package Outline DIP 8/14, DMP8/14, SSOP 8/14 .
- Bipolar Technology

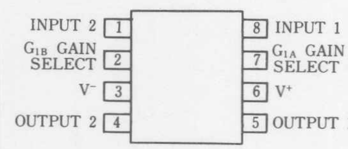
■ PACKAGE OUTLINE



■ PIN CONFIGURATION

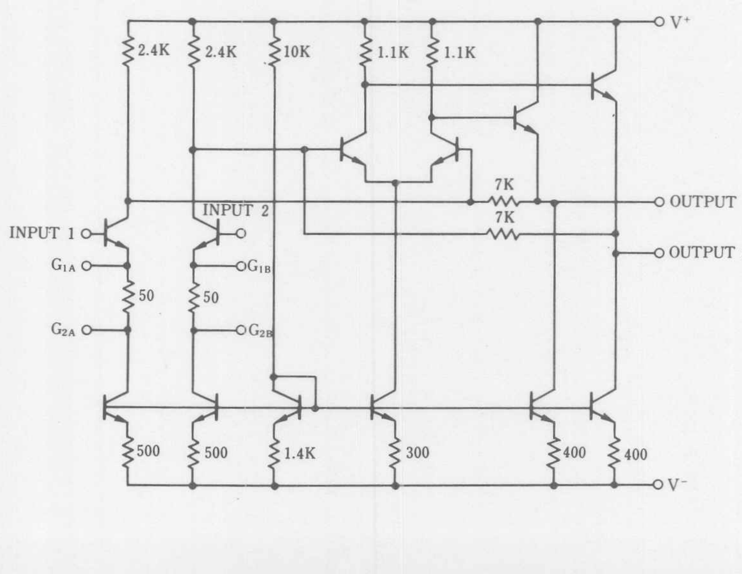


NJM592D
NJM592M
NJM592V



NJM592D8
NJM592M8
NJM592V8

■ EQUIVALENT CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+/V^-	±8	V
Differential Input Voltage	V_{DIEF}	±5	V
Common Mode Input Voltage	V_{CM}	±6	V
Output Current	I_O	10	mA
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃
Power Dissipation	P_D	(DIP14) 500	mW
		(DMP14) 300	mW
		(SSOP14) 300	mW
		(DIP8) 500	mW
		(DMP8) 300	mW
		(SSOP8) 250	mW

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, $V^{+}=\pm 6V$, $V_{CM}=0$)

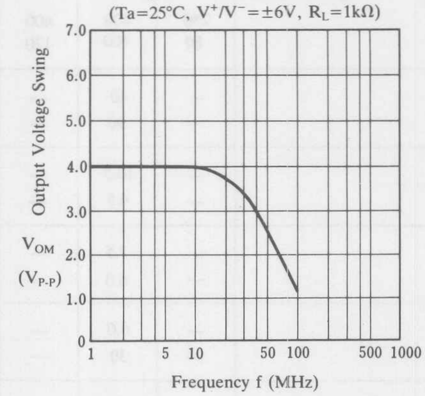
PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Differential Voltage Gain1 (note 1) Differential Voltage Gain2 (note 2, 4)	$R_L=2k\Omega$, $V_{OUT}=3V_{P-P}$	250 80	400 100	600 120	V/V
Bandwidth Gain1 (note 1) Bandwidth Gain2 (note 2,4)		— —	40 90		MHz
Rise Time Gain1 (note 1) Rise Time Gain2 (note 2,4)	$V_{OUT}=1V_{P-P}$	— —	10.5 4.5	 —	ns
Propagation Delay Gain1 (note 1) Propagation Delay Gain2 (note 2,4)	$V_{OUT}=1V_{P-P}$	— —	7.5 6.0	— —	ns
Input Resistance Gain1 (note 1) Input Resistance Gain2 (note 2,4)		— —	4.0 30	— —	kΩ
Input Capacitance Gain2 (note 2,4)		—	2.0	—	pF
Input Offset Current		—	0.4	5.0	μA
Input Bias Current		—	9.0	30	μA
Input Noise Voltage	BW=1kHz~10MHz	—	12	—	μVrms
Input Voltage Range		—	—	±1.0	V
Common Mode Rejection Ratio Gain2 (note 4) Common Mode Rejection Ratio Gain2 (note 4)	$V_{CM}=\pm 1V$, f<100kHz $V_{CM}=\pm 1V$, f=5MHz	60 —	86 60	— —	dB
Supply Voltage Rejection Ratio Gain2 (note 4)	$\Delta V^{+}/V=\pm 0.5V$	50	70	—	dB
Output Offset Voltage Gain1 (note 1) Output Offset Voltage Gain2 (note 2,4) Output Offset Voltage Gain3 (note 3)	$R_L=\infty$ $R_L=\infty$ $R_L=\infty$	— — —	— — 0.35	1.5 1.5 0.75	V
Output Common Mode Voltage	$R_L=\infty$	2.4	2.9	3.4	V
Output Voltage Swing	$R_L=2K\Omega$	3.0	4.0	—	V
Output Resistance		—	20	—	Ω
Operating Current	$R_L=\infty$	—	18	24	mA

(note 1): Gain select pins G_{1A} and G_{1B} connected together. (Gain1)
(note 2): Gain select pins G_{2A} and G_{2B} connected together. (Gain2)
(note 3): All gain select pins open.
(note 4): Apply to only 14 pin package.

■ TYPICAL CHARACTERISTICS

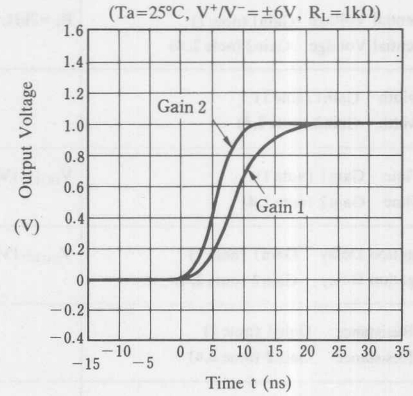
Output Voltage Swing

(Ta=25°C, V⁺/V⁻=±6V, R_L=1kΩ)



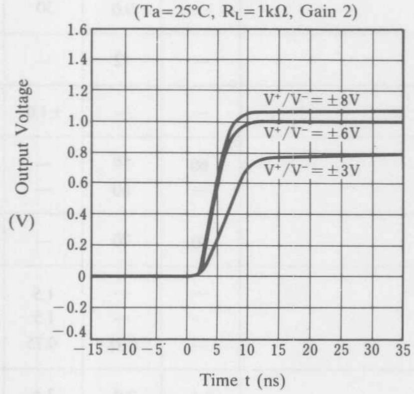
Pulse Responce

(Ta=25°C, V⁺/V⁻=±6V, R_L=1kΩ)



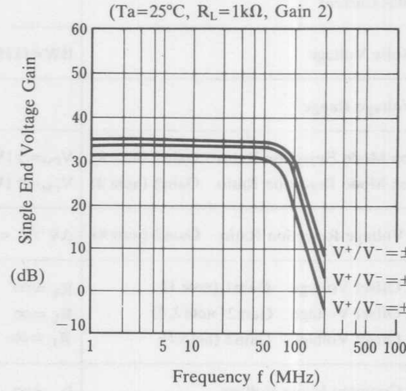
Pulse Responce

(Ta=25°C, R_L=1kΩ, Gain 2)



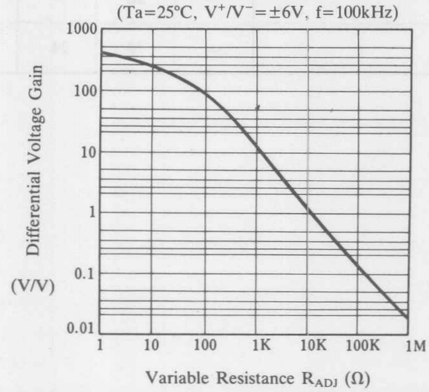
Single End Voltage Gain

(Ta=25°C, R_L=1kΩ, Gain 2)

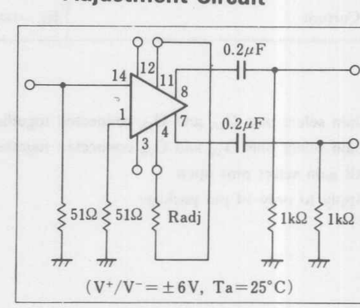


Differential Voltage Gain

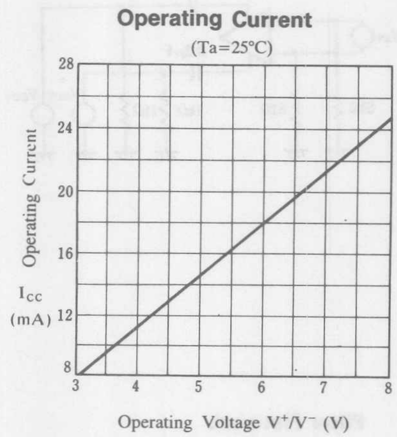
(Ta=25°C, V⁺/V⁻=±6V, f=100kHz)

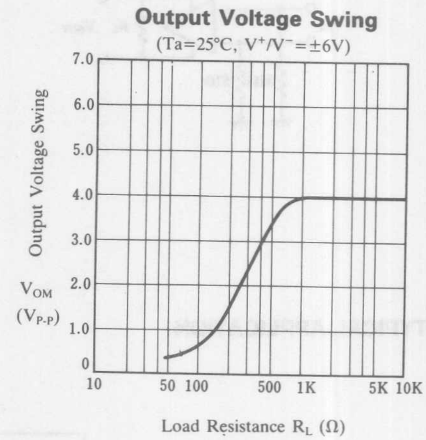


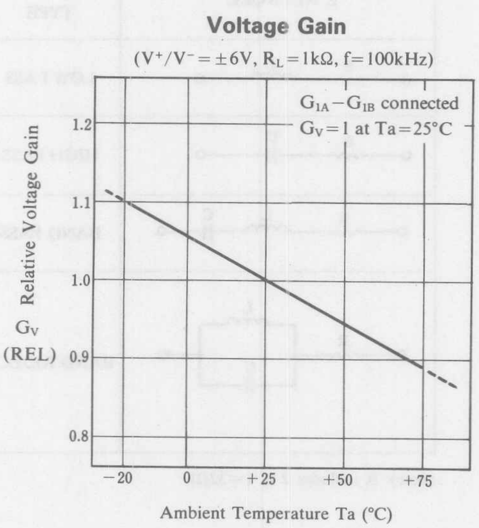
Differential Voltage Gain Adjustment Circuit



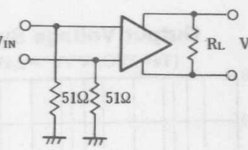
■ TYPICAL CHARACTERISTICS

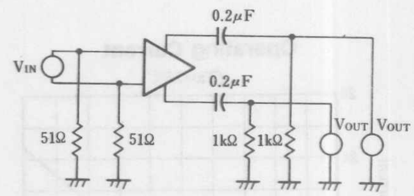






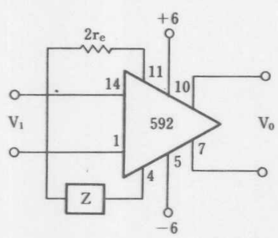
■ TEST CIRCUIT





■ TYPICAL APPLICATION

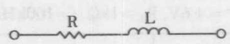
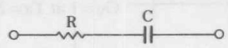
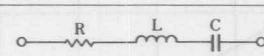
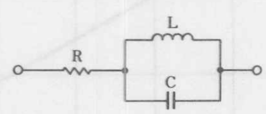
Basic circuit



$$\frac{V_0\,(s)}{V_1\,(s)} \cong \frac{1.4\times10^4}{Z(s)+2r_e}$$

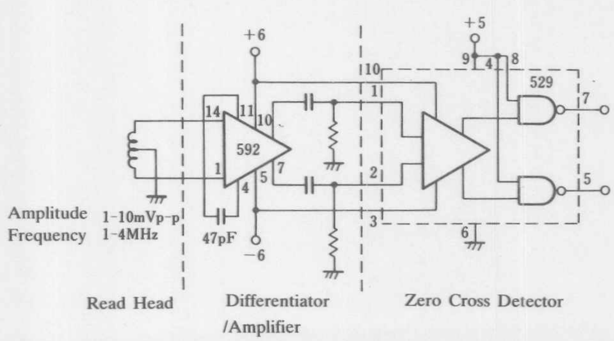
$$\cong \frac{1.4\times10^4}{Z(s)+32}$$

Filter Network

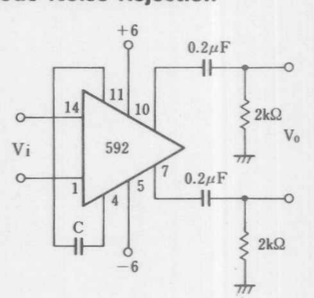
Z NETWORK	FILTER TYPE	$\frac{V_0(s)}{V_1(s)}$ TRANSFER FUNCTION
	LOW PASS	$\frac{1.0\times10^4}{L}\left[\frac{1}{s+R/L}\right]$
	HIGH PASS	$\frac{1.4\times10^4}{R}\left[\frac{s}{s+1/RC}\right]$
	BAND PASS	$\frac{1.4\times10^4}{L}\left[\frac{s}{s^2+R/L\,s+1/LC}\right]$
	BAND REJECT	$\frac{1.4\times10^4}{R}\left[\frac{s^2+1/LC}{s^2+1/LC+s/RC}\right]$

(note): R includes 2 r_e ($\approx 32\Omega$)

Disk/Tape Phase Modulated Readback Systems



Differentiation with High Common Mode Noise Rejection



$F_1 \ll 1/2\pi(32)C$

$V_o = 1.4\times10^4 C \frac{dV_i}{dT}$

TV VIDEO MODULATOR

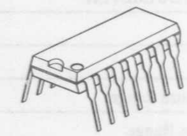
■ GENERAL DESCRIPTION

The NJM1372A is an integrated circuit to be used to generate an RF TV signal from baseband color-difference and luminance signals.

The NJM1372A contains a chroma subcarrier oscillator, lead and lag network, a quasi-quadrature suppressed carrier DSB chroma modulator, an RF oscillator and modulator, and a TTL compaible clock driver with adjustable duty cycle.

This device may also be used as a general-purpose modulator with a variety of video signal generating devices such as video games, test equipment, video type recorders, etc.

■ PACKAGE OUTLINE

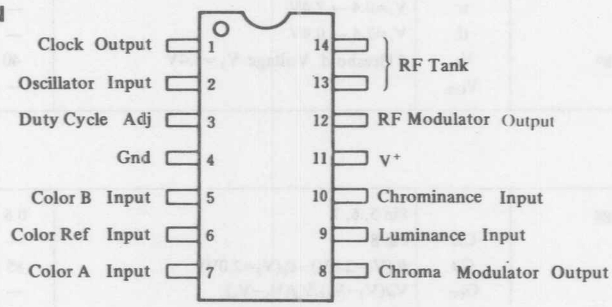


NJM1372AD

■ FEATURES

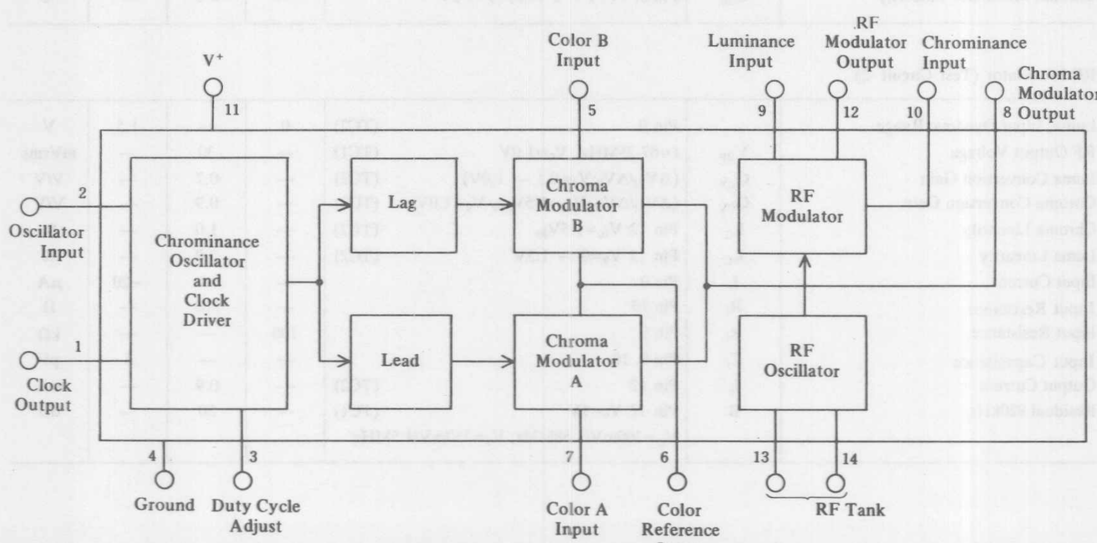
- Operating Voltage (+4.75V～+5.25V)
- Acts by Digital Control Signal
- Minimal External Components
- Composite Video Signal Generation Capability
- Low Power Dissipation
- Linear Chroma Modulators for High Versatility
- Ground-Referenced Video Prevents Over-modulation
- Package Outline DIP-14
- Bipolar Technology

■ PIN CONFIGURATION



NJM1372AD

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

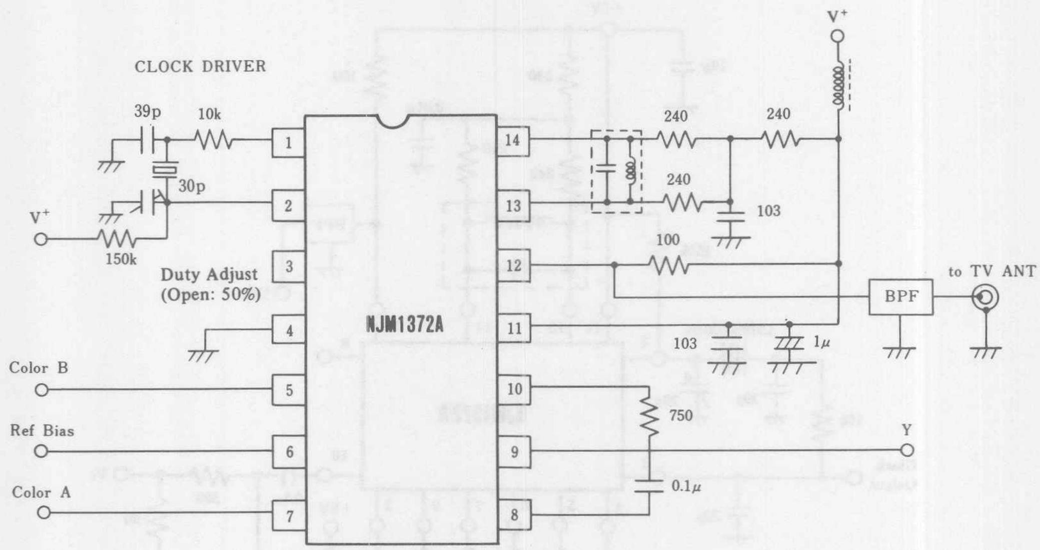
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

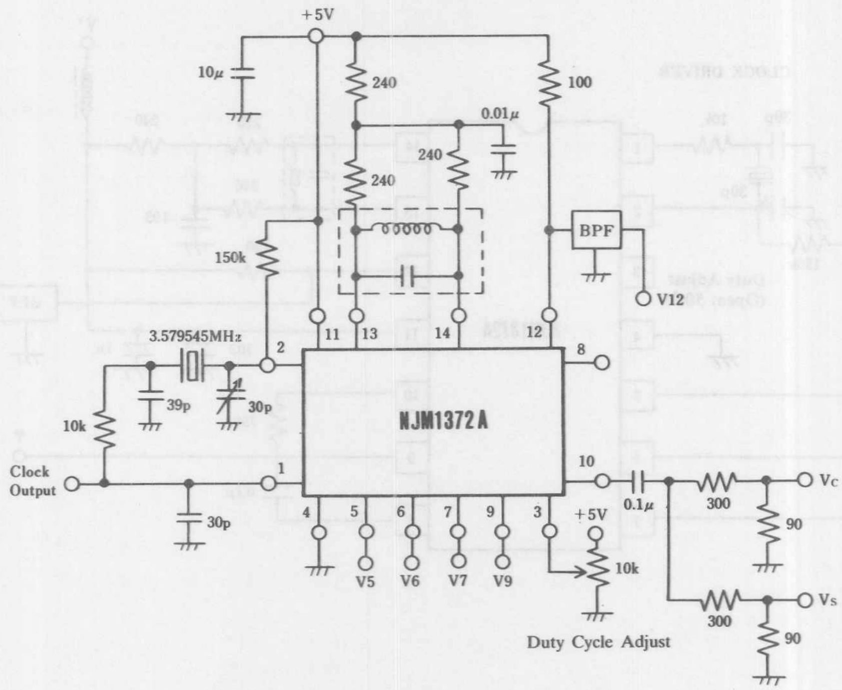
(Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		4.75	5.0	5.25	V
Operating Current	I_{CC}		—	25	—	mA
Chroma Oscillator/Clock Driver (TC1)						
Output Voltage	V_{OL}		—	—	0.4	V
Output Voltage	V_{OH}		2.4	—		V
Rise Time	tr	$V_1=0.4 \rightarrow 2.4V$	—	—	50	ns
Fall Time	tf	$V_1=2.4 \rightarrow 0.4V$	—	—	50	ns
Duty Cycle Adjustment Range	V_{aj}	THreshold Voltage $V_1=1.4V$	40	—	60	%
Inherent Duty Cycle	V_{OD}		—	50	—	%
Chroma Modulator (TC1)						
Input Common Voltage Range		Pin 5, 6, 7	0.8	—	2.3	V
Oscillator Feedthrough	CL	Pin 8	—	15	31	mV
Modulation Angle	$C\theta$	$\theta_8(V_7=2.0V)-\theta_8(V_5=2.0V)$	85	100	115	degree
Conversion Gain	G_{CC}	$V_8/(V_7-V_6);V_8/(V_5-V_6)$	—	0.8	—	V_{P-P}/V
Input Current	I_i	Pin 5, 6, 7	—	—	−20	μA
Input Resistance	R_i	Pin 5, 6, 7	100	—	—	kΩ
Input Capacitance	C_i	Pin 5, 6, 7	—	—	5	pF
Chroma Modulator Linearity	L_{cm}	Pin 8; $V_5=1 \rightarrow 2$ V:$V_7=1 \rightarrow 2V$	—	4.0	—	%
RF Modulator (Test Circuit 2)						
Luma, Input Dynamic Range		Pin 9 (TC2)	0	—	1.5	V
RF Output Voltage	V_{RF}	f=67.25MHz, $V_9=1.0V$ (TC1)	—	30	—	mVrms
Luma Conversion Gain	G_{LV}	$(\Delta V_{12}/\Delta V_9$:$V_9=0.1 \rightarrow 1.0V)$ (TC2)	—	0.7	—	V/V
Chroma Conversion Gain	G_{CV}	$(\Delta V_{12}/\Delta V_{10}$:$V_{10}=1.5V_{PP}$, $V_9=1.0V)$ (TC2)	—	0.9	—	V/V
Chroma Linearity	L_C	Pin 12 $V_{10}=1.5V_{PP}$ (TC2)	—	1.0	—	%
Luma Linearity	L_L	Pin 12 $V_9=0 \rightarrow 1.5V$ (TC2)	—	2.0	—	%
Input Current	I_i	Pin 9	—	—	−20	μA
Input Resistance	R_i	Pin 10	—	800	—	Ω
Input Resistance	R_i	Pin 9	100	—	—	kΩ
Input Capacitance	C_i	Pin 9, 10	—	—	5	pF
Output Current	I_o	Pin 12 (TC2)	—	0.9	—	mA
Residual 920kHz	B	Pin 12 $V_9=1V$ (TC1) $V_C=300mV/3.58MHz$; $V_S=250mV/4.5MHz$	—	50	—	dB

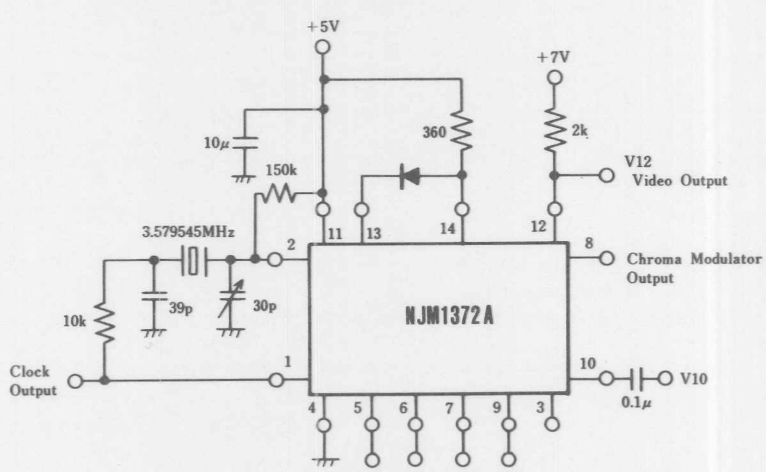
■ TYPICAL APPLICATION CIRCUIT



TEST CIRCUIT 1



TEST CIRCUIT 2



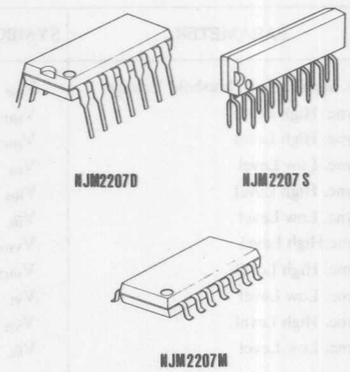
VIDEO SUPER IMPOSER

■ GENERAL DESCRIPTION

The NJM2207 is video signal superimposer, with synchronous separation circuit, vertical sinchronous reproduce circuit and two video high performance switches for switching from video signal to character signal and backgroud signal.

The NJM2207 is suitable for simply indicating the date time, TV channel and others.

■ PACKAGE OUTLINE



■ FEATURES

- Operating Voltage (+4.75V~+13V)
- With Synchronous Separation Circuit
- With Vertical Sinchronous Reproduce Circuit
- Package Outline DIP-14, DMP-14, ZIP-16
- Bipolar Technology

■ RECOMMENDED OPERATING CONDITION

- Operating Voltage 4.75~13V

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	17	V
Power Dissipation	P_D	(ZIP16) 500	mW
		(DIP14) 700	mW
		(DMP14) 300	mW
Operating Temperature Range	T_{opr}	−20~+75	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V⁺=5V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}		—	6.5	9	mA

Video Signal Processing Section (Video Input $2V_{PP}$, Source Resistance=75Ω)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
OFF-SET Voltage (Back-ground Input)	V_{BOS}	Cross Voltage In Ext. 10kΩ Resistor	—	—	0.1	V
OFF-SET Voltage (Char. Input)	V_{COS}	Cross Voltage In Ext. 10kΩ Resistor.	—	—	0.1	V
OFF-Voltage (Background Cont. Input)	V_{BL}		—	—	0.4	V
OFF-Voltage (Char. Cont Input)	V_{CL}		—	—	0.4	V
ON-Voltage (Background Cont. Input)	V_{BH}		2.0	—	—	V
ON-Voltage (Char. Cont. Input)	V_{CH}		2.0	—	—	V
Transfer Gain	G_V	R_L=5kΩ	−1	—	+1	dB
Frequency Response	Gf	f=10MHz, R_L=5kΩ	—	−0.2	—	dB
Crosstalk In Each Signal	C_T	Video Input (f=3.58MHz) Background Input (f=3.48MHz) Char. Input (f=3.68MHz) Each Signal. is Sine-Wave R_L=5kΩ	—	50	—	
Video Differential Phase	DP	R_L=5kΩ	—	—	3	Deg
Video Differential Gain	DG	R_L=5kΩ	—	—	3	%

■ ELECTRICAL CHARACTERISTICS SYNC. SEPARATION SECTION

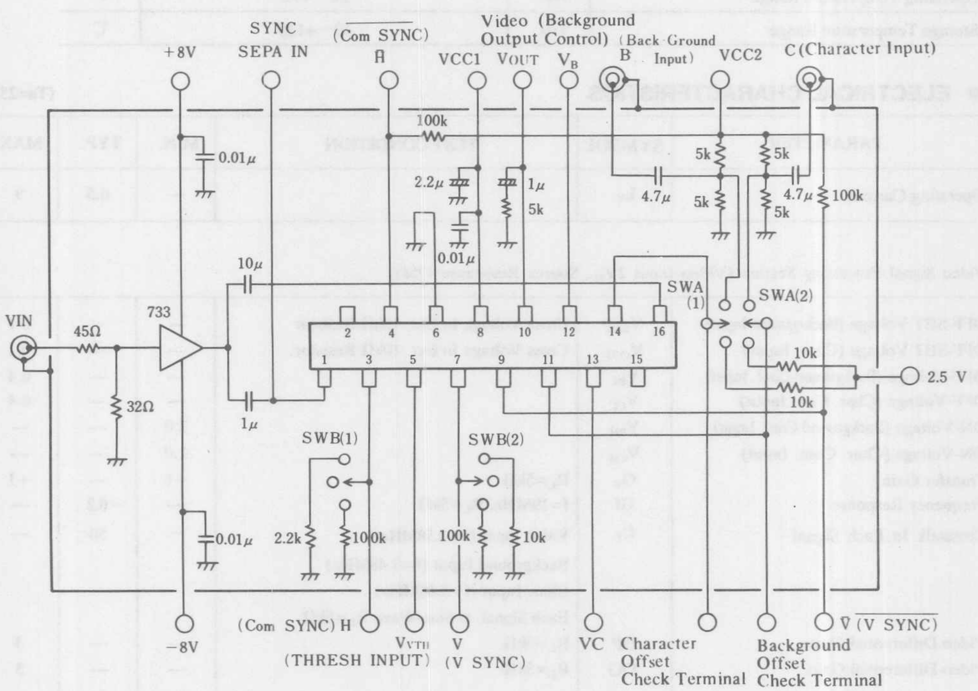
(Ta=25℃, V⁺=5V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
*Sync. Sepa. Input Threshold Voltage	V_{ISP}	Source Resistance Rg=75Ω	100	140	180	mV
H-Sync. High Level	V_{HH1}	R_L=100kΩ Pin 3 (13)	4.0	—	—	V
H-Sync. High Level	V_{HH2}	R_L=2.2kΩ Pin 3 (13)	3.6	4.1	—	V
H-Sync. Low Level	V_{HL}	R_L=2.2kΩ Pin 3 (13)	—	—	0.1	V
H-Sync. High Level	$V_{\bar{H}H}$	R_L=100kΩ Pin 4 (14)	4.9	—	—	V
H-Sync. Low Level	$V_{\bar{H}L}$	R_L=100kΩ Pin 4 (14)	—	—	0.3	V
V-Sync.High Level	V_{VH1}	R_L=100kΩ Pin 7 (2)	4.0	—	—	V
V-Sync. High Level	V_{VH2}	R_L=10kΩ Pin 7 (2)	3.6	4.1	—	V
V-Sync. Low Level	V_{VL}	R_L=10kΩ Pin 7 (2)	—	—	0.1	V
V-Sync. High Level	$V_{\bar{V}H}$	R_L=100kΩ Pin 9 (4)	4.9	—	—	V
V-Sync. Low Level	$V_{\bar{V}L}$	R_L=100kΩ Pin 9 (4)	—	—	0.3	V
Schmitt Trigger						
Threshold High Level	V_{VTH}	Pin 5 Input Voltage (1)	1.9	2.1	2.3	V
Threshold Low Level	V_{VTL}	Pin 5 Input Voltage (1)	1.1	1.3	1.5	V

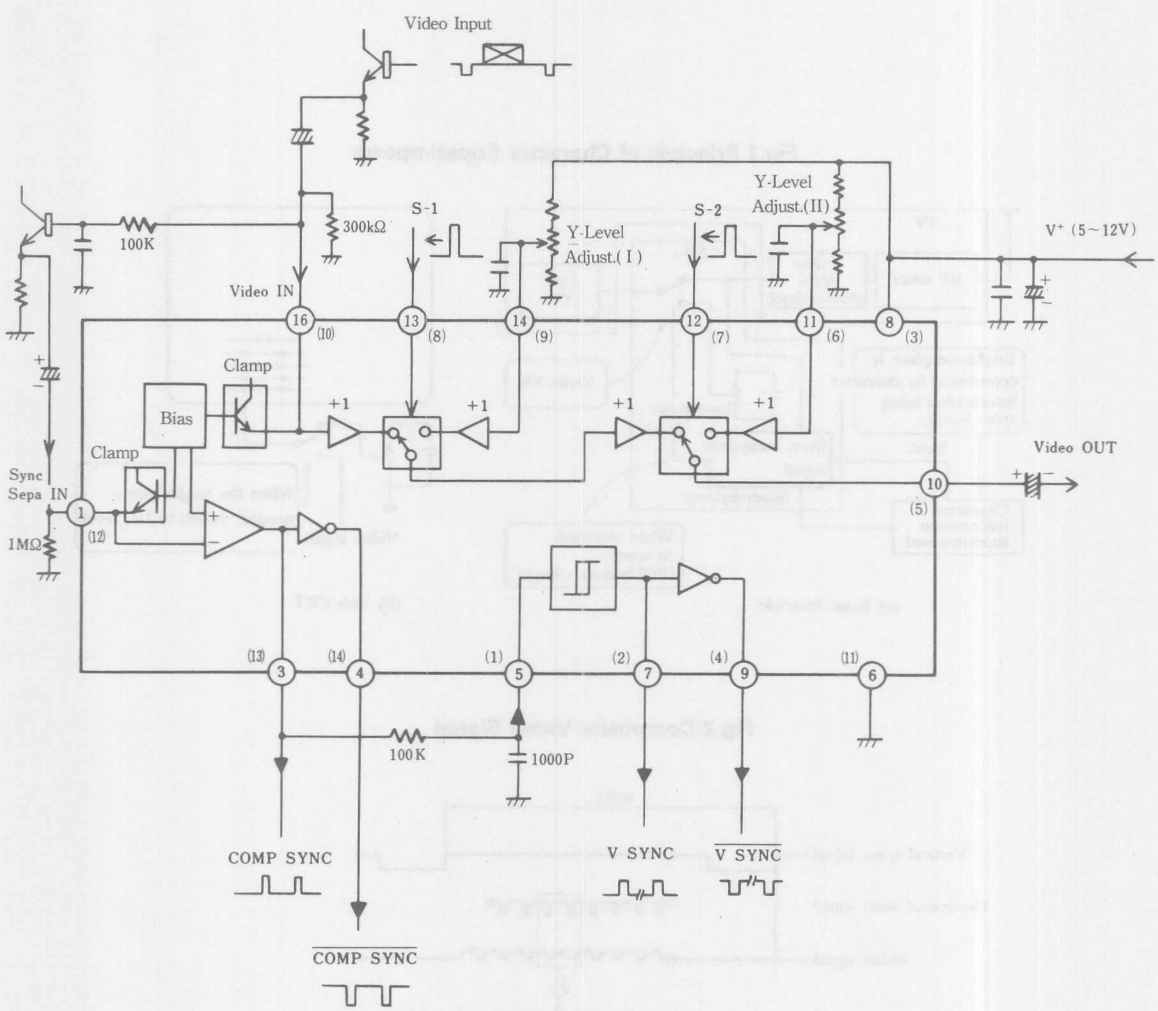
(Note) : ( ) to DIP-14/DMP-14

* A version (100mV Typ.)

■ TEST CIRCUIT



■ TYPICAL APPLICATION



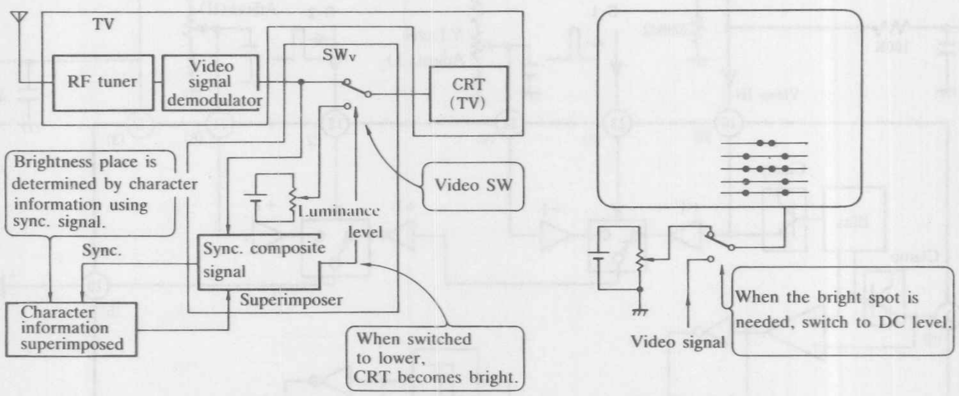
Note 1: Pin Connection to ZIP-16 (Pin 2, Pin 15: NC). ( ) to DIP-14/DMP-14
Note 2: Syn. Sepa. Input Threshold voltage increases 40mV (typ.) when putting 1MΩ in to Pin 1 (Pin 12).

■ PRINCIPLE OF CHARACTER SUPERIMPOSER

Basic principle is shown at Fig. 1.

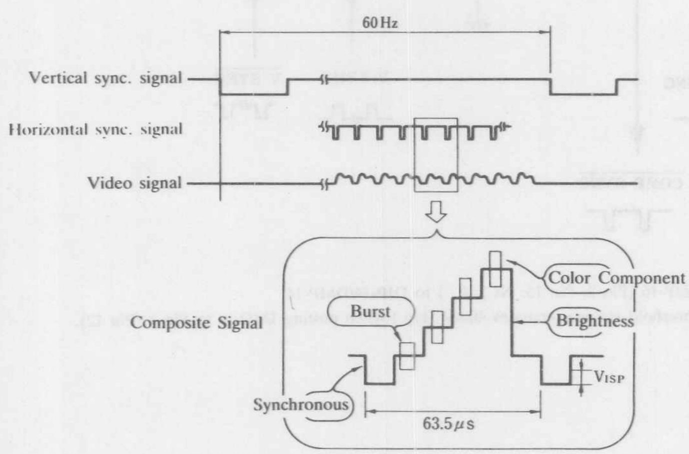
Usual TV has video (composite) signal output and input terminals to connect VCR or others. There is all information about picture on video composite signal (Ref. to Fig. 2). Its time signal of horizontal and vertical synchronous signal indicates the brighten place of TV tube. For brightening TV tube regardless video signal, the video input signal has to be switched to DC level (luminance level) on that scanning time. On this method, character is shown with background of usual picture.

Fig.1 Principle of Character Superimposer



(a) Basic Principle (b) with CRT

Fig.2 Composite Video Signal



■ CIRCUIT CONFIGURATION

Date superimposer circuit configuration on TV is shown at Fig. 3. The NJM2207 includes video switches which convert, usual video signal (horizontal and vertical synchronous signal, video) to signal, of superimposed character given by character generator.

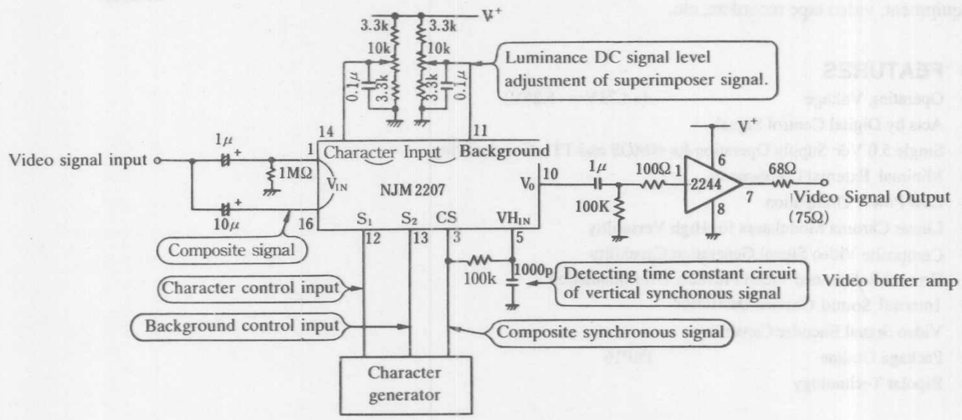


Fig.3 Typical circuit of date superimposer

TV VIDEO MODULATOR

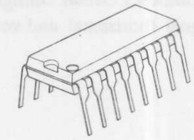
■ GENERAL DESCRIPTION

The NJM2208, an integrated circuit used to generate an RF TV signal from baseband color-difference and luminance signals.

The NJM2208 contains a chroma subcarrier oscillator, 3.58MHz oscillator, 4.5MHz oscillator, 3.58MHz lead and lag network, an RF oscillator, sound carrier oscillator, and a TTL compaible clock driver with adjustable duty cycle.

This device may also be used as a general-purpose modulator with a variety of video signal generating devices such as video games, test equipment, video tape recorders, etc.

■ PACKAGE OUTLINE

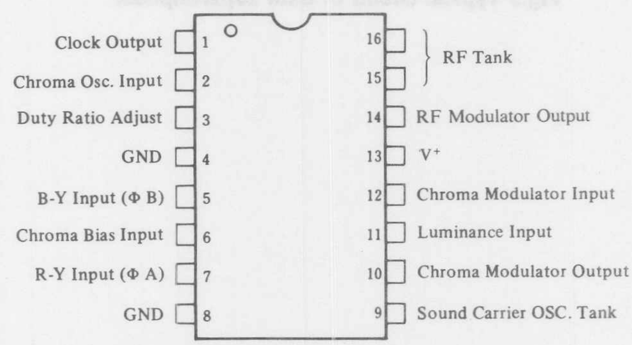


NJM2208D

■ FEATURES

- Operating Voltage (+4.75V~+5.25V)
- Acts by Digital Control Signal
- Single 5.0 Vdc Supply Operation for NMOS and TTL Compatibility
- Minimal External Components
- Low Power Dissipation
- Linear Chroma Modulators for High Versatility
- Composite Video Signal Generation Capability
- Ground-Referenced Video Prevents Overmodulation
- Internal Sound Carrier Oscillator
- Video Signal Encoder Capability
- Package Outline DIP16
- Bipolar Technology

■ PIN CONFIGURATION



NJM2208D

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

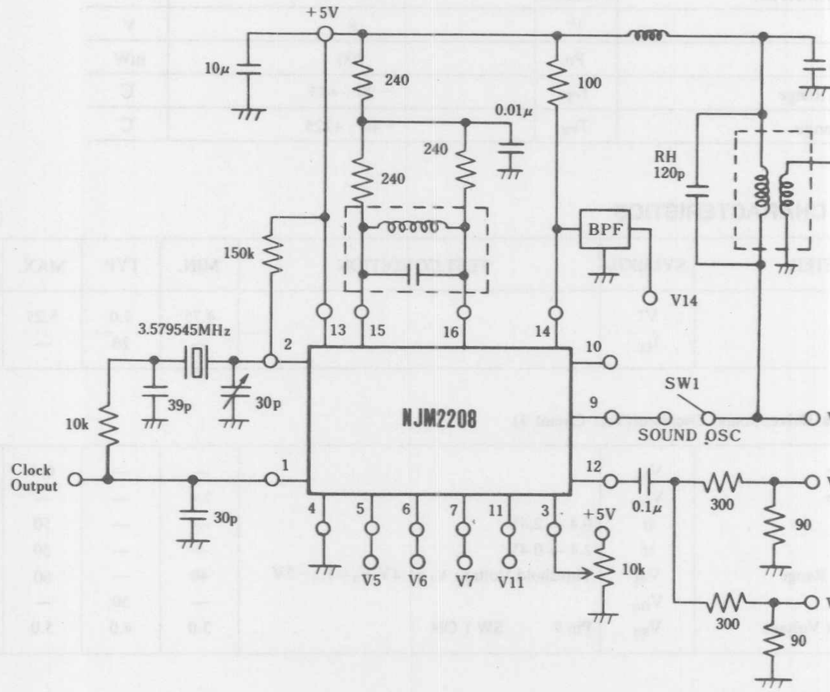
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

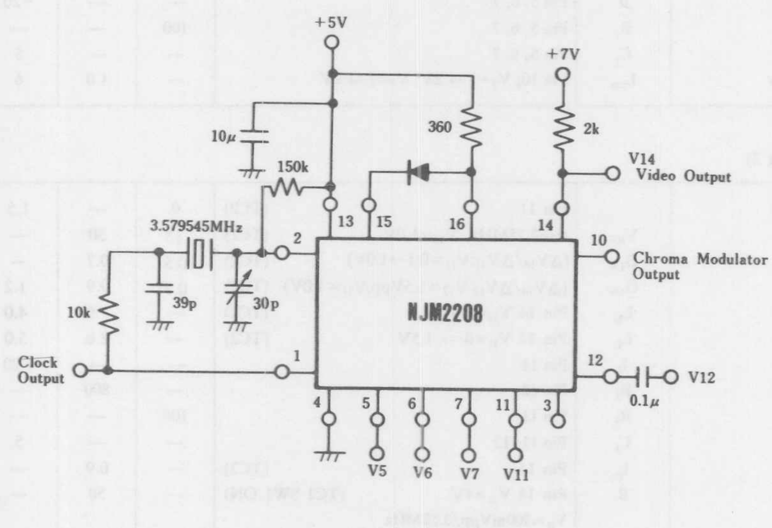
(Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		4.75	5.0	5.25	V
Operating Current	I_{CC}		—	26	—	mA
Chroma Oscillator/Clock Driver/Sound Oscillator(Test Circuit 1)						
Chroma Output Voltage	V_{OL}		—	—	0.4	V
Chroma Output Voltage	V_{OH}		2.4	—	—	V
Rise Time	tr	0.4 → 2.4V	—	—	50	ns
Fall Time	tf	2.4 → 0.4V	—	—	50	ns
Duty Cycle Adjustment Range	Vaj	Threshold Voltage V_1=1.4V,V_3=1.2～5V	40	—	60	%
Inherent Duty Cycle	V_{OD}		—	50	—	%
Sound Oscillator Output Voltage	V_{SO}	Pin 9 SW 1 ON	3.0	4.0	5.0	$V_{p\text{-}p}$
Chroma Modulator (Test Circuit 1)						
Input Common Mode Voltage Range		Pin 5, 6, 7	0.8	—	2.3	V
Oscillator Feedthrough	CL	Pin 10	—	15	31	mV
Modulation Angle	Cθ	θ_{10} (V_7=2.0V) − θ_{10} (V_5=2.0V)	85	100	115	degree
Conversion Gain	G_{CC}	$V_{10}/(V_7-V_6)$: $V_{10}/(V_5-V_6)$	—	0.6	—	$V_{p\text{-}p}$/V
Input Current	Ii	Pin 5, 6, 7	—	—	−20	μA
Input Resistance	R_i	Pin 5, 6, 7	100	—	—	kΩ
Input Capacitance	C_i	Pin 5, 6, 7	—	—	5	pF
Chroma Modulator Linearity	L_{cm}	Pin 10; V_5=1 → 2V; V_7=1 → 2V	—	4.0	6	%
RF Modulator (Test Circuit 2)						
Luma Input Dynamic Range		Pin 11 (TC2)	0	—	1.5	V
RF Output Voltage	V_{RF}	f=67.25MHz, V_{11}=1.0V (TC1)	15	30	—	mVrms
Luminance	G_{LV}	($\Delta V_{14}/\Delta V_{11}$:$V_{11}$=0.1→1.0V) (TC2)	0.5	0.7	—	V/V
Chroma Conversion Gain	G_{CV}	($\Delta V_{14}/\Delta V_{12}$:$V_{12}$=1.5Vpp,$V_{11}$=1.0V) (TC2)	0.7	0.9	1.2	V/V
Chroma Linearity	L_C	Pin 14 V_{12}=1.5V_{PP} (TC2)	—	1.0	4.0	%
Luminance	L_L	Pin 14 V_{11}=0 → 1.5V (TC2)	—	2.0	5.0	%
Input Current	I_i	Pin 11	—	—	−20	μA
Input Resistance	R_i	Pin 12	—	800	—	Ω
Input Resistance	R_i	Pin 11	100	—	—	kΩ
Input Capacitance	C_i	Pin 11, 12	—	—	5	pF
Output Current	I_o	Pin 14 (TC2)	—	0.9	—	mA
Residual 920kHz	B	Pin 14 V_{11}=1V (TC1 SW1 ON) V_C=300mVpp/3.58MHz V_S=250mVpp/4.5MHz	—	50	—	dB

TEST CIRCUIT 1



TEST CIRCUIT 2



■ DESCRIPTION OF OPERATION

NJM2208 produces color difference signals and luminance signal from microcomputer output signals RGB, clock, and hold signals through the matrix circuit, and also produces the TV RF signal or video base band signal. Sound Carrier Input is also added to this IC, and a color TV RF modulator is composed by adding the video and sound carrier tank LC and crystal oscillator.

● Properties of TV waves

Fig. 2 shows the frequency band of TV RF signal. The band width of this signal is 6MHz, in which video signals (luminance signal and synchronous signals) are distributed with a video carrier wave of 4MHz. As a result, coase images appear at about 0Hz, while fine images appear at about 4MHz. The color signals are distributed over a range of 3.58MHz±500kHz from the color carrier. These signals are not included in monochromatic images, of course.

The color signals conduct the perpendicular 2-phase modulation with suppressed carrier in order to avoid the interference with the video signals. Unlike in AM and FM systems, this system modulates the color signals with the color difference signals obtained by deviating the carrier phase by 90°.

The TV sound carrier signal is distributed over a range of 4.5MHz ± 25kHz lated, the color signals are phase-modulated, and the sound carrier signal is FM-modulated in one channel, these signals overlap each other in a narrow band to be compatible with monochromatic TV, causing the TV waves to be complicated.

● RF modulator for color TV

Fig. 3 shows the basic operation circuit of NJM2208. Now, the operation will be described according to the production sequence of broadcast waves. A 3.58MHz color carrier is oscillated by a crystal oscillator at pins 1 and 2. This output (pin 1) can be led as a microcomputer clock. Higher harmonic components are removed from this square waveform through a BPF (bandpass filter).

Then, two signals are produced from a 3.58MHz sine wave. Of these signals, the LEAD signal is obtained by leading the phase by 45°, while the LAG signal is obtained by lagging the phase by 45° from the carrier phase by the CR constant in the IC, repectively. On the other hand, the color signals RGB are converted into two color difference signals E_{B-Y} and E_{R-Y} by the matrix circuit, and applied to pins 5 and 7. The LEAD wave is modulated and added by E_{B-Y}, while the LAG wave is modulated and added by E_{R-Y}. These chroma-modulated signals are output to pin 10. photo 1 shows the relationship between the color difference signals and the modulation output in case of color bars (TV quasi signal generation).

A sound carrier 4.5MHz is oscillated by L_1 connected to pin 9, and FM-modulated by the audio signal. Accordingly, a VHF (2ch) is oscillated in the LC tank circuit of pins 15 and 16 by inputting the color and sound modulation signals to pin 12 and also color luminance signals to pin 11, and the differential transistors in IC are switched by the VHF voltage to generate an RF signal by the AM modulation. Photo 2 shows individual waveforms.

The RF signal is obtained through 75Ω to match the TV antenna impedance. Photo 3 indicates the RF signal with the sound carrier signal super imposed.

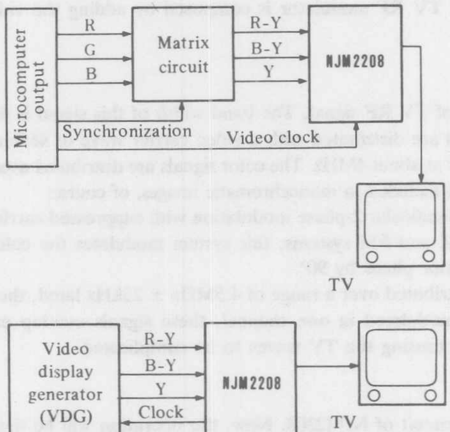
Since signals are present in the VHF band, the PCB patterns should be not long at pins 15 and 16, and a bypass capacitor should be connected to the power supply without fail. In addition, three oscillation signals should be isolated enough from each other with a sufficient mounting section interval.

● Application to base band output

This IC can also be taken as the video base band output as well as the RF output. In order to convert the RGB output signals from the microcomputer into the color difference signals and luminance signal, they are converted by the matrix circuit and connected to the color input terminals of NJM2208. This IC serves as a color encoder. TV images become clear, because neither RF modulation nor RF demodulation is done. For this purpose, remove the LC from pins 15 and 16, and connect the diode instead, so that the differential voltage in IC is fixed to drive IC as an amplifier.

An 1kΩ video signal is obtained. However, since this video signal output voltage is low and its output impedance is high, the video signal is amplified through an operational amplifier.

(Fig. 1) Application of video RF modulator (color encoder IC)



(Fig. 2) Freqency Spectrum In TV Wave

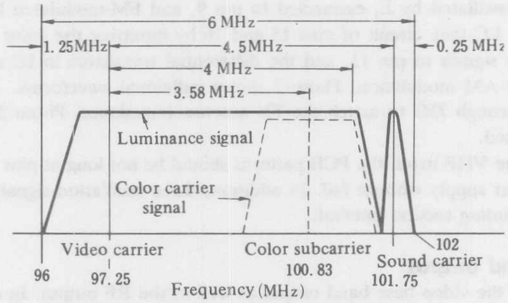


Fig - 3 MODULATOR FOR COLOR TV.

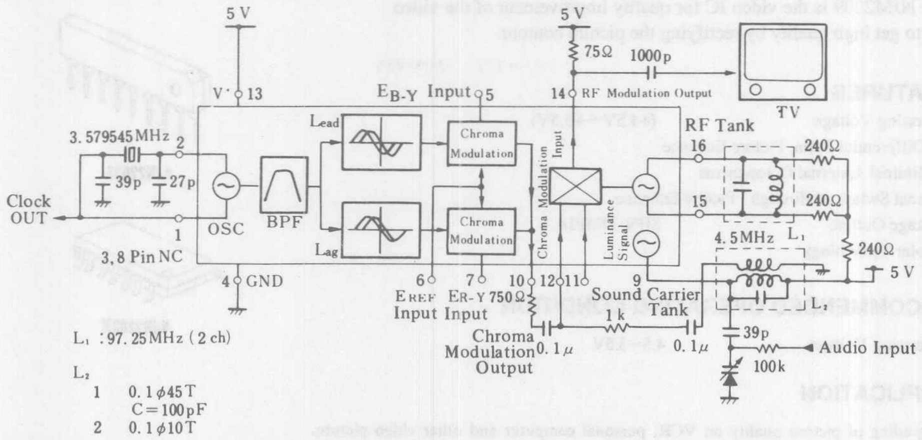


Fig - 4 APPLICATION OF BASE-BAND OUTPUT

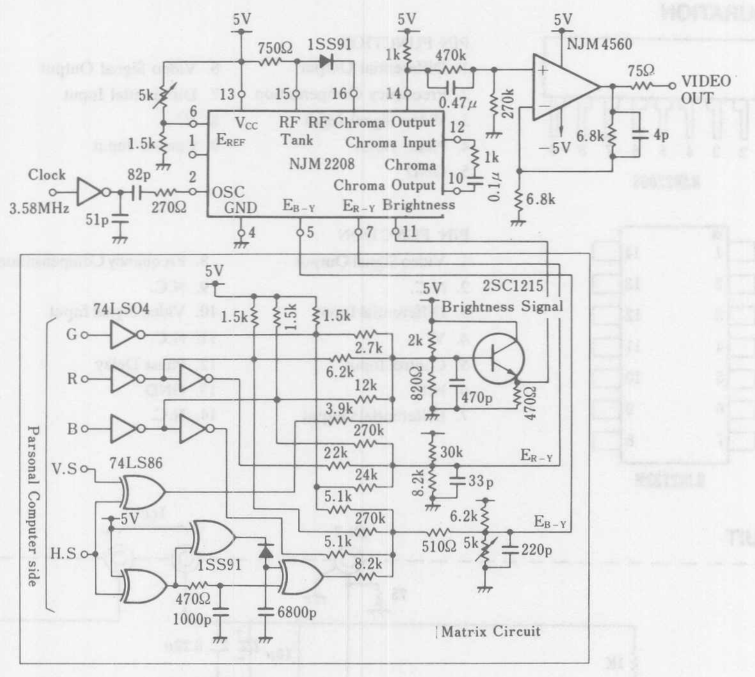
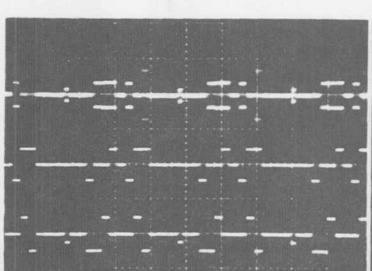
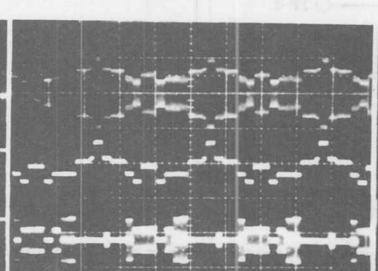


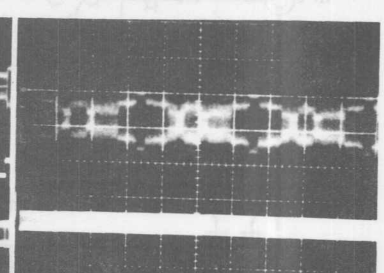
Photo-1 Color Difference Signals and Modulation Output by Color Bar

Photo-2 Video Luminance Signal and RF Output

Photo-3 RF Output with Sound Carrier Signal Superimposed





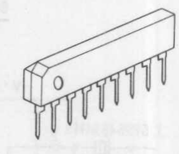


VIDEO PICTURE ENHANCER

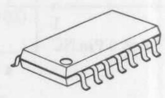
■ GENERAL DESCRIPTION

The NJM2209 is the video IC for quality improvement of the video picture to get high quality by rectifying the picture contour.

■ PACKAGE OUTLINE



NJM2209S



NJM2209M

■ FEATURES

- Operating Voltage (+4.5V~+5.5V)
- By Differential Form, Picture Enhance
- at Minimal External Components
- Internal Switch of Hirough / Picture Enhance
- Package Outline SIP9, DMP14
- Bipolar Technology

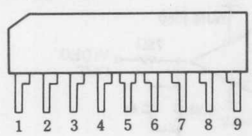
■ RECOMMENDED OPERATING CONDITION

- Operating Voltage 4.5~5.5V

■ APPLICATION

- Upgrading of picture quality on VCR, personal computer and other video picture.

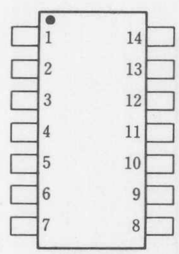
■ PIN CONFIGURATION



NJM2209S

PIN FUNCTION

1. Differential Output
2. Frequency Compensation
3. Video Signal Input
4. Phase Delay
5. GND
6. Video Signal Output
7. Differential Input
8. V+
9. Control Input

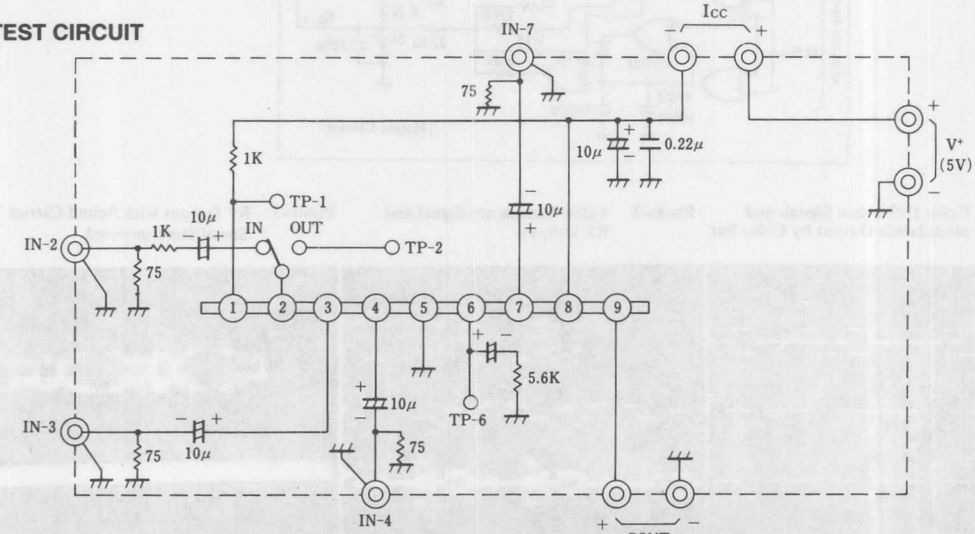


NJM2209M

PIN FUNCTION

1. Video Signal Output
2. N.C.
3. Differential Input
4. V+
5. Control Input
6. N.C.
7. Differential Output
8. Frequency Compensation
9. N.C.
10. Video Signal Input
11. N.C.
12. Phase Delay
13. GND
14. N.C.

■ TEST CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

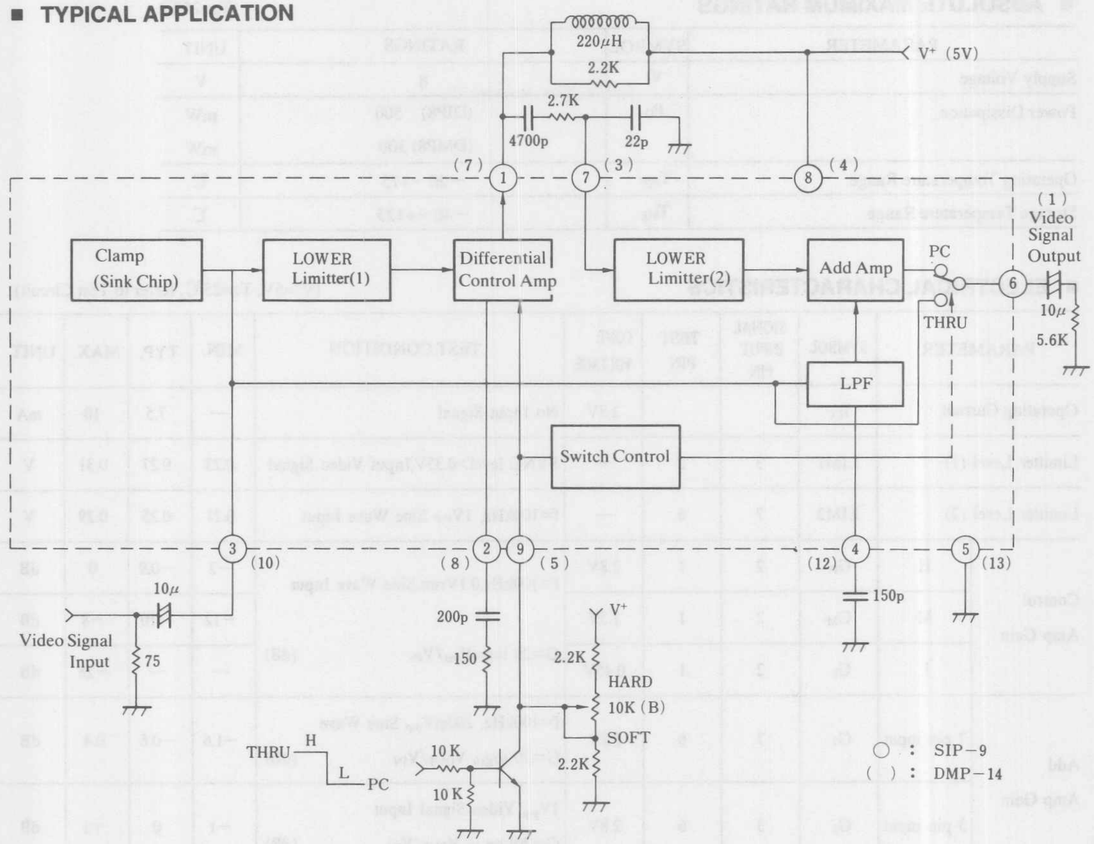
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃, Refer to Test Circuit))

PARAMETER		SYMBOL	SIGNAL INPUT PIN	TEST PIN	CONT. VOLTAGE	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current		I_{CC}			2.8V	No Input Signal	—	7.5	10	mA
Limitter Level (1)		LIM1	3	2	—	SYNC level>0.35V,Input Video Signal	0.23	0.27	0.31	V
Limitter Level (2)		LIM2	7	6	—	f=100kHz, $1V_{P-P}$ Sine Wave Input	0.21	0.25	0.29	V
Control Amp Gain	H	G_H	2	1	2.8V	f=100kHz,0.1Vrms.Sine Wave Input	−2	−0.9	0	dB
	M	G_M	2	1	1.3V		−12	−10	−8	dB
	L	G_L	2	1	0.45V	$G=20\log_{10}V_{out}/V_{IN}$ (dB)	—	—	−28	dB
Add Amp Gain	7 pin input	G_7	7	6	2.8V	f=100kHz, $200mV_{p-p}$ Sine Wave $G=20\log_{10}V_{OUT}/V_{IN}$ (dB)	−1.6	−0.6	0.4	dB
	3 pin input	G_3	3	6	2.8V	$1V_{p-p}$ Video Signal Input $G=20\log_{10}V_{OUT}/V_{IN}$ (dB)	−1	0	+1	dB
Switch Cross Talk		C_{SW}	4	6	2.8→0V	f=2MHz, $1V_{P-P}$ Sine Wave $C_{SW}=20\log_{10}V(0V)/V(2.8V)$ (dB)	—	−50	—	dB
Through Gain		G_T	3	6	0V	$1V_{P-P}$ Video Signal Input $G_T=20\log_{10}V_{OUT}/V_{IN}$ (dB)	−1	0	1	dB
Switch Control Threshold Voltage		V_{TH}	4	6		f=100kHz, $1V_{p-p}$ Sine Wave Input $-40dB=20\log_{10}V_{OUT}/V_{IN}$	0.2	0.3	0.4	V
Differential Gain(Note 1)		DG_{PC}	3	6	2.8V	DGDP Tester	—	1	3	%
Differential Gain(Note 2)		DG_T	3	6	0V	Video Signal $1V_{p-p}$(Stair Step)	—	0	3	%
6 PIN Voltage(Note 1)		V_{6PC}		6	2.8V		—	1.8	—	V
6 PIN Voltage(Note 2)		V_{6T}		6	0V		—	2.0	—	V

■ TYPICAL APPLICATION



■ PRINCIPLES OF OPERATION,BI BLOCK DIAGRAM

The NJM2209 is a video signal IC which converts an input video signal to a compensated video signal of the picture outline by adding an input signal through a differential amplifier to the original input signal.

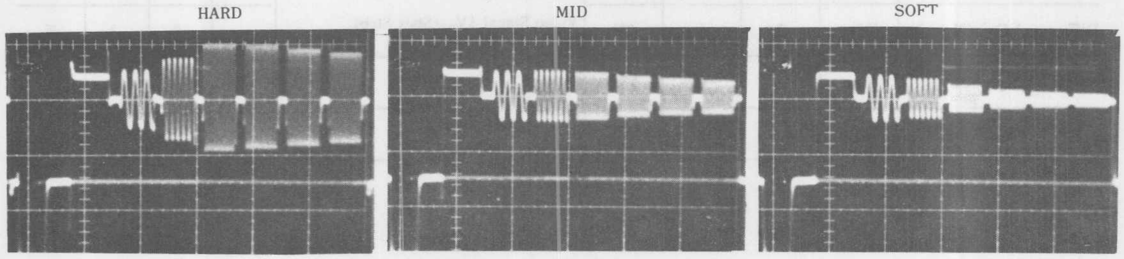
The compensating (enhanced) ratio is decided by pin 9 voltage and so the original signal comes when pin 9 voltage is zero.

A peaking frequency compensation of the internal differential amplifier is changed by C.R attached to pin 2 and L.R to pin 1.

The compensation signal and the original video signal are delayed the phase by low pass filter. These are done by a capacitor attached to pin 4. The compensated ratio is originally settled by the coupling condenser between pin 1 and pin 7.

Example (Multi-Burst Enhancer)

HARD MID SOFT



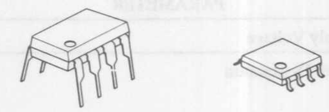
VIDEO NOISE REDUCER

■ GENERAL DESCRIPTION

The NJM2210 is a video noise reducer IC of which operation is to reduce noise contained in video color and luminance signal and at the same time to correct outline of horizontal and vertical image signal.

The NJM2210 is suit for VCR camera especially.

■ PACKAGE OUTLINE



NJM2210D NJM2210M

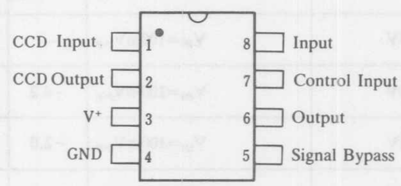
■ FEATURES

- Operating Voltage (+4.75V~+5.25V)
- It can compose Combtype Filter, with CCD IH delay line by that connect with
- It can be useful as Switching Noise Reduce Mode and Enhence
- Mode that are because of to Comb type Filter
- Package Outline DIP8, DMP8
- Bipolar Technology

■ RECOMMENDED OPERATING CONDITION

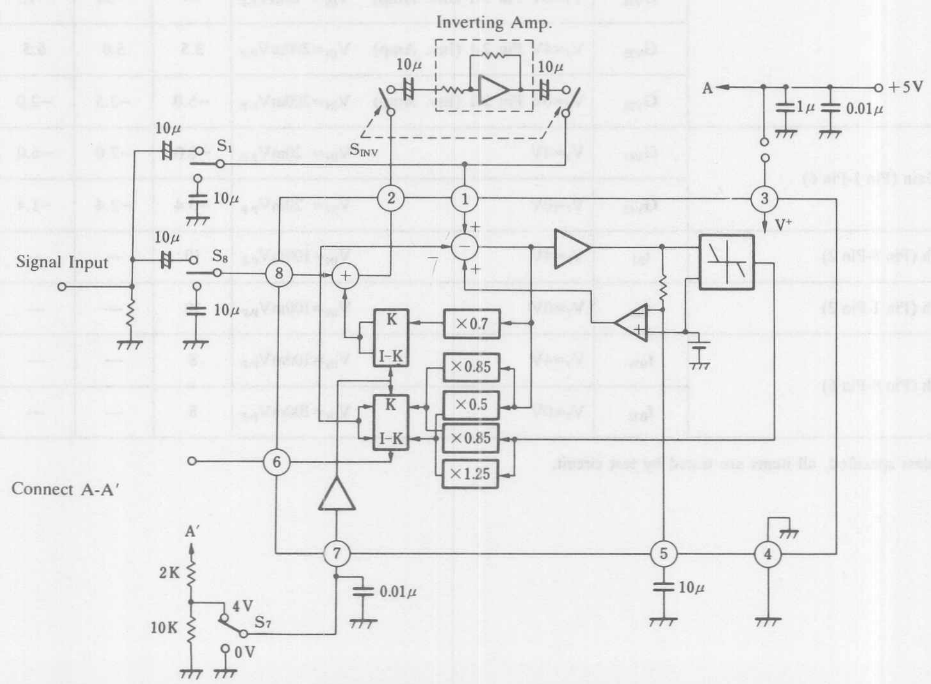
- Operating Voltage 4.75~5.25V

■ PIN CONFIGURATION



NJM2210D
NJM2210M

■ TEST CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Power Dissipation	P_D	(SIP8) 500	mW
		(DMP8) 300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

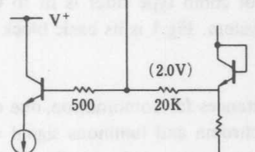
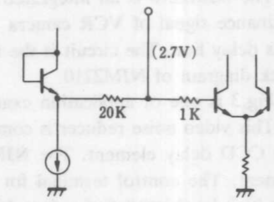
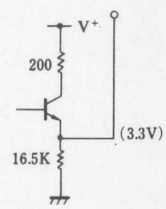
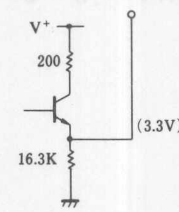
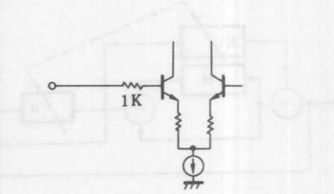
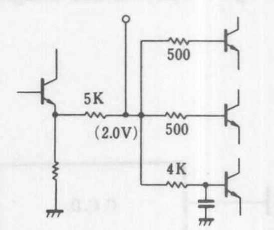
■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V⁺=5V, F=100kHz)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Curent	I_{CC}			—	6.9	10	mA
Voltage Gain (Pin 8-Pin 2)	G_{V11}	V_7=4V	V_{IN}=100m$V_{P\text{-}P}$	−1	0	+1	dB
	G_{V12}	V_7=0V	V_{IN}=100m$V_{P\text{-}P}$	−11.5	−10	−8.5	
Voltage Gain (Pin 1-Pin 2)	G_{V21}	V_7=4V	V_{IN}=100m$V_{P\text{-}P}$	—	−45	−38	dB
	G_{V22}	V_7=0V	V_{IN}=100m$V_{P\text{-}P}$	−4.2	−3.2	−2.2	
Voltage Gain (Pin 8-Pin 6)	G_{V31}	V_7=4V	V_{IN}=100m$V_{P\text{-}P}$	−2.0	−1.0	0	dB
	G_{V32}	V_7=0V	V_{IN}=100m$V_{P\text{-}P}$	−2.0	−1.0	0	
	G_{V33}	V_7=4V Pin 2-1 (Inv. Amp)	V_{IN}=10m$V_{P\text{-}P}$	—	−30	−18	
	G_{V34}	V_7=0V Pin 2-1 (Inv. Amp)	V_{IN}= 10m$V_{P\text{-}P}$	—	−30	−18	
	G_{V35}	V_7=4V Pin 2-1 (Inv. Amp)	V_{IN}=200m$V_{P\text{-}P}$	3.5	5.0	6.5	
	G_{V36}	V_7=0V Pin 2-1 (Inv. Amp)	V_{IN}=200m$V_{P\text{-}P}$	−5.0	−3.5	−2.0	
Voltage Gain (Pin 1-Pin 6)	G_{V41}	V_7=4V	V_{IN}= 20m$V_{P\text{-}P}$	−8.0	−7.0	−6.0	dB
	G_{V42}	V_7=0V	V_{IN}= 20m$V_{P\text{-}P}$	−3.4	−2.4	−1.4	
Bandwidth (Pin 8-Pin 2)	f_{B1}	V_7=4V	V_{IN}=100m$V_{P\text{-}P}$	10	—	—	MHz
Bandwidth (Pin 1-Pin 2)	f_{B2}	V_7=0V	V_{IN}=100m$V_{P\text{-}P}$	10	—	—	MHz
Bandwidth (Pin 8-Pin 6)	f_{B31}	V_7=4V	V_{IN}=100m$V_{P\text{-}P}$	8	—	—	MHz
	f_{B32}	V_7=0V	V_{IN}=100m$V_{P\text{-}P}$	8	—	—	

Note: Unless specified, all items are tested by test circuit.

■ TERMINAL FUNCTION

1 CCD Input		5 Signal Bypass	
2 CCD Output		6 Output	
3 V+		7 Control Input	
4 GND		8 Input	

■ APPLICATION NOTE

The NJM2210 is an integrated circuit of composing variable comb type filter which reduces noise mixed at chroma or luminance signal of VCR camera or others. Time delay element of comb type filter is fit to CCD delay element, not to glass delay line. The circuit is the most excellent FB with NULL system. Fig.1 is its basic block diagram and Fig.2 is actual block diagram of NJM2210.

Fig.3 is one of application examples.

This video noise reducer is composed of NJM2210, three capacitances for combination, one capacitance for signal bypass and CCD delay element. The NJM2210 is applicable to both of chroma and luminous signal with each fitted CCD delay element. The control terminal for switching reduce and enhance operates as enhance (increasing of high frequency part) with high level input and reduce (decreasing of high frequency part) with low level input. Its threshold level is about 2.25V at 5V supply voltage. Fig.4 is basic operating characteristics.

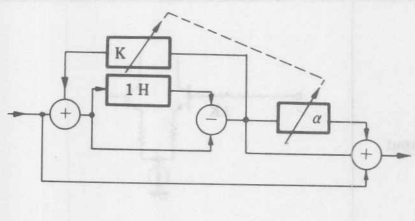


Fig.1 Basic Block Diagram

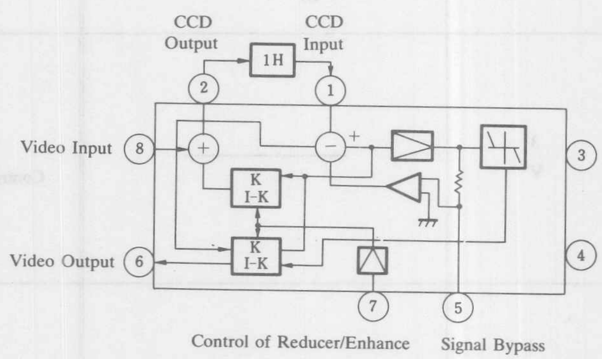


Fig.2 Block Diagram

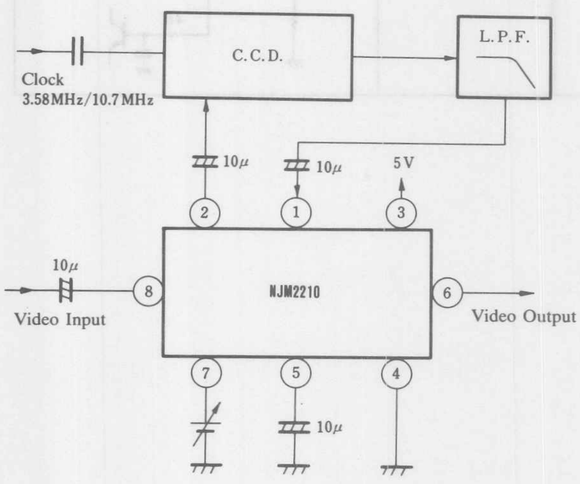


Fig.3 Application

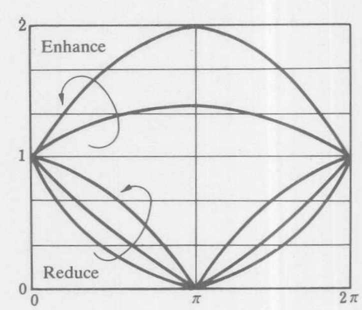


Fig.4 Basic Operating Characteristic

The comb type filter has special frequency characteristics like Fig.5 and is widely used to separate luminance and color signal in VCR circuit. The NJM2210 is automatical video signal noise reducer and signal enhancer.

Fig.6 shows video signal wave form and its frequency component.

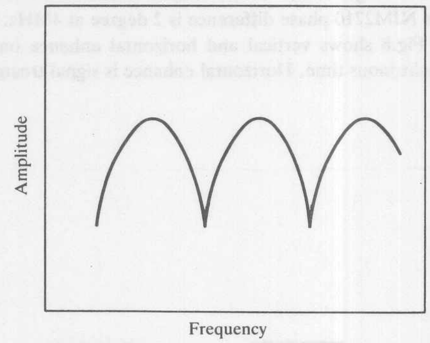


Fig.5 Comb Type Filter Frequency Characteristic

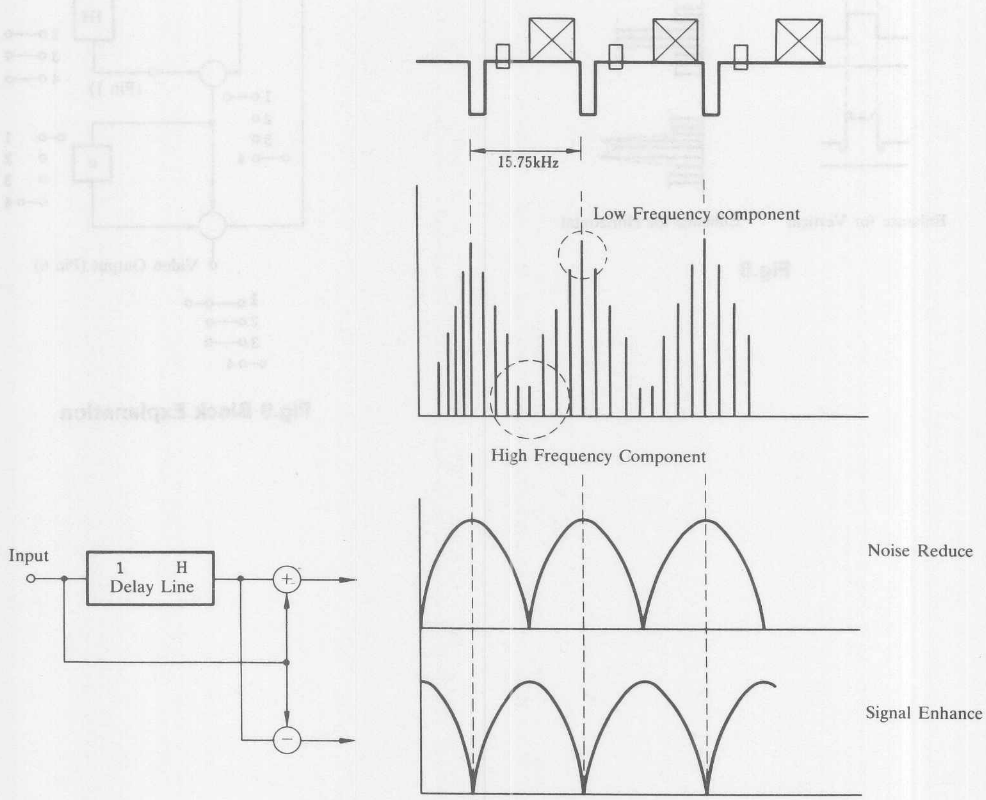


Fig.6 Video Signal Waveform & Frequency Component

The NJM2210 operates automatically as noise reducer with low supply voltage to Pin 7 and signal enhancer with high voltage to Pin 7.

Fig.7 shows output characteristics when applied high or low voltage to Pin 7. This system is adding and subtracting form of signals and so the output characteristic distortion comb type filter comes from phase difference of each system. The NJM2210 phase difference is 2 degree at 4MHz. High dynamic range of video signal is reallized by high supply voltage.

Fig.8 shows vertical and horizontal enhance on display. Vertical enhance is signal treatment within 1H of horizontal synchronous time. Horizontal enhance is signal treatment between each horizontal synchronous signal and Fig.9 shows this.

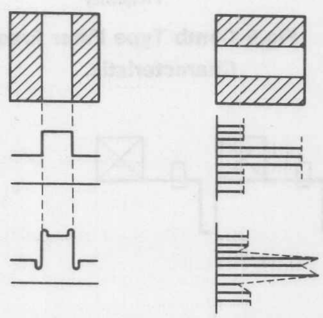


Fig.8

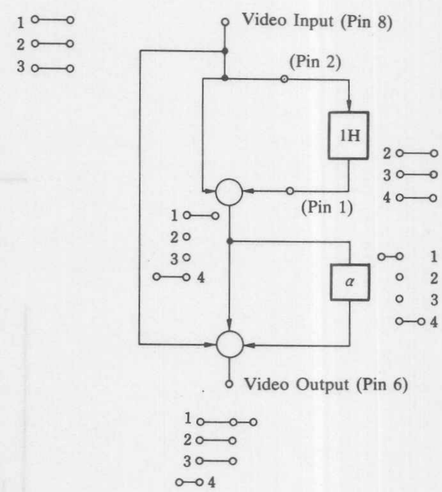
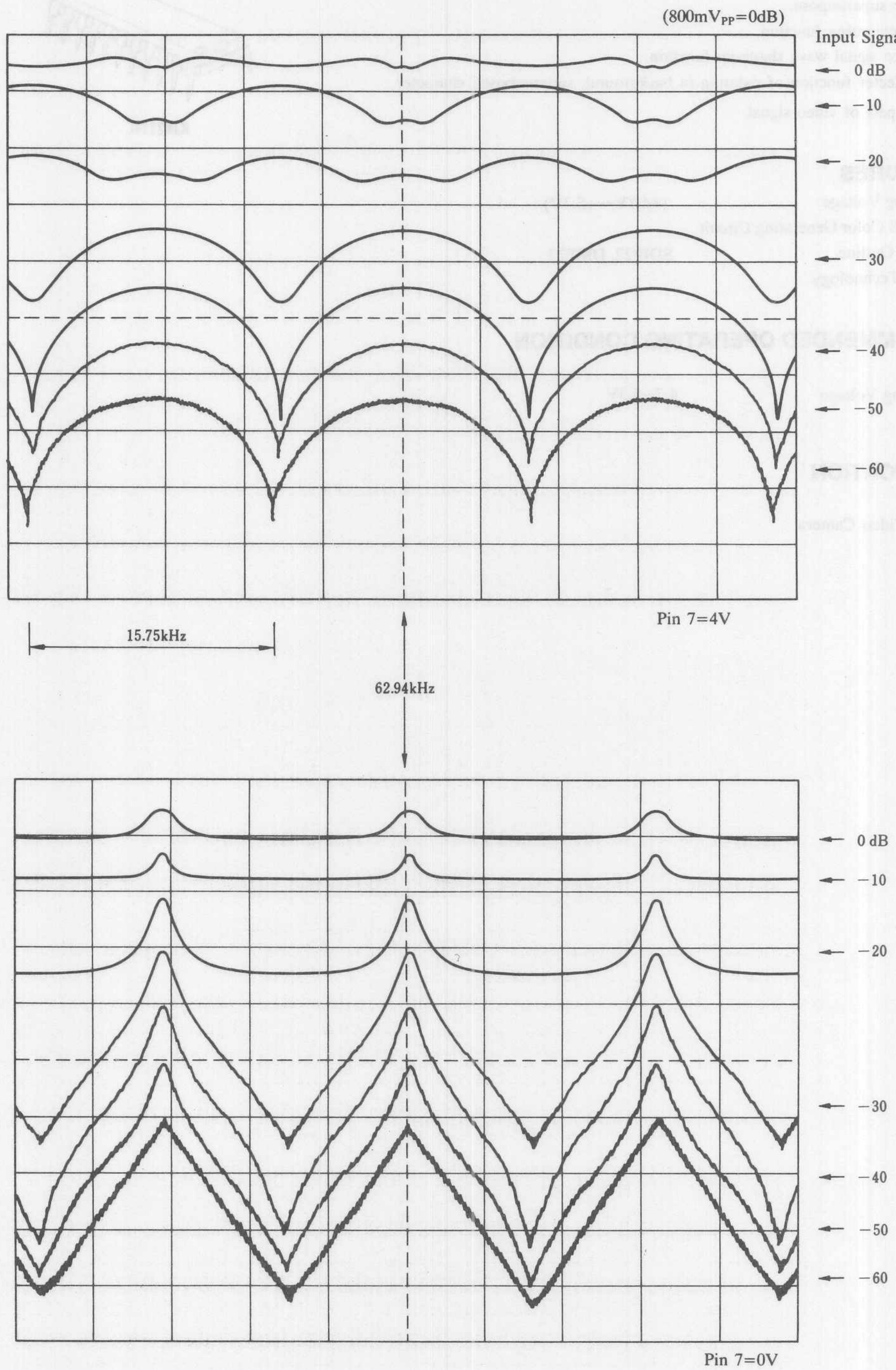


Fig.9 Block Explanation

Fig. 7 Comb Type Filter Characteristics vs. Input Signal Level (800mV$_{PP}$=0dB)



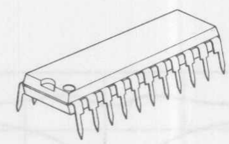
VIDEO ON-SCREEN DISPLAY

■ GENERAL DESCRIPTION

The NJM2214 is a video display convertive integrated circuit. Its function is below.

- Character superimpose.
- 8 color generating function.
- Luminance signal wave shape-up function.
- Video effecter function of painting to background, superimposed character or some part of video signal.

■ PACKAGE OUTLINE



NJM2214L

■ FEATURES

- Operating Voltage (+4.7V~+5.3V)
- Internal 8 Color Generating Circuit
- Package Outline SDIP22, DMP22
- Bipolar Technology

■ RECOMMENDED OPERATING CONDITION

- Operating Voltage 4.7~5.3V

■ APPLICATION

- VCR, Video Camera

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	10	V
Power Dissipation	P_D	(SDIP22) 700	mW
Operating Temperature Range	T_{opr}	−20~+75	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V⁺=5V)

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Curent		I_{CC}	No signal, No load	17	25	33	mA
Video Switch Voltage Gain		G_V	10, 11, 15, 22 Pin=Low 10STEP Stair wave, $2.2V_{P-P}$, R1=5K	−1	0	+1	dB
Frequency Characteristics		G_F	10, 11, 15, 22 Pin=Low $2V_{P-P}$, 4MHz, R1=5K	−1	0	+1	dB
Differential Gain		DG	10, 11, 15, 22 Pin=Low 10STEP Stair wave, $2.2V_{P-P}$, R1=5K	−3	0	+3	%
Differential Phase		DP	10 STEP Stair wave, $2.2V_{P-P}$R1=5K	−3	0	+3	degree
8 Color Output			15 Pin=High, 10, 11, 22 Pin=Low (Note)				
White	Amplitude	C_{1A}		—	0	100	mV_{P-P}
	Luminance	C_{1D}		1.56	1.66	1.76	V
	Phase	C_{1P}		—	—	—	degree
Yellow	Amplitude	C_{2A}		810	900	990	mV_{P-P}
	Luminance	C_{2D}		1.45	1.55	1.65	V
	Phase	C_{2P}	Phase: Ref. to Yellow	−10	0	10	degree
Cyan	Amplitude	C_{3A}		1160	1290	1420	mV_{P-P}
	Luminance	C_{3D}		1.26	1.36	1.46	V
	Phase	C_{3P}		106	116	126	degree

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V^+=5V)

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Green	Amplitude	C_{4A}		1080	1200	1320	mV_{p-p}
	Luminance	C_{4D}		1.14	1.24	1.34	V
	Phase	C_{4P}		63	73	83	degree
Magenta	Amplitude	C_{5A}		1080	1200	1320	mV_{p-p}
	Luminance	C_{5D}		0.96	1.06	1.16	V
	Phase	C_{5P}		243	253	263	degree
Red	Amplitude	C_{6A}		1160	1290	1420	mV_{p-p}
	Luminance	C_{6D}		0.85	0.95	1.05	V
	Phase	C_{6P}		286	296	306	degree
Blue	Amplitude	C_{7A}		810	900	990	mV_{p-p}
	Luminance	C_{7D}		0.66	0.76	0.86	V
	Phase	C_{7P}		170	180	190	degree
Black	Amplitude	C_{8A}		—	0	100	mV_{p-p}
	Luminance	C_{8D}		0.54	0.64	0.74	V
	Phase	C_{8P}		—	—	—	degree
Blanking Pulse Input Threshold Voltage		V_{TH-19}	Pin 19	1.0	1.5	2.0	V
HD		V_{TH-18}	Pin 18	1.0	1.5	2.0	V
Invert		V_{TH-11}	Pin 11	1.0	1.5	2.0	V
2 value Selection		V_{TH-10}	Pin 10	1.0	1.5	2.0	V
Background ON/OFF		V_{TH-15}	Pin 15	1.0	1.5	2.0	V
Matrix 1		V_{TH-M1}	Pin 1	3.3	3.9	4.5	V
Matrix 2		V_{TH-M2}	Pin 2	3.3	3.9	4.5	V
Matrix 3		V_{TH-M3}	Pin 3	3.3	3.9	4.5	V
Character Input		V_{TH-21}	Pin 21	0.5	1.0	1.5	V
EXT/Character Seclection		V_{TH-20}	Pin 22	1.0	1.5	2.0	V

(Note): f_{SC1},f_{SC2}=3.58MHz, 300mV_{PP}

f_{SC1}: same phase of color burst signal.

f_{SC2}: 90 degree phase lag from f_{SC1}.

■ RELATION BETWEEN 8 COLOR OUTPUT AND MATRIX INPUT

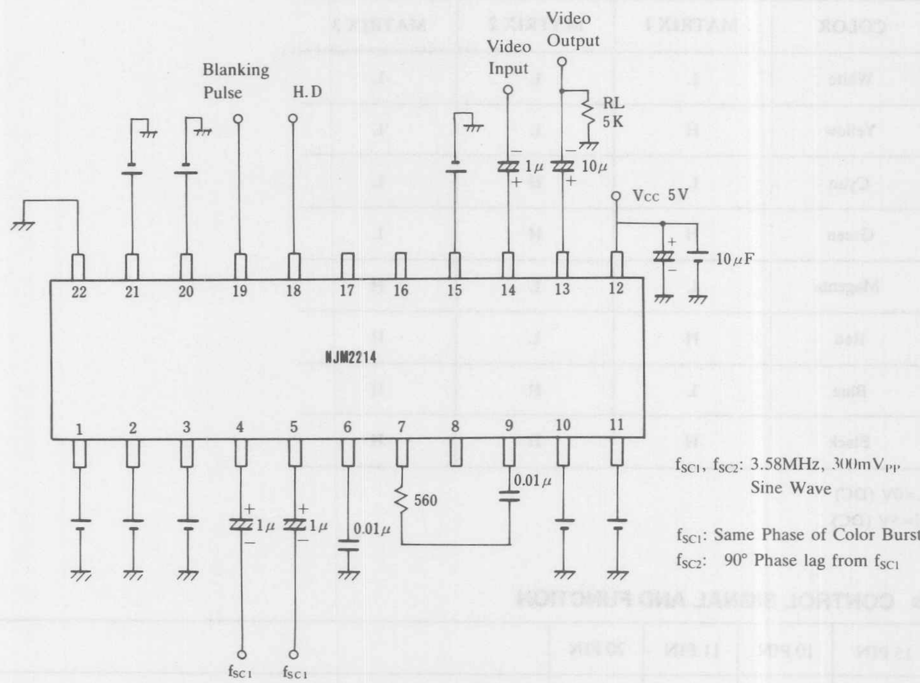
COLOR	MATRIX 1	MATRIX 2	MATRIX 3
White	L	L	L
Yellow	H	L	L
Cyan	L	H	L
Green	H	H	L
Magenta	L	L	H
Red	H	L	H
Blue	L	H	H
Black	H	H	H

L=0V (DC)
H=5V (DC)

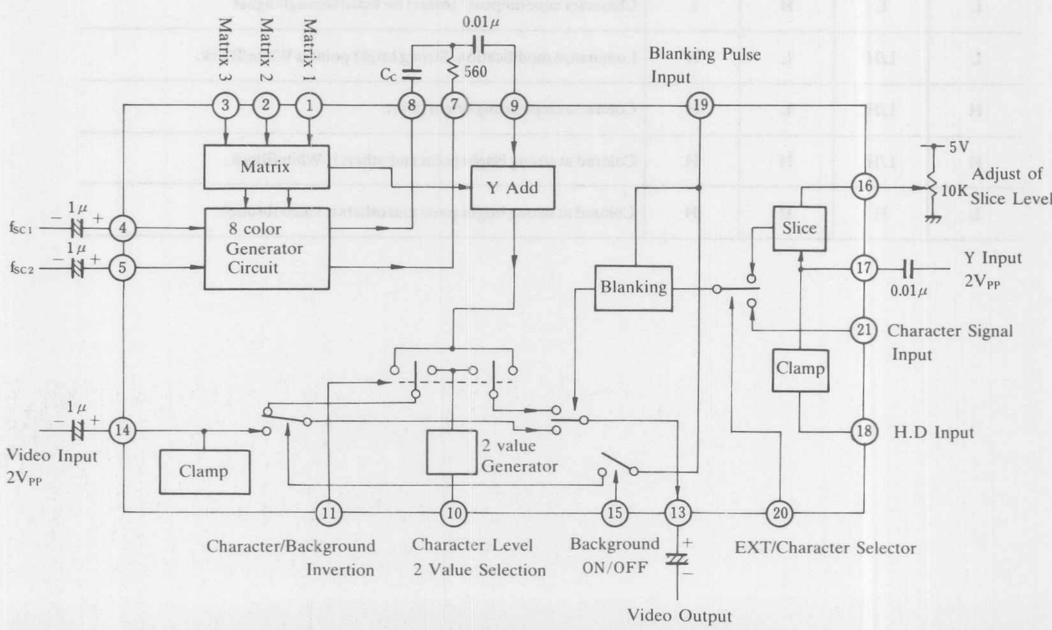
■ CONTROL SIGNAL AND FUNCTION

15 PIN	10 PIN	11 PIN	20 PIN	
L	L/H	L	L	Character superimposer (White/Black) on video through signal output.
H	L/H	L	L	Character superimposer (White/Black) on background (8 color)
H	L/H	H	L	Character superimposer (color) on background (White/Black)
L	L	H	L	Character superimposer (color) on video through signal
L	L/H	L	H	Luminance modification. Strong bright point is White/Black.
H	L/H	L	H	Colored except strong bright point.
H	L/H	H	H	Colored at strong bright point and others is White/Black.
L	H	H	H	Colored at strong bright point and others is video through.

■ TEST CIRCUIT



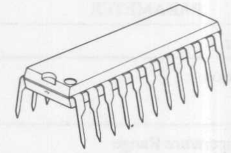
■ TYPICAL APPLICATION



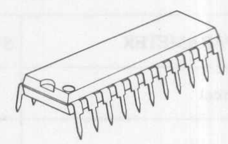
■ GENERAL DESCRIPTION

The NJM2217 has functions of character and background superimposition to video signal and consists of synchronous separation circuit, vertical synchronous reproducing circuit, video switch and AFC circuit. Built-in AFC circuit makes the NJM2217 stable to noise and disorder of synchronous signal and takes off character disorder on Display Broun tube.

■ PACKAGE OUTLINE



NJM2217D



NJM2217L

■ FEATURES

- Operating Voltage (+4V~+6V)
- 2 video signal input terminals
- Internal synchronous separation Circuit and internal horizontal synchronous reproduce circuit. Can make trigger signal to character generator.
- Stable horizontal synchronous signal by build-in AFC circuit.
- Package Outline DIP22, SDIP22
- Bipolar Technology

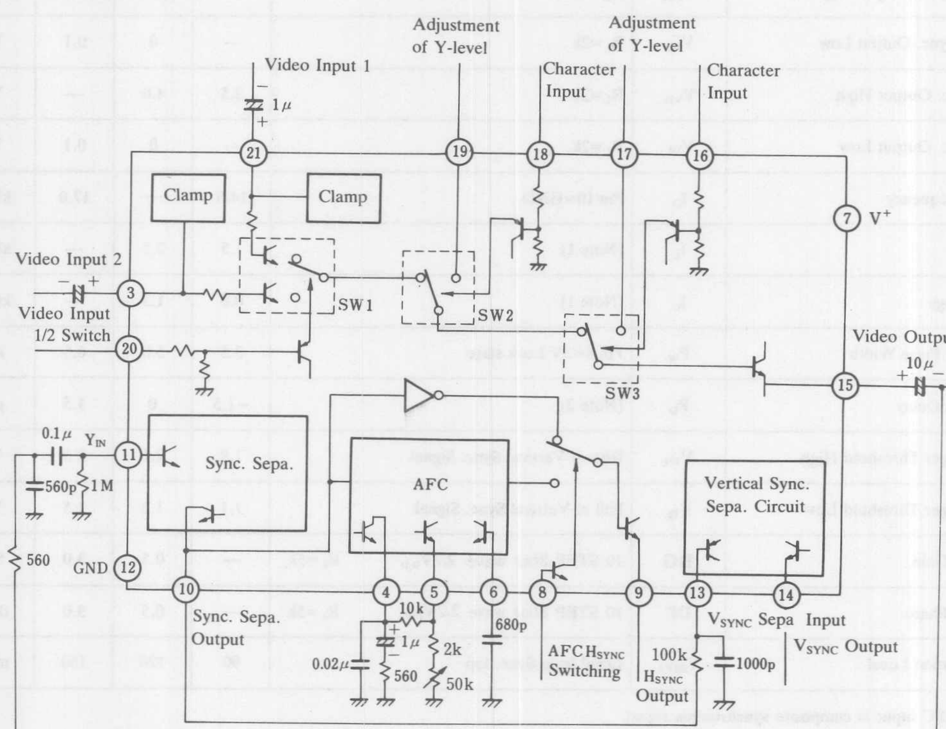
■ RECOMMENDED OPERATING CONDITION

- Operating Voltage 4V~6V

■ APPLICATION

- VCR, Video Camera, Other Video Equipment

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	7	V
Power Dissipation	P_D	(DIP22) 1000 (SDIP22) 700	mW mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

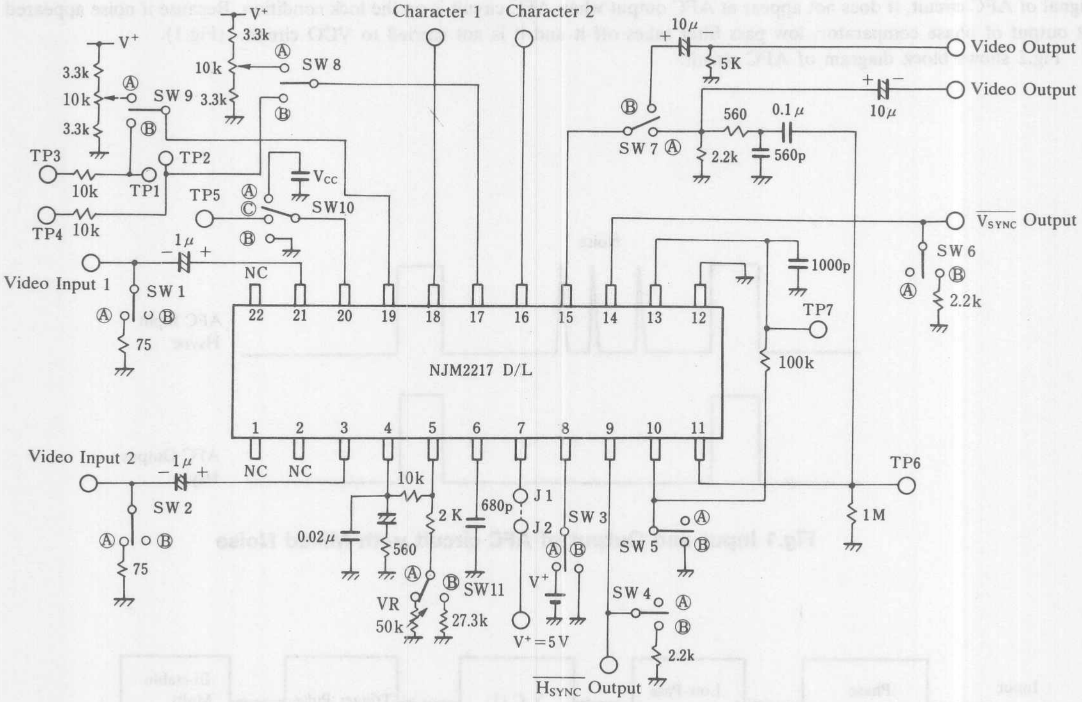
■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	No signal		—	20	26	mA
Offset Voltage of Luminance Control	V_{OS}	Ex. 10kΩ, Voltage difference between both terminals of resistor at 2.5V supply voltage 19 Pin, 17 Pin		—	—	0.1	V
Control Terminal Threshold	V_{TH}	16 Pin, 18 Pin, 20 Pin		0.4	1.4	2.0	V
Gain	G_V	10 STEP Stair wave $2.2V_{p\text{-}p}$	R_L=5k	−1	0	+1	dB
Frequency Characteristic	G_F	DC~5MHz $2V_{p\text{-}p}$	R_L=5k	−1	0	+1	dB
Cross-Talk	CT	3.58MHz $2V_{p\text{-}p}$ One side 75Ω terminal		—	50	—	dB
Horizontal Sync. Output High	V_{HH}	R_L=2k		3.5	4.0	—	V
Horizontal Sync. Output Low	V_{HL}	R_L=2k		—	0	0.1	V
Vertical Sync. Output High	V_{VH}	R_L=2k		3.5	4.0	—	V
Vertical Sync. Output Low	V_{VL}	R_L=2k		—	0	0.1	V
Free-Run Frequency	f_O	Pin 10=GND		14.5	—	17.0	kHz
Lock Range	f_L	(Note 1)		1.5	2.5	—	kHz
Capture Range	f_C	(Note 1)		0.6	1.3		kHz
AFC Output Pulse Width	P_W	Pin 8=5V Lock state		3.5	5.0	6.5	μs
AFC Output Delay	P_D	(Note 2)		−1.5	0	1.5	μs
Schmitt Trigger Threshold High	V_{TH}	Rise of Vertical Sync. Signal		1.9	2.1	2.3	V
Schmitt Trigger Threshold Low	V_{TL}	Fall of Vertical Sync. Signal		1.1	1.3	1.5	V
Differential Gain	DG	10 STEP Stair wave $2.2V_{p\text{-}p}$	R_L=5k	—	0.5	3.0	%
Differential Phase	DP	10 STEP Stair wave $2.2V_{p\text{-}p}$	R_L=5k	—	0.5	3.0	deg
Sync. Separation Level	V_{SEPA}	Level from Sync. top		90	120	150	mV

(Note 1): AFC input is composite synchronous signal.

(Note 2): Time lag between horizontal synchronous signal with AFC and without AFC. (The timing gap at 9 pin output, in the case of 8 pin =high, and 8 pin=low.)

■ **TEST CIRCUIT**



■ AFC CIRCUIT CONFIGURATION & ITS FEATURE

The NJM2217 has AFC function of horizontal synchronous signal applied to character generator. AFC circuit of the NJM2217 is like PLL circuit and operates as band pass filter. If pulse Noise is mixed to the input horizontal synchronous signal of AFC circuit, it does not appear at AFC output when AFC circuit is on the lock condition. Because if noise appeared at output of phase comparator, low pass filter takes off it and it is not carried to VCO circuit. (Fig.1).

Fig.2 shows block diagram of AFC circuit.

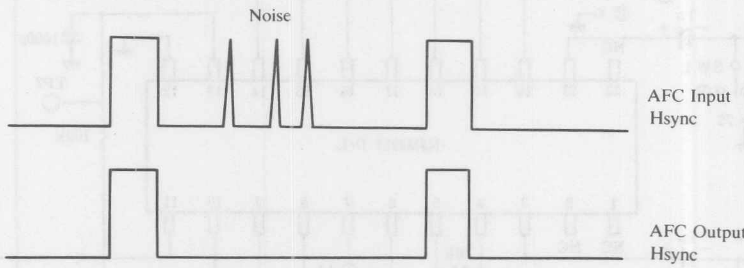


Fig.1 Input and Output of AFC circuit with Mixed Noise

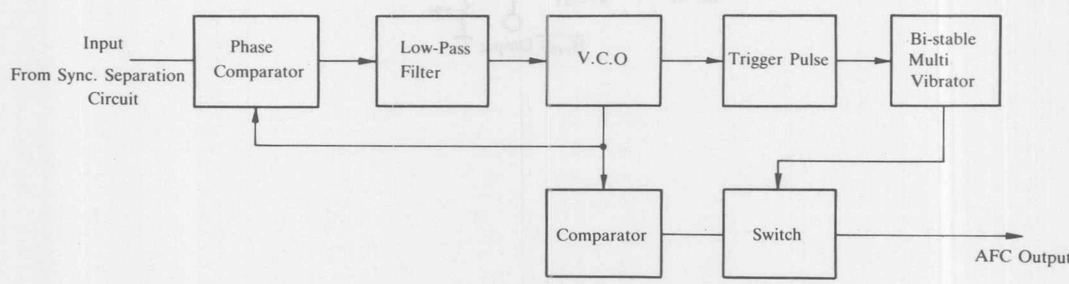
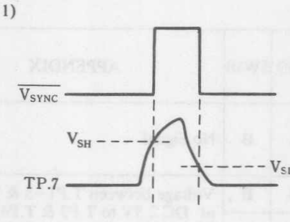


Fig.2 AFC Circuit Configuration

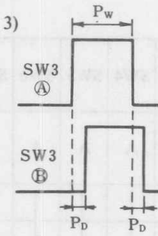
■ TEST CIRCUIT CONDITION

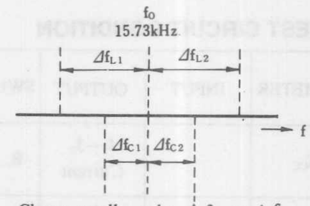
PARAMETER	INPUT	OUTPUT	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	APPENDIX
I_{CC}		J_1-J_2 Current	B	B	B	A	A	A	A	A	A	B	No Signal
V_{OS}	T.P3	T.P1	B	B						A	B	B,	Voltage between T.P1~3 & T.P2~4, at DC 2.5V to T.P3 & T.P4, DC 1.5V to character 1 & 2
	T.P4	T.P2	B	B						B	A	B	
V_{TH}	T.P5	Video								A	A	C	Voltage of video output 1, when video signal to video input 1, DC0→2V to T.P5, character 1, 2
	chra. 1, 2	Out 1											
G_V	Video In 1	Video							B			B	Input; 2.2$V_{P\text{-}P}$, 10 STEP stair wave
	Video In 2	Out 2										A	
G_F	Video In 1	Video										B	Input; 2$V_{P\text{-}P}$, Video sweep signal
	Video In 2	Out 2										A	(0~5MHz)
C_T	Video In 1	Video	B	A								A	Input; 2$V_{P\text{-}P}$, Sine wave, 3.58MHz
	Video In 2	Out 2	A	B								B	
DG	Video In 1	Video	B	B								B	Input; 2.2$V_{P\text{-}P}$, 10 STEP stair wave,
	Video In 2	Out 2	B	B								A	Chroma 40IRE
DP	Video In 1	Video	B	B								B	Input; 2.2$V_{P\text{-}P}$, 10 STEP stair wave
	Video In 2	Out 2	B	B					B			A	Chroma 40IRE
V_{HH} V_{HL}	Video In 1	$\overline{H_{SYNC}}$	B	B		B			A			B	Input; standard color bar signal, 2$V_{P\text{-}P}$
V_{VH} V_{VL}	Video In 1	$\overline{V_{SYNC}}$				A		B					Input; standard color bar signal, 2$V_{P\text{-}P}$
V_{SEPA}	Video In 1	$\overline{H_{SYNC}}$						A					Level from SYNC. signal top at T.P6
V_{TH}	Video In 1	$\overline{V_{SYNC}}$						B					Test at T.P7 & $\overline{V_{SYNC}}$ Pin (Note 1)
f_O	Video In 1	$\overline{H_{SYNC}}$	B	B	A	A	B	A	A	A	A	B	Count of frequency at $\overline{H_{SYNC}}$ output with SW11 to Ⓑ.
f_L	Video In 1	$\overline{H_{SYNC}}$					A/B						Input; standard color bar 2$V_{P\text{-}P}$ (Note 2)
f_C	Video In 1	$\overline{H_{SYNC}}$					A/B						Input; standard color bar, 2$V_{P\text{-}P}$ (Note 2)
P_W	Video In 1	$\overline{H_{SYNC}}$					A						Input; standard color bar, 2$V_{P\text{-}P}$ (Note 3)
P_D	Video In 1	$\overline{H_{SYNC}}$			A/B		A/B						Input; standard color bar 2$V_{P\text{-}P}$ (Note 3)

(Note 1)



(Note 3)





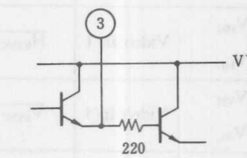
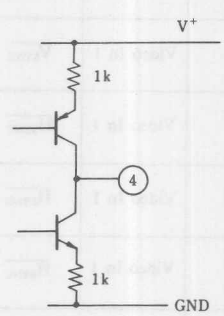
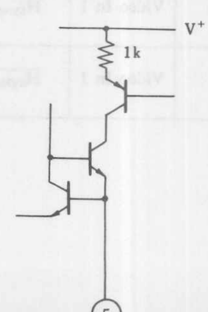
Choose smaller value Δf_{L1} or Δf_{L2}, and Δf_{C1} or Δf_{C2}

(Note 2): Lock Range: At that time from lock to unlock condition by changing variable resistor value, change SW5 to Ⓑ and measure frequency at $\overline{H_{SYNC}}$ output (upper and lower limit).

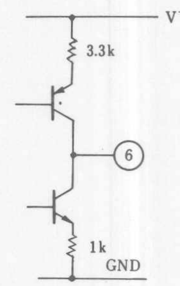
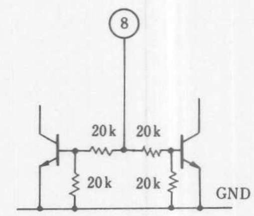
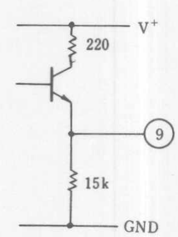
Capture Range: At that time from unlock to lock condition by changing variable resistor value, change SW5 to Ⓑ and measure frequency at $\overline{H_{SYNC}}$ output (upper and lower limit).

(Note 3): After adjusting $\overline{H_{SYNC}}$ output frequency to 15.73kHz with SW5 to Ⓑ, changing SW3 alternately with AFC and without AFC condition of $\overline{H_{SYNC}}$ and measure delay time of two signal rise and fall wave.

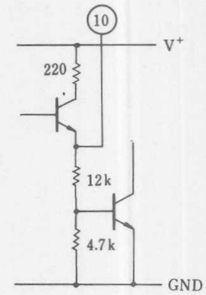
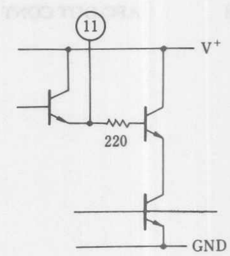
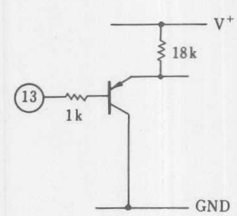
■ TERMINAL FUNCTION

PIN NO.	PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	NC	No connection	
2	NC	No connection	
3	VIDEO-IN 2	Video signal input terminal Sink chip clamp at 2.1V	
4	AFC-LPF	Connect AFC low pass filter.	
5	f FREE-CONT	Connect variable resistor and adjust free-run frequency.	

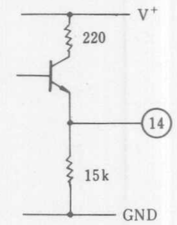
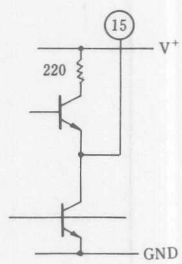
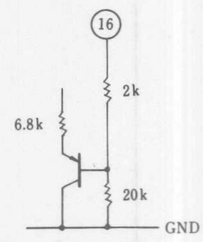
■ TERMINAL FUNCTION

PIN NO.	PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
6	VCO-OUT	Connect capacitor to decide VCO frequency.	
7	V+	Supply voltage	
8	AFC-OUT CONT	Control Pin 9 signal.	
9	Hsync-OUT	Horizontal synchronous signal output pin. Emitter follower output.	

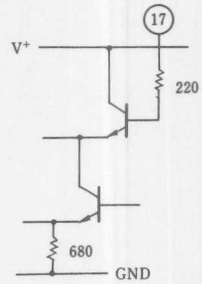
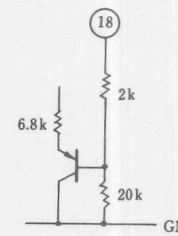
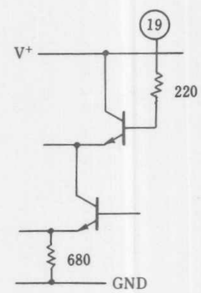
■ TERMINAL FUNCTION

PIN NO.	PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
10	Sync Sepa-OUT	Synchronous separation circuit output. When testing free run oscillation frequency, short to GND.	
11	Sync Sepa-IN	Synchronous separation circuit input.	
12	GND	Ground	
13	Vsync Sepa-IN	Vertical synchronous reproduce circuit input.	

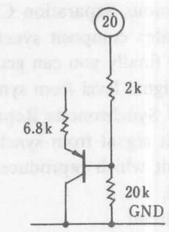
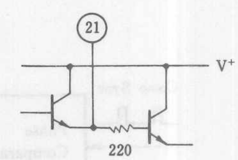
■ TERMINAL FUNCTION

PIN NO.	PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
14	Vsync-OUT	Vertical synchronous output. (Emitter follower output)	
15	VIDEO-OUT	Video signal output. (Emitter follower output)	
16	Charact-IN 1	Control pin of video SW-3.	

■ TERMINAL FUNCTION

PIN NO.	PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
17	Lum-CONT 2	Luminance level adjustment of pin 16 character signal	
18	Charact-IN 1	Control pin of video SW-2	
19	Lum-CONT 1	Luminance level adjustment of pin 18 character signal.	

■ TERMINAL FUNCTION

PIN NO.	PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
20	SW-CONT	Control pin of video SW-1. Input SW-1 output Low Video input 1 High Video input 2	
21	VIDEO-IN 1	Video signal input pin. Sink chip clamp at 2.1V.	
22	NC	No connection	

■ PRINCIPLES OF OPERATION

1) Video Switch

The NJM2217 has three video switches. One of them is used to select one video signal from two input video signal, and two others are used for super-imposer of character and background. Switching operation is done by putting DC voltage in to Pin 16,18 or 20, and its threshold voltage is 1.4V typical.

The NJM2217 has inside clamp circuit, and input video signal of Pin3 or Pin21 is sink-chip-clamped at 2.1V. Output circuit is emitter follower and drives to 5kΩ load.

2) Synchronous Separation Circuit

It separates composit synchronous signal from video signal, and this composit synchronous signal is applied to AFC circuit. And finally you can get horizontal synchronous signal (H_{sync}) from AFC circuit. Operation of synchronous separation is possible if signal level from synchronous signal top is more than $120mV_{p-p}$.

3) Vertical Synchronous Reproduce Circuit

Composit signal from synchronous separation circuit is applied to integrator and triangle wave from it goes to schmitt trigger circuit which reproduces vertical synchronous signal. Output circuit is emitter follower and output voltage is $4V_{P-P}$ at 2kΩ load.

4) AFC Circuit

Fig.3 shows block diagram of AFC circuit. Voltage proportional to phase difference between horizontal synchronous signal putted in to phase comparator and triangular wave from VCO is smoothed by low pass filter and is put in to VCO. This VCO frequency is changed to direction of coincidence with input frequency. Triangular wave from VCO output flows through window comparator and 5μs width of output pulse signal which is same width to H_{sync} appears.

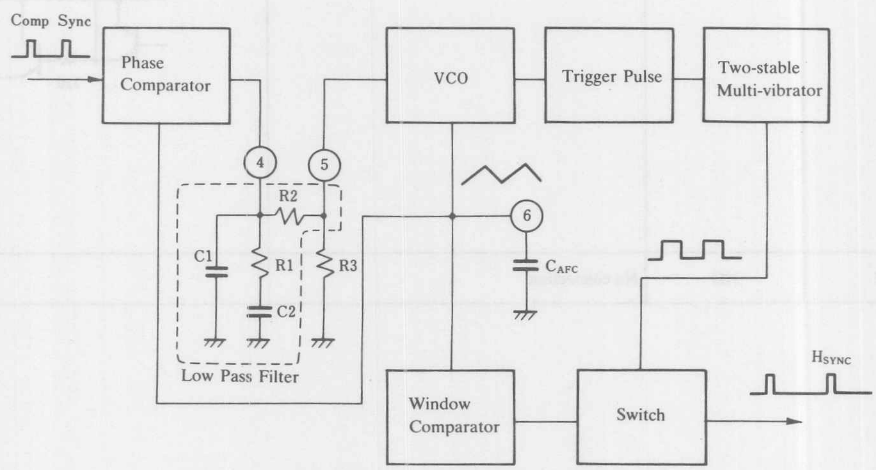


Fig.3 AFC Circuit Block

a) Free-Run Frequency

Free-run frequency depends on resistor R3 between Pin 5 and ground, and capacitor C_{AFC} between Pin6 and ground.

$$f_{FREE} = 1/(3.3 \cdot C_{AFC} \cdot R3)\,[Hz] \quad (1)$$

b) Parameter of Low Pass Filter
Impedance vs. frequency characteristic from Pin 4 to Pin 5 is shown on Fig.4.

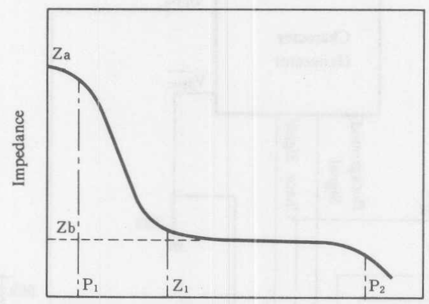


Fig.4 Low Pass Filter Impedance Characteristics

P_1, P_2, Z_1, Za, Zb are shown below.

$P_1 = 1/\{2\pi C_2(R_2+R_3)\}$ [Hz] (2)
$P_2 = 1/(2\pi C_1 \cdot R_1)$ [Hz] (3)
$Z_1 = 1/(2\pi C_2 \cdot R_1)$ [Hz] (4)
$Za = R_2 + R_3$ (5)
$Zb = R_1$ (6)

Za is decided by R_2 and R_3 is decided by free run frequency and so Za is generally decided by R_2. Value of P_1,P_2,Z_1,Za,Zb affects lock range, capture range, frequency fluctuations of AFC output and others. It is preferable that P_2 is 15kHz and Z_1 is 60Hz. When Zb becomes large, lock and capture range becomes wide but fluctuations of AFC output frequency will increase. Large Za decreases fluctuations.

■ DESIGN EXAMPLE OF L.P. FILTER

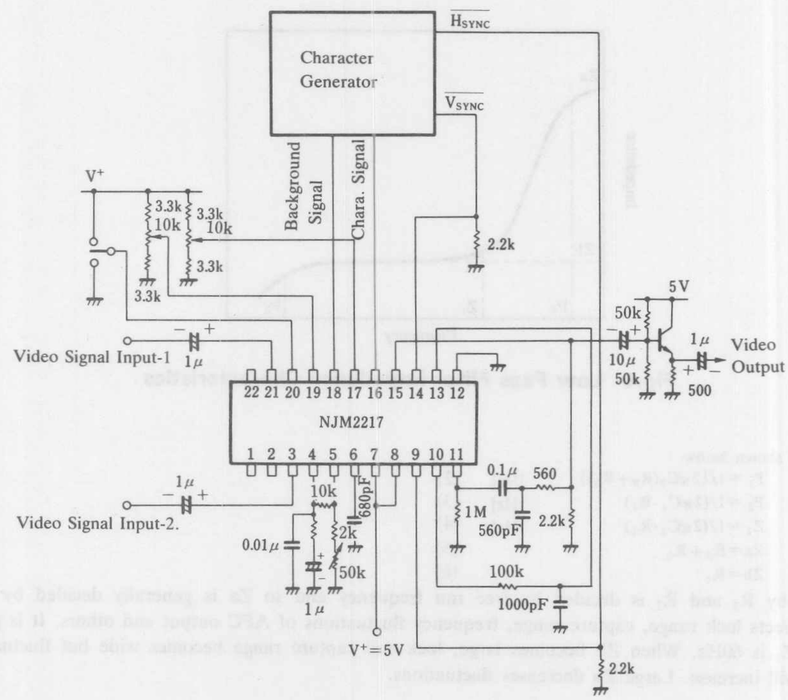
$P_1 = 2Hz$
$P_2 = 16kHz$
$Z_1 = 60Hz$
$Za = 40k\Omega$
$Zb = 1k\Omega$
$C_{AFC} = 680pF$

Each value of low pass filter is caluculated below. If decided free run frequency to 15.74kHz, and from equation (1).
$R_3 = 28.4k\Omega$
$Za = 40k\Omega$ and equation (5),
$R_2 = 12k\Omega$
From equation (2),
$C_2 = 2.1\mu F$
From equation (4),
$R_1 = 1.3k\Omega$
From equation (3)
$C_1 = 7700pF$
Measured value at $R_1=1k\Omega$, $R_2=10k\Omega$, $C_1=1\mu F$, $C_2=2.2\mu F$.
Lock range=3.3kHz
Capture range=1.7kHz

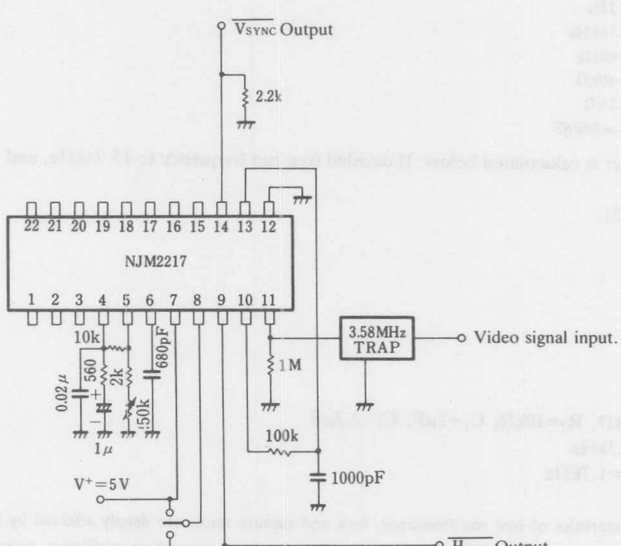
(Note) Temperature characteristics of free run frequency, lock and capture range are deeply affected by temperature coefficient of C_{AFC} and each device of low pass filter, and so it is preferable using low temperature coefficient device. If temperature coefficient of C_{AFC} and R_3 is 0ppm/°C temperature coefficient of free run frequency is almost 0ppm/°C. (Ref. to typical characteristics graph.)

■ TYPICAL APPLICATION

Character superimposer on video signal.



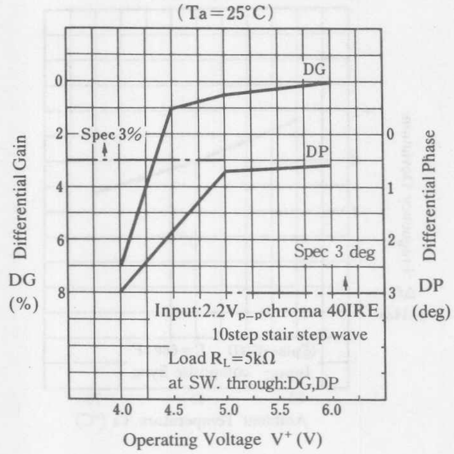
Synchronous separation of video signal.



■ TYPICAL CHARACTERISTICS

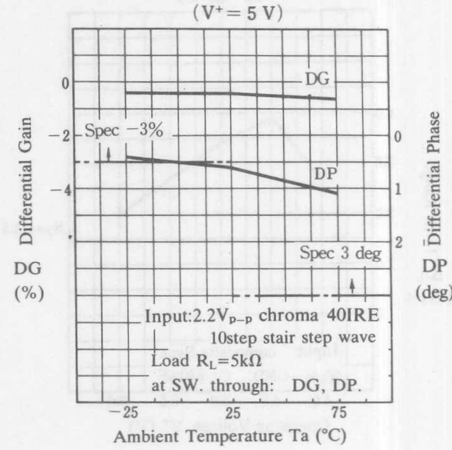
Differential Gain/Differential

(Ta=25°C)



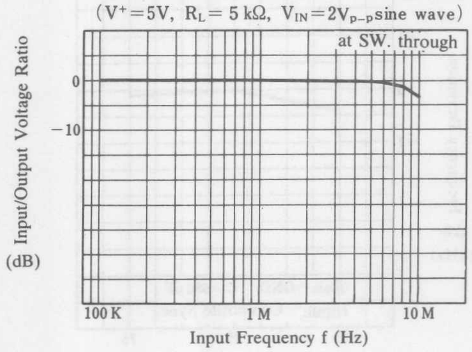
Differential Gain/Differential Phase

(V+= 5 V)



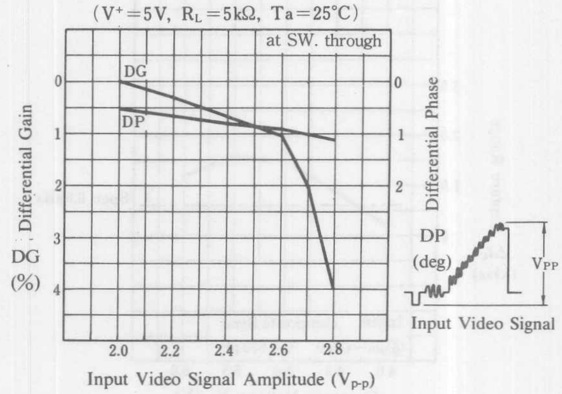
Video Switch Frequency Response

(V+=5V, RL= 5 kΩ, VIN=2Vp-psine wave)



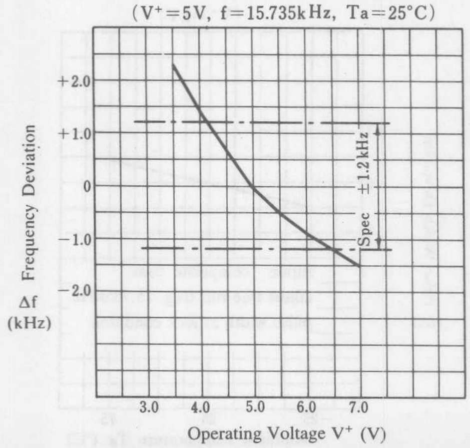
Differential Gain/Differential Phase

(V+=5V, RL=5kΩ, Ta=25°C)



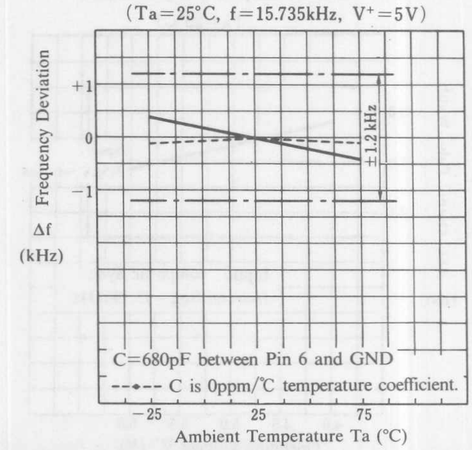
AFC Free Run Frequency

(V+=5V, f=15.735kHz, Ta=25°C)



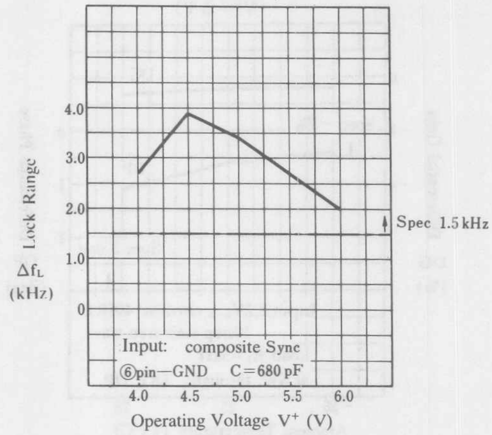
AFC Free Run Frequency

(Ta=25°C, f=15.735kHz, V+=5V)

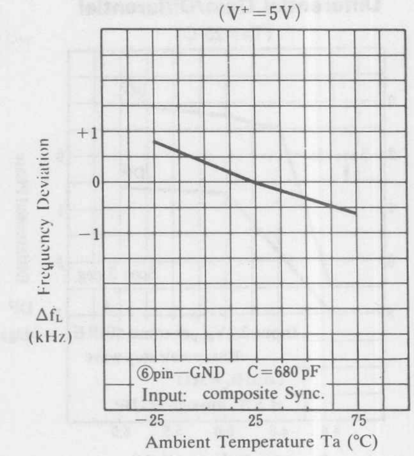


■ TYPICAL CHARACTERISTICS

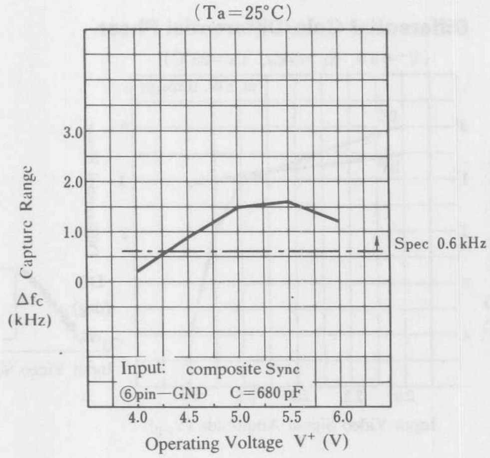
Lock Range
(Ta=25°C)



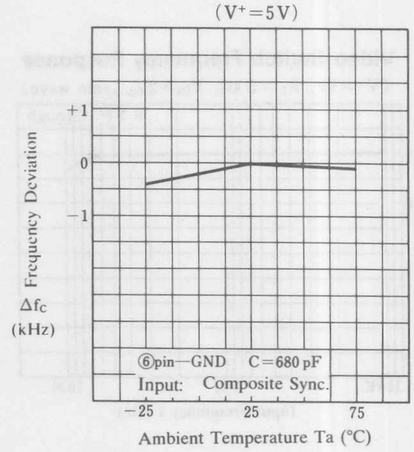
Lock Range
(V+=5V)



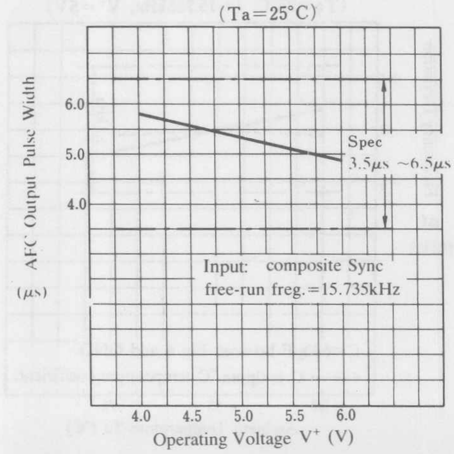
Capture Range
(Ta=25°C)



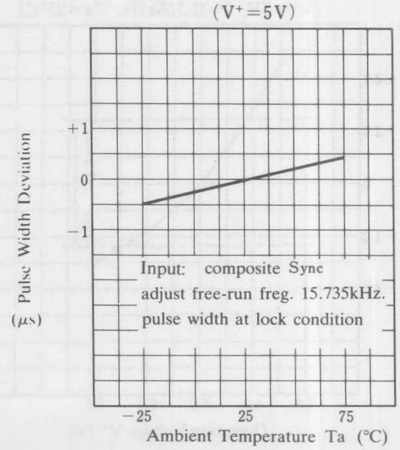
Capture Range
(V+=5V)



AFC $\overline{\text{Hsync}}$ Pulse width
(Ta=25°C)



AFC $\overline{\text{Hsync}}$ Pulse Width
(V+=5V)



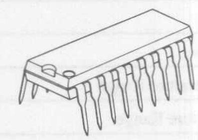
NTSC-M/PAL CONVERTOR

■ GENERAL DESCRIPTION

The NJM2218 is a signal processing IC for M/PAL Video signal. It is possible to convert from NTSC signal to M/PAL signal.

The NJM2218 has functions of Video Sub-Carrier Doubler Block, Synchronous Signal AFC Block, Logic Block, Convert Block and Video Switch Block.

■ PACKAGE OUTLINE



NJM2218D

■ FEATURES

- 1chip NTSC-M/PAL convertor
- Internal AFC block
- Package Outline DIP18
- Operating Voltage (+4.5V~5.5V)
- Bipolar Technology

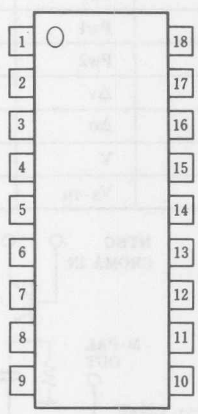
■ RECOMMENDED OPERATING CONDITION

- Operating Voltage V⁺=+4.5V~+5.5V

■ APPLICATION

- TV, VCR

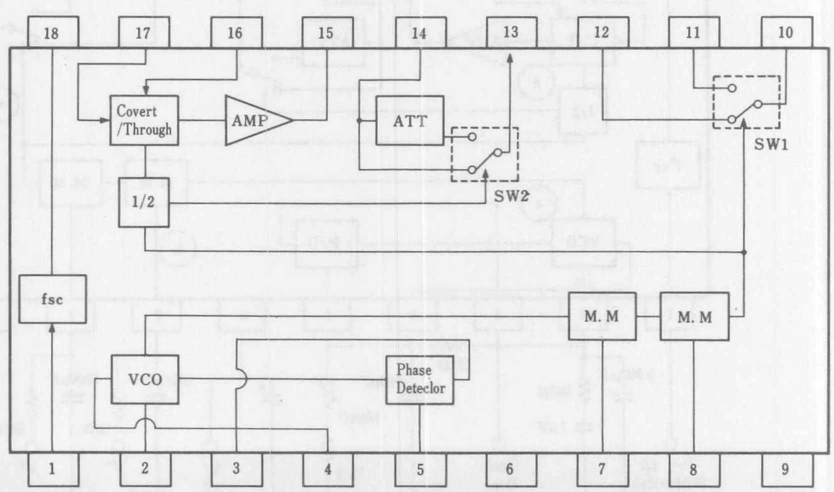
■ PIN CONFIGURATION



NJM2218D

1)fsc Input
2)VCO Control
3)COMP. SYNC Input
4)VCO Filter
5)Phase Detect Filter
6)V⁺
7)Mono Multi C/R(1)
8)Mono Multi C/R(2)
9)GND
10)Switch 1
11)45deg Phase Shift Input
12)NTSC Chroma Input
13)M/PAL Output
14)Switch 2 Input
15)Convert/Through Output
16)Convert/Through Input
17)BPF Output
18)2fsc Output

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

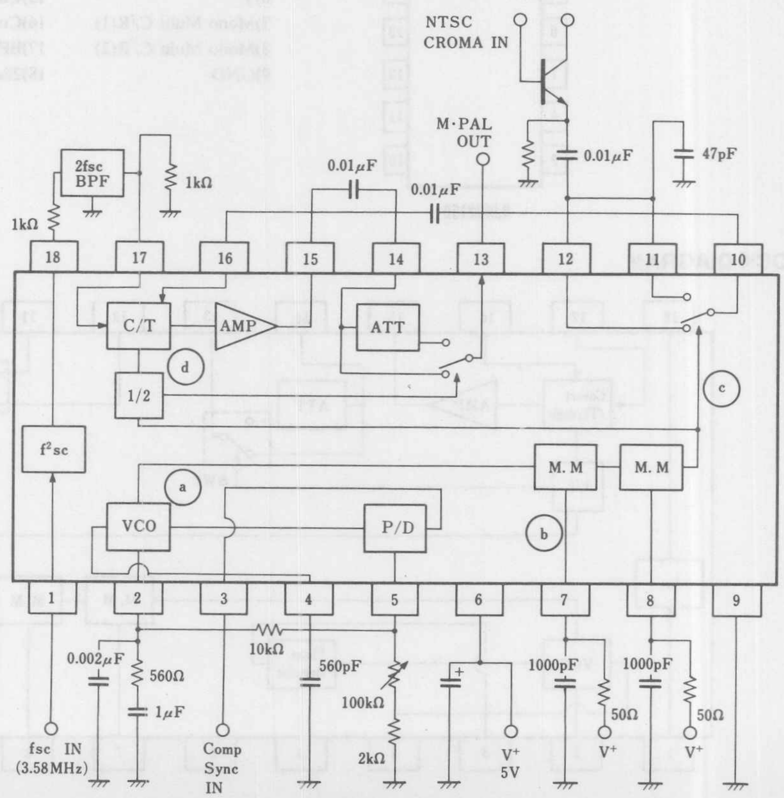
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+10	V
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	−20〜+75	℃
Storage Temperature Range	T_{stg}	−40〜+125	℃

■ ELECTRICAL CHARACTERISTICS

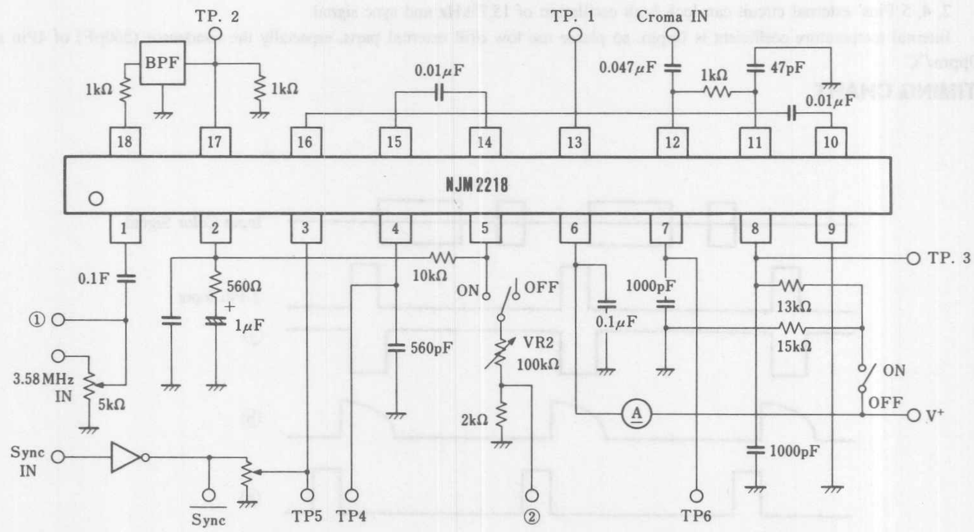
(V^+=50V, Ta=25℃)

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Current		I_{CC}	—	20	28	mA
Signal Doubler Gain		G2fsc	−1.4	+0.6	+2.6	dB
AFC Characteristic	Free-Run Frequency	$f\,f_H$	18.0	20.0	—	kHz
		$f\,f_L$	—	11.0	18.5	kHz
	Lock Range	Δfl	3.0	5.0	—	kHz
	Capture Range	Δf_C	0.8	1.3	—	kHz
Mono Multi Characteristic	Pulse Deley Time	P_{DT}	−0.7	3.0	13.0	μs
	Pulse Wide (1)	Pw1	7.0	9.0	11.0	μs
	Pulse Wide (2)	Pw2	8.0	10.0	12.0	μs
M/PAL Convert Characteristic	Offset Voltage	Δv	0	20	80	mV
	Gain Difference	Δ_G	2.0	5.0	8.0	dB
	M/PAL Convert Gain	V	−3.0	−1.0	1.0	dB
SyncThreshold Level		V_{S-TH}	0.7	1.4	2.0	V

■ APPLICATION



■ TEST CIRCUIT



■ BLOCK EXPLANATIOR

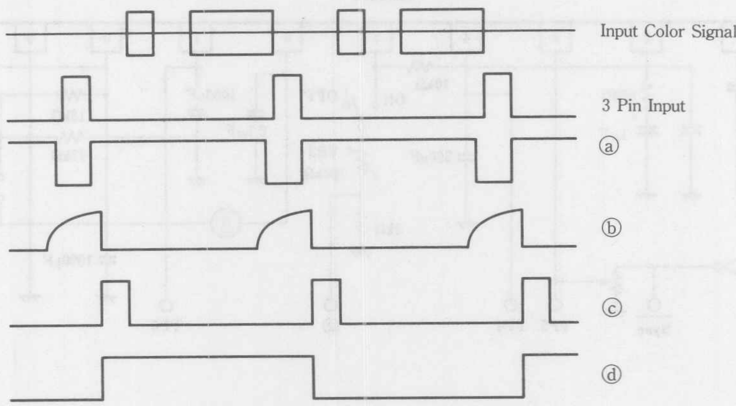
- AFC, M/M BLOCK

3 Pin input is Positive Composite Sync Signal

2, 4, 5 Pins' external circuit can lock both oscillation of 15.75kHz and sync signal.

Internal temperature coefficient is 0ppm, so please use low drift external parts, especially the condensor (560pF) of 4Pin should be 0ppm/°C

■ TIMING CHART



- SIGNAL DOUBLER BLOCK

3.58 (fsc)×2=7.16MHz generator

1 Pin: 100~200mVp-p input pin

18 Pin: about +0.6dB (GAIN) output pin

- SW1 BLOCK

12 Pin: NTSC COLOR SIGNAL (100~200mV$_{p-p}$) input pin

10 Pin: 45deg Phase shift Color Burst Signal output pin

- CONVERT/THROUGH, AMPLIFIER, ATT, SW2 BLOCK

16 Pin: NTSC Color Signal (Phase Shift Color Burst) input pin

17 Pin: 7.16MHz (fsc×2) input pin

M/PAL Signal is output from 13 Pin through the Amplifier and ATT Block.

VIDEO SYNCHRONOUS DETECTOR

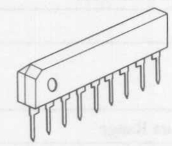
■ GENERAL DESCRIPTION

The NJM2220/2230 discriminate existance and fineness of video signal. It is applicable to VCR, TV, Video camera, Hi-Fi VCR, on screen display and others.

■ FEATURES

- Operating Voltage (+4.5V~+13V)
- Package Outline DMP8, SIP9
- Bipolar Technology

■ PACKAGE OUTLINE



NJM2220S

NJM2230M

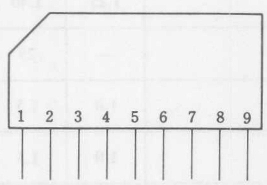
■ RECOMMENDED OPERATING CONDITION

- Operating Voltage : V^{+}=4.75~10V

■ APPLICATION

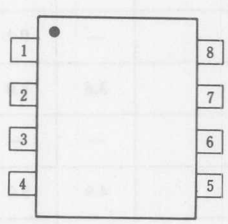
- Video camera, other video equipment

■ PIN CONFIGURATION



NJM2220S

PIN FUNCTION
1. M.M Time Constant set
2. SYNC Input (Comp, N, V SYNC)
3. SYNC Output
4. SSG SYNC Input
5. GND
6. SYNC DET, Judgement Control
7. SYNC DET
8. M.M Smoothing
9. V^{+} 5~10V



NJM2230M

PIN FUNCTION
1. M.M Time Constant Set
2. SYNC Input (Comp, H, V SYNC)
3. SYNC Output
4. SSG SYNC Input
5. GND
6. SYNC DET, Judgement Control
7. M.M Smoothing
8. V^{+} 5~10V

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	12	V
Power Dissipation	P_D	(SIP9) 500	mW
		(DMP8) 300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

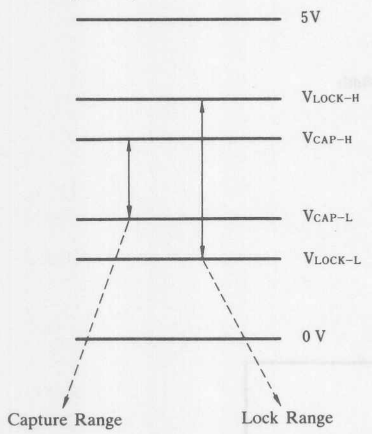
■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current		I_{CC}		—	8	11	mA
Schmitt Circuit CAP Voltage	H side	$V_{CAP\text{-}H}$	(Note 1)	2.07	2.22	2.37	V
	L side	$V_{CAP\text{-}L}$	(Note 1)	1.57	1.72	1.87	V
Schmitt Circuit LOCK Voltage	H side	$V_{LOCK\text{-}H}$	(Note 1)	2.53	2.68	2.83	V
	L side	$V_{LOCK\text{-}L}$	(Note 1)	1.25	1.40	1.55	V
Mono-Multi Output Width		W_{MM}	(Note 2)	—	25	—	μsec
Input Threshold Level	2P	$V_{TH\text{-}2}$		1.0	1.5	2.0	V
	4P	$V_{TH\text{-}4}$		1.0	1.5	2.0	V
	6P	$V_{TH\text{-}6}$		—	0.8	1.4	V
Output Voltage Pin 7	H side	$V_{7\text{-}H}$		4.9	5.0	—	V
	L side	$V_{7\text{-}L}$		—	0.1	0.3	V
Output Voltage Pin 6	H side	$V_{6\text{-}H}$		3.6	4.0	—	V
	L side	$V_{6\text{-}L}$		—	—	0.1	V
Output Voltage Pin 3	H side	$V_{3\text{-}H}$		4.9	5.0	—	V
	L side	$V_{3\text{-}L}$		—	0.1	0.3	V
M.M Smoothed D.C. Voltage		V_8 (V_7)	Pin 2=2V	2.9	3.2	3.5	V

( ): Apply to 2230M

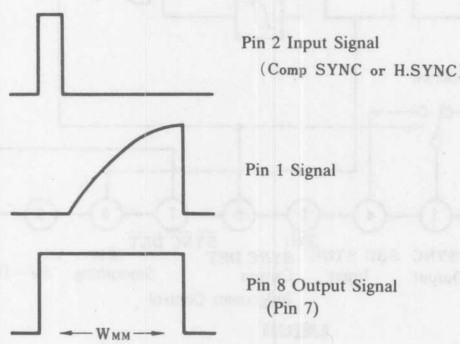
(Note 1)



ITEM	V_{CAP-L} V_{LOCK-H} V_{CAP-H} V_{LOCK-L}
Pin 8 Voltage (Pin 7)	0 → 5 → 0
Pin 6 Voltage	L → H → L → H → L
Pin 7 Voltage	H → L → H → L → H

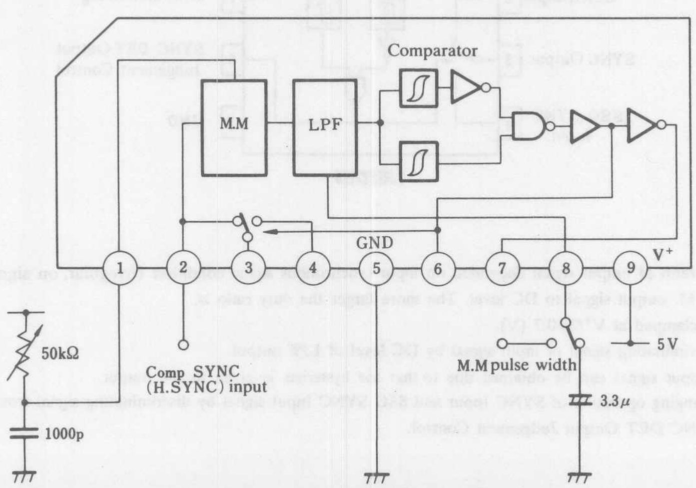
Measure Pin 8 (Pin 7) DC voltage at a moment when Pin 6 output voltage turns state.

(Note 2)

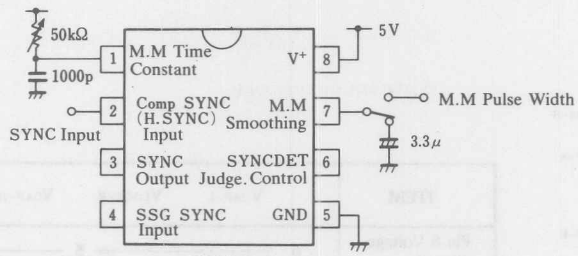


Adjust Pin 8 (Pin 7) DC Voltage to 2V (at V^{+}=5V) by varying Pin 1 outer resistor, and test Pin 8 output pulse width after taking off Pin 8 outer capacitor.

■ TEST CIRCUIT

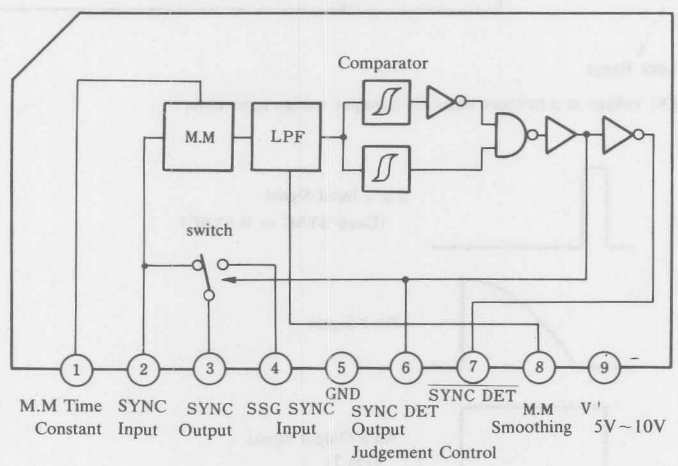


NJM2220S

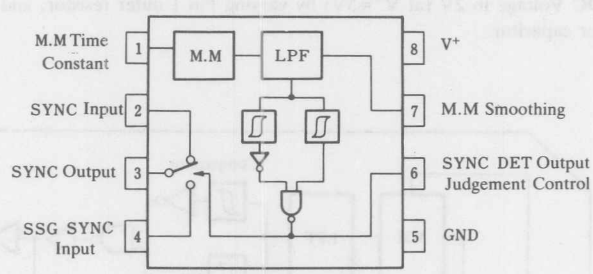


NJM2230M

■ OPERATIVE PRINCIPLE



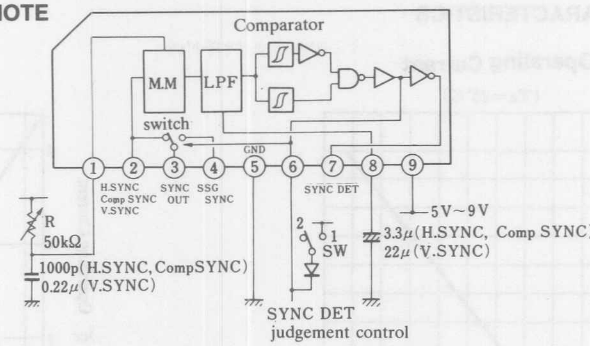
NJM2220S



NJM2220M

- M.M: Varies duty ratio of output signal depended on input synchronous signal condition (irregular, on signal).
- LPF: Converts M.M. output signal to DC level. The more larger the duty ratio is, DC level is clamped at $V^+/2+0.7$ (V).
- Comparator: Outputs discriminating signal of input signal by DC level of LPF output. Stablized output signal can be obtained due to that the hysterises is given to the output.
- Switch: Makes exchanging operation of SYNC Input and SSG SYNC Input signal by discriminating signal from comparator or Pin 6 signal of SYNC DET Output Judgement Control.

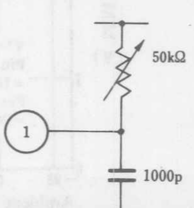
■ TYPICAL APPLICATION NOTE

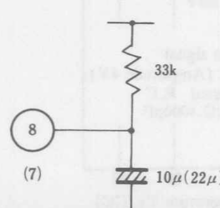


■ TERMINAL FUNCTION

PIN NO.	EXPLANATION
1	Connect resistor and capacitor for M.M. time constant. (Value of R, C is changed by a kind of Pin 2 SYNC Input signal.)
2	Input synchronous signal (Comp SYNC, H.SYNC or V.SYNC) separated from video signal.
3	It outputs Pin 2 or Pin 4 signal by Pin 2 signal condition. ● Pin 2 input signal; normal → Output Pin 2 input signal. ● Pin 2 input signal; abnormal → Output Pin 4 input signal.
4	Input artificial synchronous signal generated by SSG (Sync. Signal Generator).
5	GND
6	It outputs DC voltage (H or L state) by Pin 2 signal condition. When outer SW is turned to 1, Pin 2 input signal is forced to flow out from Pin 3. ● Pin 2 input signal; normal → H state ● Pin 2 input signal; abnormal → L state
7	It outputs DC voltage (H or L state) by Pin 2 signal condition. ● Pin 2 input signal; normal → L state ● Pin 2 input signal; abnormal → H state
8 (7)	Connect capacitor for smoothing M.M. (Value depends on Pin 2 input signal). Adjust Pin 1 attached volume to the level that Pin 8 voltage becomes 2V (V^+=5V) with Pin 2 signal If V^+>5V, then $V_{8(7)}=2/5V^+$ (V)
9(8)	V^+: 5~10V

(Note) In some application,it happens that still,search or tracking is large off the point and unordinary SYNC or lack of SYNC occurs. If it is not desirable, you can do in SYNC condition by using Pin 6 as control input terminal. Also recommend sensitivity adjust ment of outer device change, by it error detection of unordinary SYNC will lapse.
It makes volume to low value,in other word it makes time constant of M.M to low value.In this case synchronous peak voltage at Pin 8 (Pin 7) becomes lower and so makes to 2V (V^+=5V) by putting resistor in to V^+.
(Adjust to 2V by Pin 1 resistor attached.)

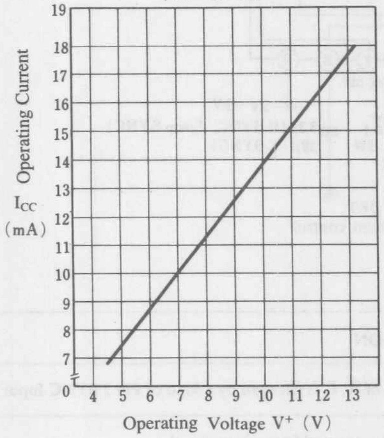




■ TYPICAL CHARACTERISTICS

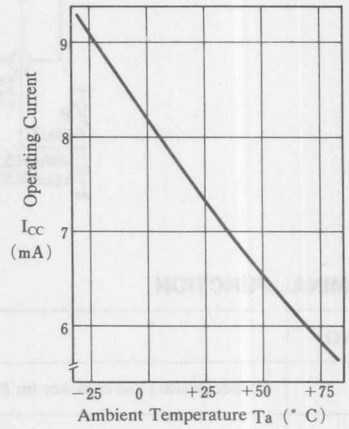
Operating Current

(Ta=25°C)



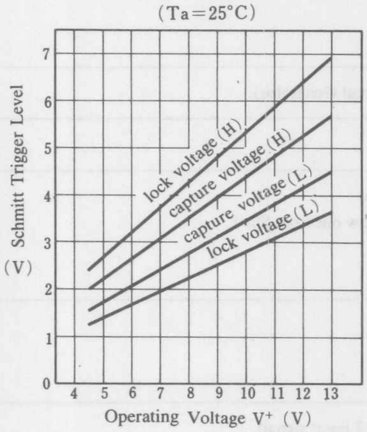
Operating Current

(V^+=5V)



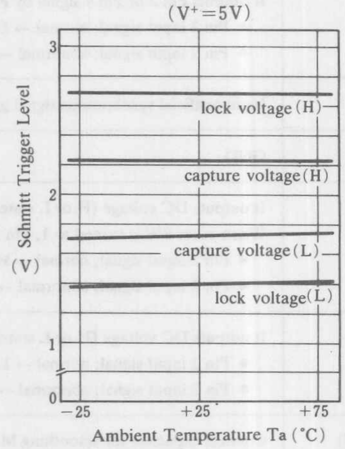
Schmitt Trigger Level

(Ta=25°C)



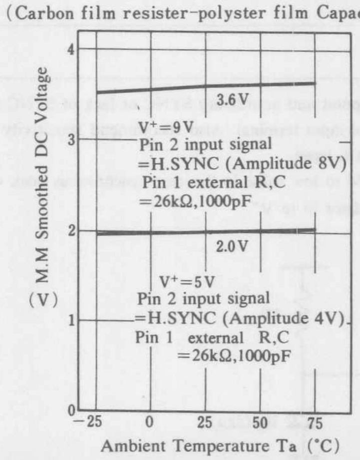
Schmitt Trigger Level

(V^+=5V)



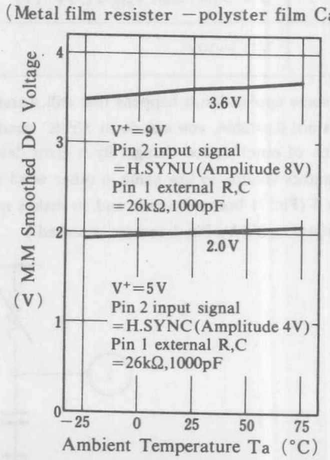
M.M Smoothed DC Voltage

(Carbon film resister-polyster film Capacitor)



M.M Smoothed DC Voltage

(Metal film resister −polyster film Capacitor)



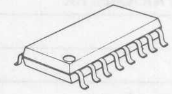
VIDEO SWITCH WITH 8dB AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2223 is an integrated bipolar video switch with 8dB amplifier which selects one video signal from three different composit video signals.

The NJM2223 has also function of superimposer and synchronous signal clipping and is suit to picture in picture configuration

■ PACKAGE OUTLINE

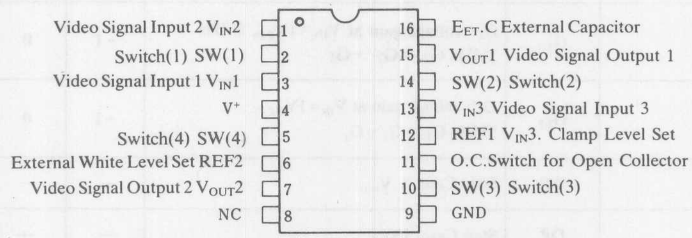


NJM2223M

■ FEATURES

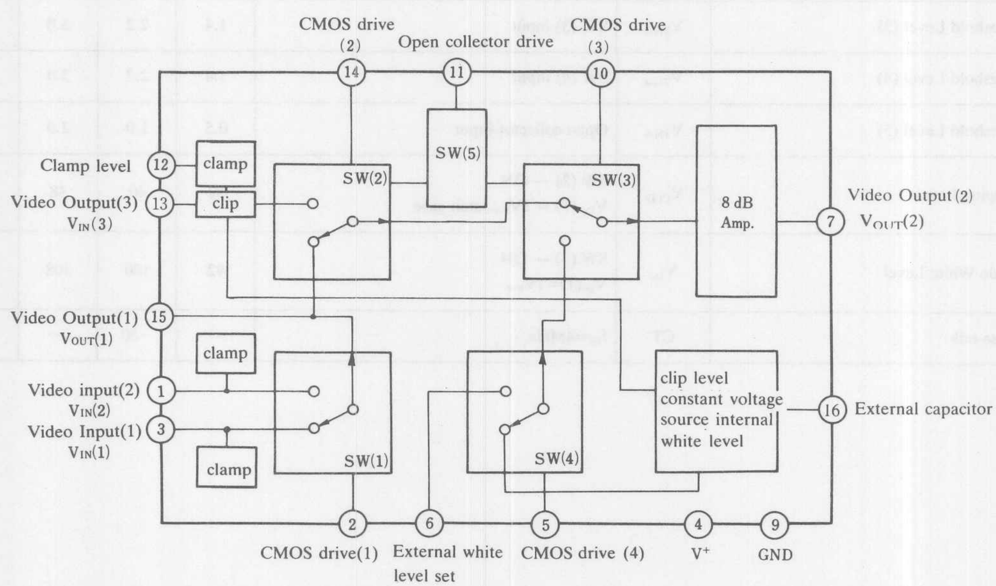
- 12V operation.
- 3 input video signal.
- 2 output video signal.
- Switch operates with CMOS level.
- Super imposer function.
- Intemal 8dB Amp.
- Package Outline DMP16
- Bipolar Technology

■ PIN CONFIGURATION



NJM2232M

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DMP16) 300	mW
Operating Temperature Range	Topr	−20～+75	℃
Storage Temperature Range	Tstg	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V⁺=12V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}		—	14	19	mA
Voltage Gain (1)	G_1	V_{IN}=1MHz, 1V_{P-P}	−1	0	1	dB
Voltage Gain (2)	G_2	V_{IN}=1MHz, 1V_{P-P}	7	8	9	dB
Frequency Charact. (1)	G_{1-1}	G_2 ':voltage gain at V_{IN}=1V_{P-P}, 5MHz 5MHz $G_{2-2}=G_2'-G_2$	−1	0	1	dB
Frequency Charact. (2)	G_{2-2}	G_1': voltage gain at V_{IN}=1V_{P-P}, 5MHz $G_{1-1}=G_1'-G_1$	−1	0	1	dB
Differential Gain	DG	Stair Case, 1 V_{P-P}	—	—	3	%
Differential Phase	DP	Stair Case, 1V_{P-P}	—	—	3	deg
Threshold Level (1)	V_{TH-1}	SW (1) input	1.4	2.2	3.0	V
Threshold Level (2)	V_{TH-2}	SW (2) input	1.4	2.2	3.0	V
Threshold Level (3)	V_{TH-3}	SW (3) input	1.4	2.2	3.0	V
Threshold Level (4)	V_{TH-4}	SW (4) input	1.4	2.2	3.0	V
Threshold Level (5)	V_{TH-5}	Open collector input	0.5	1.0	2.0	V
Clipping Level	V_{CLIP}	SW (2) — ON V_{IN} (1) = 1V_{P-P}, stair case	32	40	48	IRE
Inside White Level	V_{IN}	SW (3) — ON V_{IN}(1)=1V_{P-P}	92	100	108	IRE
Cross-talk	CT	f_{IN}=4MHz	—	−50	—	dB

■ OUTPUT SELECT CODE

● Video Output (1)

SW (1)	V_{OUT} (1) Output Signal
0	V_{IN} (1)
1	V_{IN} (2)

● Video Output (2)

SW (1)	SW (2)	SW (3)	V_{OUT}(2) Output Signal
0	0	0	V_{IN} (1)
0	1	0	V_{IN} (3)
1	0	0	V_{IN} (2)
1	. 1	0	V_{IN} (2)

● Super Imposer

1. Switching of SW (3), it imposes DC level in video signal regardless to SW (1), SW (2) Condition.

SW (3)	V_{OUT} (2) Output Signal
0	Video Signal
1	DC Level

2. Switching of SW (4), it selects DC level at internal white level (100 IRE) or external setting level.

SW (4)	V_{OUT} (2) Output Signal
0	Internal White Level
1	External Set Level

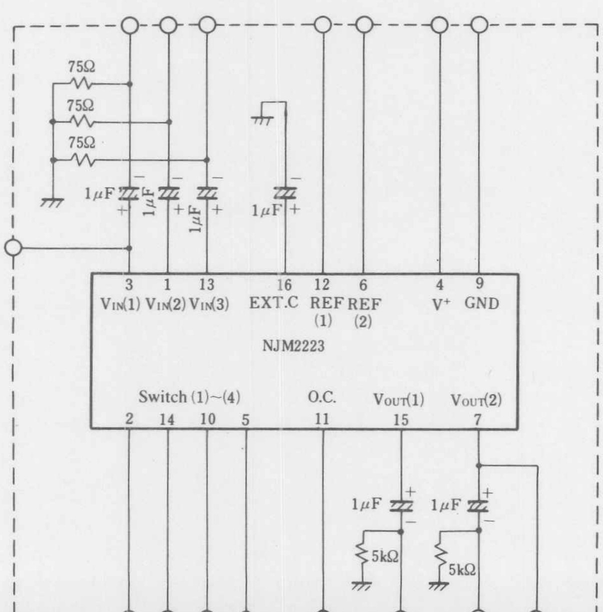
● Open Collector Drive Switch

This switch has function to make SW (2), SW (3) no working and V_{OUT} (2) output signal to the same output signal of V_{OUT} (1). It operates in CMOS level.

■ TERMINAL FUNCTION

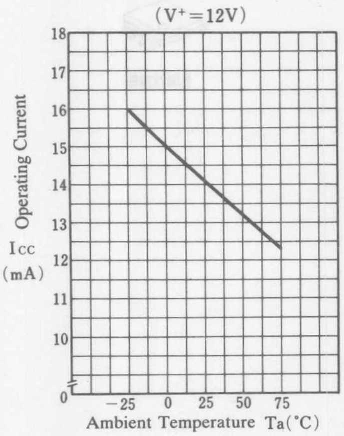
PIN.	EQUIVALENL CCT	PIN.	EQUIVALENT CCT
1 $V_{IN}2$	V^+	9 GND	—
2 SW(1)	GND	10 SW(3)	GND
3 $V_{IN}1$	V^+	11 open. O.C.	V^+ GND
4 V^+		12 REF1	V^+ GND
5 SW(4)	GND	13 $V_{IN}3$	V^+
6 REF2	V^+	14 SW(2)	GND
7 $V_{OUT}2$	V^+ GND	15 $V_{OUT}1$	V^+
8 NC	—	16 $E_{FT}.C$	V^+ GND

■ TEST CIRCUIT

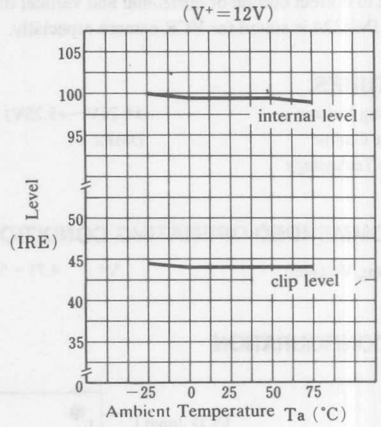


■ TYPICAL CHARACTERISTICS

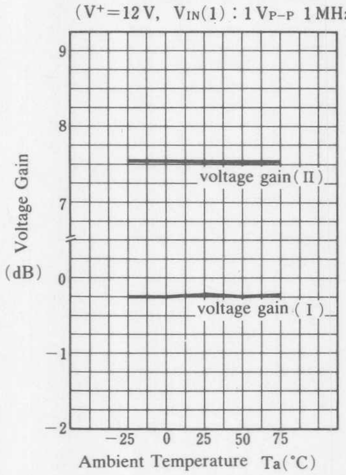
Operating Current



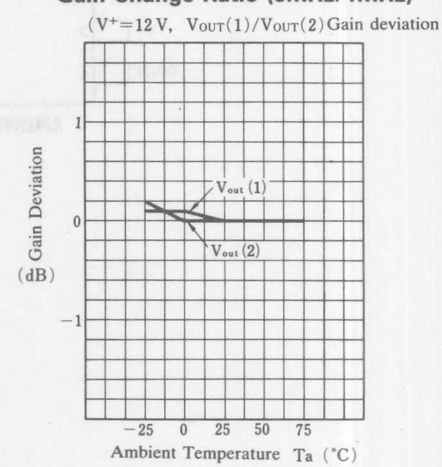
Clipping/Internal Level



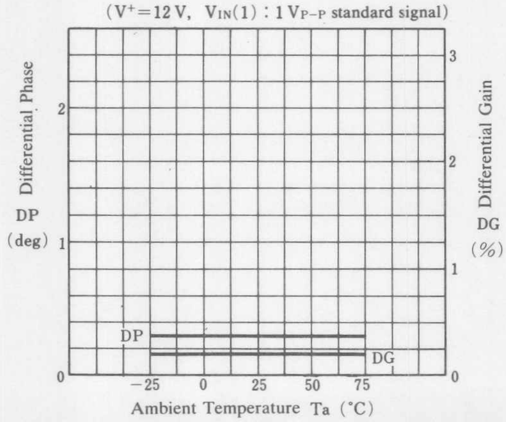
Voltage Gain (1),(2)



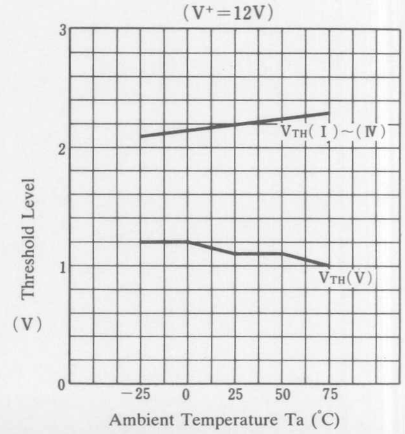
Gain Change Ratio (5MHz/1MHz)



Differential Gain/Differential Phase



Threshold Level

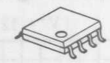


■ GENERAL DESCRIPTION

The NJM2224 is a video noise reducer IC of which operation is to reduce noise contained in video color and luminance signal, and at the same time to correct outline of horizontal and vertical image signal.

The NJM2224 is suited for VCR camera especially.

■ PACKAGE OUTLINE



NJM2224M

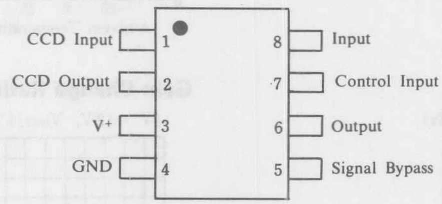
■ FEATURES

- Operating Voltage (+4.75V~+5.25V)
- Package Outline DMP8
- Bipolar Technology

■ RECOMMENDED OPERATING CONDITION

- Operating Voltage V^+ 4.75~5.25V

■ PIN CONFIGURATION



NJM2224M

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

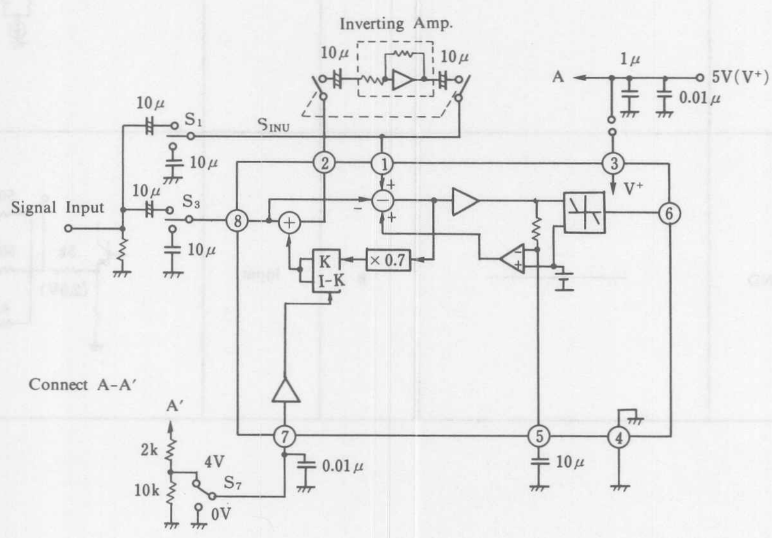
■ ELECTRICAL CHARACTERISTICS

(V^+=5V, f=100kHz, Ta=25℃)

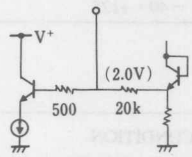
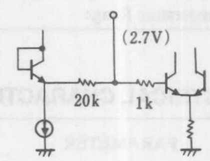
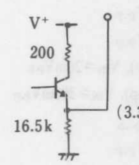
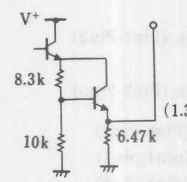
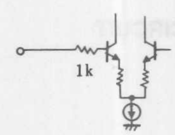
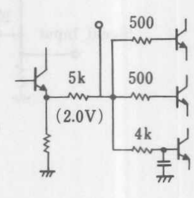
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}		—	6.9	10	mA
Voltage Gain (Pin8-Pin2)	A_{U11}	V_7=4V, V_{IN}=100mV_{P-P}	−1	0	+1	dB
	A_{U12}	V_7=0V, V_{IN}=100mV_{P-P}	−11.5	−10	−8.5	
Voltage Gain (Pin1-Pin2)	A_{U21}	V_7=4V, V_{IN}=100mV_{P-P}	—	−45	−38	dB
	A_{U22}	V_7=0V, V_{IN}=100mV_{P-P}	−4.2	−3.2	−2.2	
Voltage Gain (Pin8-Pin6)	A_{U31}	V_7=4V, Pin2−1(Inv. Amp), V_{IN}=20mV_{P-P}	—	—	−20	dB
	A_{U32}	V_7=4V, Pin2−1 (Inv. Amp), V_{IN}=300mV_{P-P}	−5	−3	−1	
Bandwidth (Pin8-Pin2)	f_{B1}	V_7=4V, V_{IN}=100mV_{P-P}	10	—	—	MHz
Bandwidth (pin1-pin2)	f_{B2}	V_7=0V, V_{IN}=100mV_{P-P}	10	—	—	MHz
Bandwidth (Pin8-Pin6)	f_{B3}	V_7=4V, V_{IN}=100mV_{P-P}	8	—	—	MHz
Pin6 DC Voltage	V_{6-DC}		—	1.3	—	V

Note: Unless specified, all items are tested by Test Circuit.

■ TEST CIRCUIT



■ TERMINAL FUNCTION

PIN NO.	PIN NAME	INSIDE EQUIVALENT CIRCUITS	PIN NO.	PIN NAME	INSIDE EQUIVALENT CIRCUITS
1	CCD Input		5	Signal Bypass	
2	CCD Output		6	Output	
3	V+	—	7	Control Input	
4	GND	—	8	Input	

■ APPLICATION NOTE

The NJM2224 is an integrated circuit of composing variable comb type filter which reduces noise mixed in chroma or luminance signal of VCR camera and others. The CCD delay device is suitable for outside delay element composing comb type filter, compared with a glass delay device. The basic circuit is the most excellent FB system with NULL.

Fig.1 is its basic block diagram and Fig.2 is actual block diagram of NJM2224.

Fig.3 is one of application examples.

The video noise reducer system is composed of three capacitors for connection and one capacitor for signal bypass and CCD delay device. The NJM2224 is applicable to both of chroma and luminous signal using CCD delay device suitable for each signal. High level input to the Control of Reduce/Enhance terminal (Pin7) makes enhance mode (increasing of high frequency part) and Low level input makes reduce mode (decreasing of high frequency part.) Its threshold level is about 2.25V at 5V supply voltage. Basic operating characteristics is shown in Fig.4.

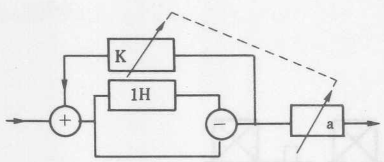


Fig. 1 Basic Block Diagram

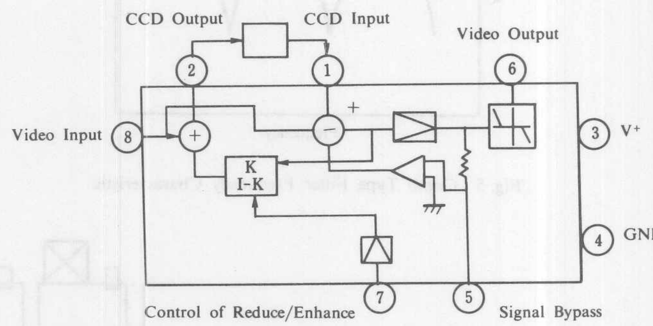


Fig. 2 Block Diagram

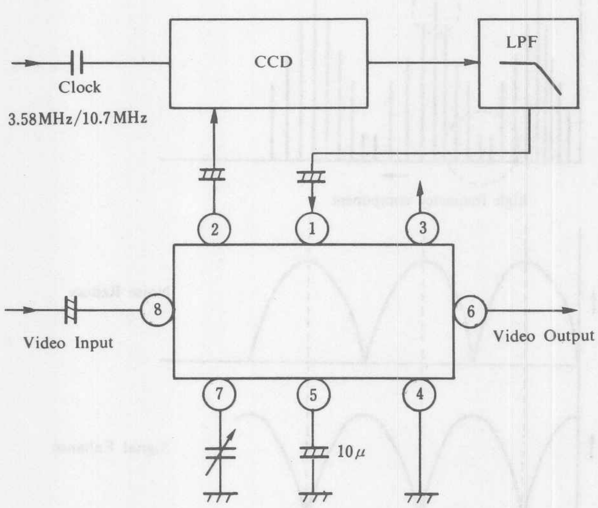


Fig. 3 Application

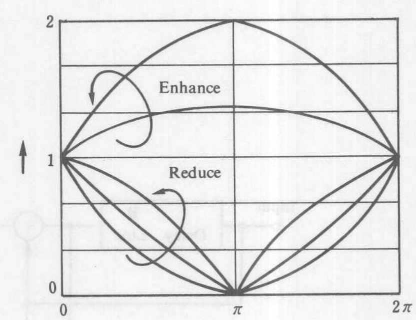


Fig. 4 Basic Operating Characteristic

The comb type filter has special frequency characteristics shown Fig.5, and is widely used to separate luminance and color signal in video-signal circuit. Using this comb type filter, the NJM2224 reduces noise and enhances signal in video signal, automatically.

Fig.6 shows video signal wave form and its frequency component.

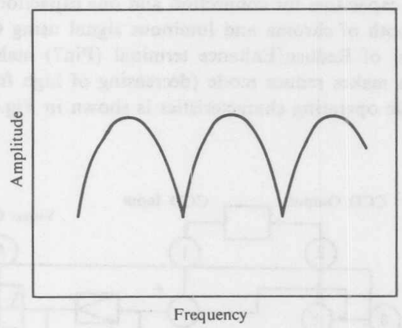


Fig. 5 Comb Type Filter Frequency Characteristic

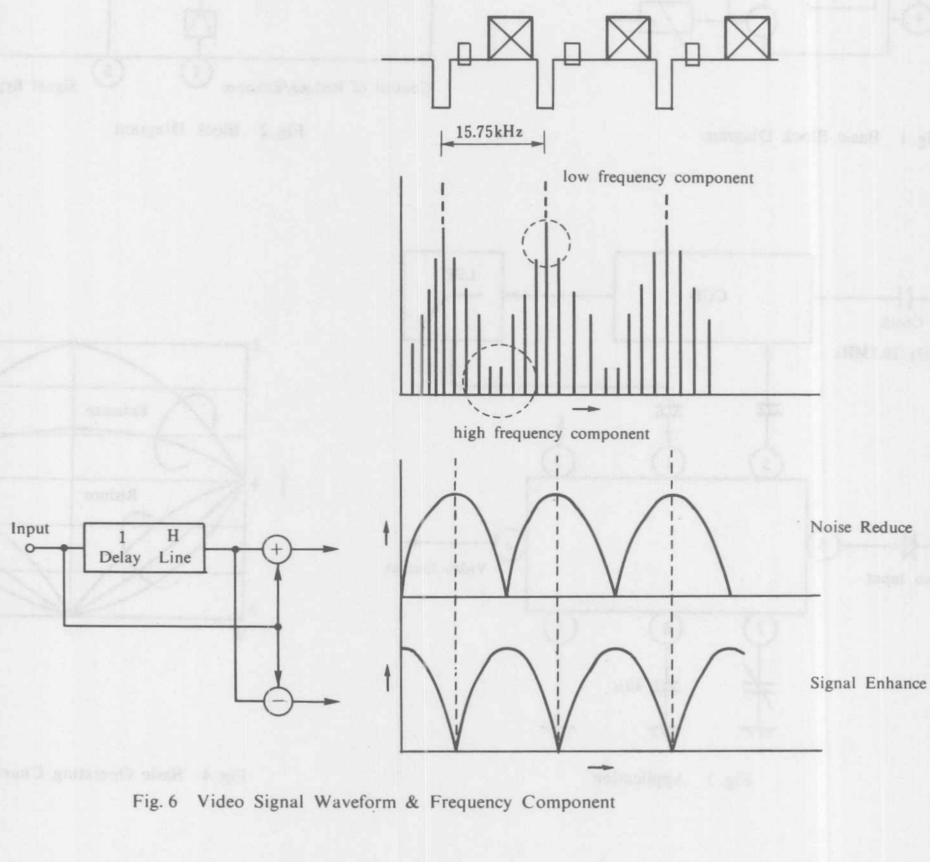
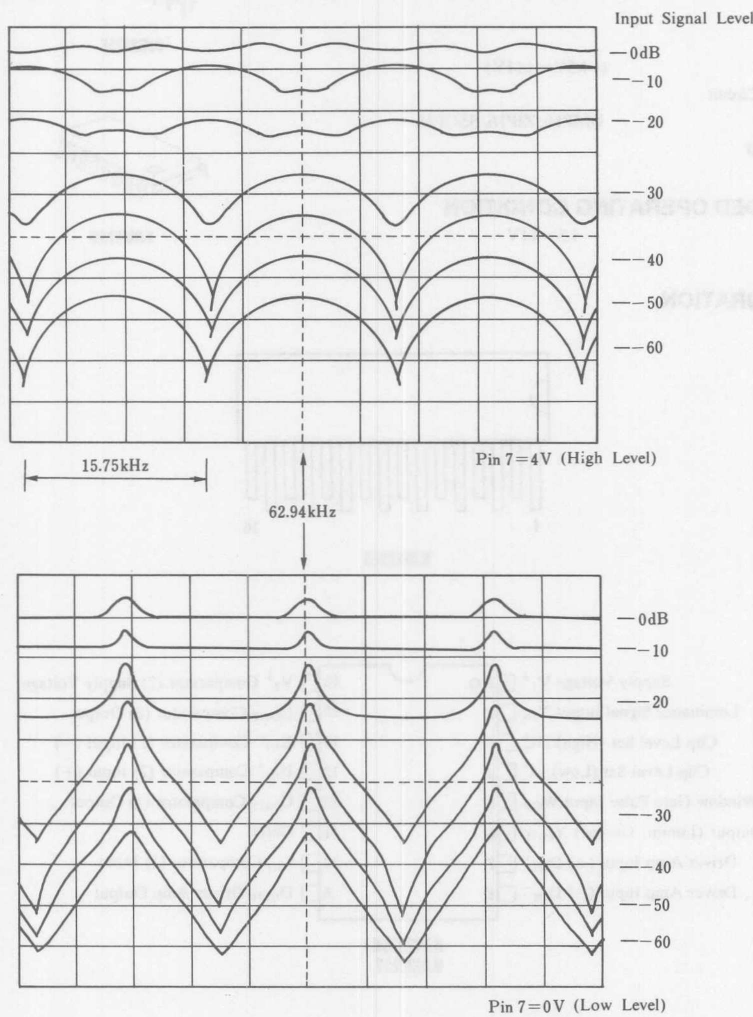


Fig. 6 Video Signal Waveform & Frequency Component

Fig.7 shows output characteristics determined by the input level to Pin7. The phase difference of each signal makes the output distortion of comb type filter characteristics, because FB system adds and substracts each signal. The NJM2224 phase difference is 2 degree at 4MHz. High dynamic range of video signal is realized by high supply voltage.

Fig. 7 Comb Type Filter Characteristics vs. Input Signal Level (800mV$_{P-P}$=0dB)

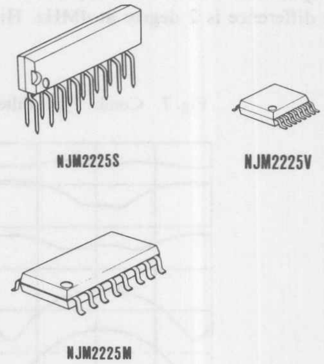


VIDEO CAMERA AUTO-IRIS FUNCTION

■ GENERAL DESCRIPTION

The NJM2225 are bipolar integrated circuits of motor drive for video camera. The NJM2225 have function of auto iris by video luminance signal and external information input to AGC circuit. They are composed of clipping circuit of video luminance signal, amplifier for driving motor and comparator for AGC circuits.

■ PACKAGE OUTLINE



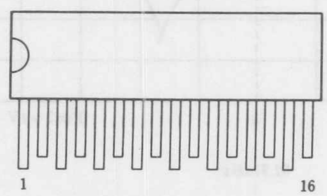
■ FEATURES

- Operating Voltage (+4.5V~+11V)
- Internal Auto Iris Circuit
- Package Outline DMP16, ZIP16, SSOP16
- Bipolar Technology

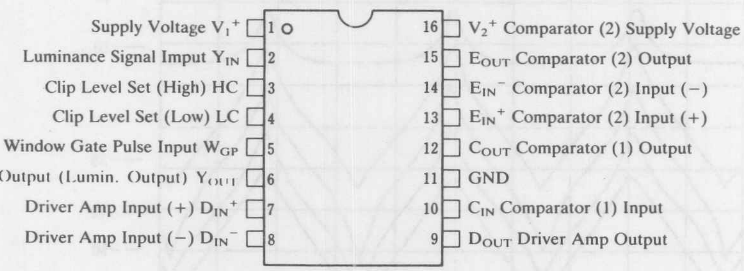
■ RECOMMENDED OPERATING CONDITION

- Operating Voltage 4.5~11V

■ PIN CONFIGURATION



NJM2225S



NJM2225M
NJM2225V

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

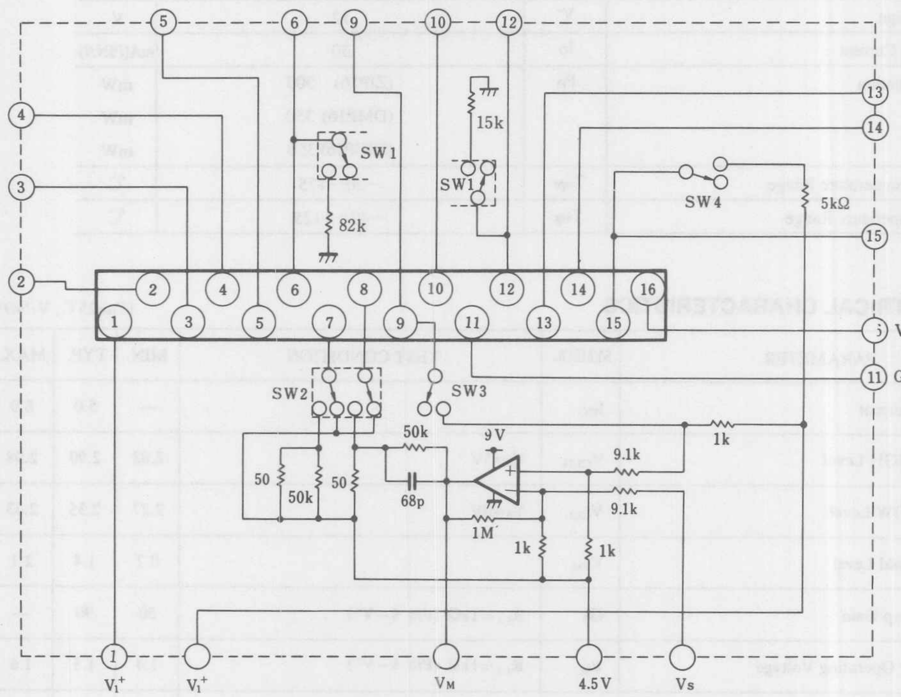
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	12	V
Motor Drive Current	I_O	30	mA(PIN.9)
Power Dissipation	P_D	(ZIP16) 500	mW
		(DMP16) 350	mW
		(SSOP16) 350	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V_1^+=9V, V_2^+=9V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}		—	5.0	8.0	mA
Pin 3 Clip HIGH Level	V_{CLH}	V_5=5V	2.82	2.90	2.98	V
Pin 3 Clip LOW Level	V_{CLL}	V_5=0V	2.27	2.35	2.43	V
Pin 5 Threshold Level	V_{TH}		0.7	1.4	2.1	V
7-9 Open Loop Gain	G_0	R_{L1}=1kΩ (Pin 9−V^+)	80	90	—	dB
Pin 9 Output Operating Voltage	V_{9L}	R_{L1}=1kΩ (Pin 9−V^+)	1.4	1.5	1.6	V
Pin 10 DC Level	V_{10}		1.9	2.1	2.3	V
AGC Clip Level	V_{12CL}	R_{L2}=15kΩ	3.80	4.00	4.20	V
Pin 15 Saturation Level	V_{15L}	E_{IN}^+=2V, E_{IN}^-=2.1V, R_{L3}=5kΩ	—	0.2	0.4	V
Pin 15 OFF Level	V_{15H}	E_{IN}^+=2V, E_{IN}^-=1.9V, R_{L3}=5kΩ	8.9	9.0	—	V

■ TEST CIRCUIT

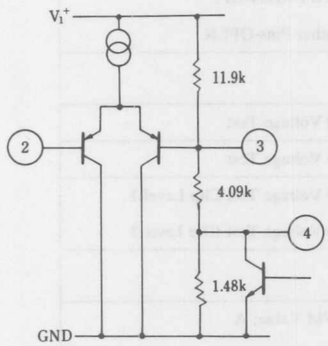
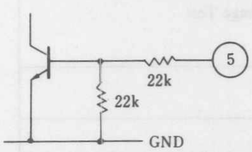
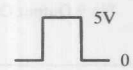
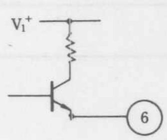
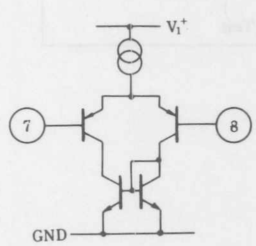
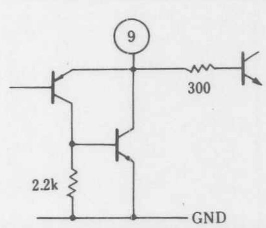


■ TEST CONDITION

PARAMETER	TEST CONDITION
Operating Current	$V_1^+=V_2^+=9V$ ⑤-GND, ⑬⑭-4.5V SW1~SW4-OFF Other Pins-OPEN
(Clip Circuit)	SW1~SW4-OFF
Pin 3 Clip HIGH Level	⑤-5V ③ Voltage Test
Pin 3 Clip LOW Level	⑤-0V ③ Voltage Test
Pin 5 Threshold Level	⑤-0.8V ③ Voltage Test Clip Level 1 ⑤-2.0V ③ Voltage Test Clip Level 2
(Driver-Amp Circuit)	SW2, SW3-ON
7-9 Open Loop Gain	Vs-6V, VM Value; A Vs-3V, VM Value; B O.L.Gain=20LOG [3000/(A-B)]
Pin 9 Output Operating Voltage	Vs-0.5V ⑨ Voltage Test SW3-ON
(Comparator Circuit)	
Pin 10 DC Level	⑩ Voltage Test
AGC Clip Level	SW1~SW3-ON Vs-8V ⑫ Voltage Test
(External Comparator Circuit)	
Pin 15 Saturation Level	SW4-ON ⑬-2V ⑭-2.1V ⑮ Voltage Test
Pin 15 OFF Level	⑬-2V ⑭-1.9V ⑮ Voltage Test

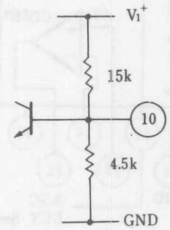
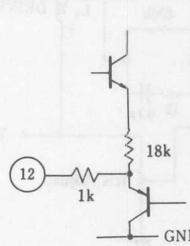
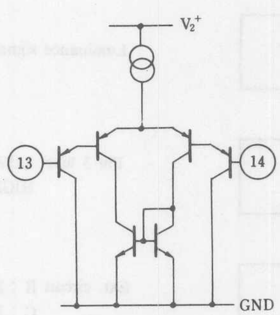
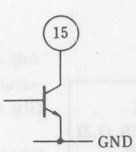
■ TERMINAL FUNCTION

(V_1^+=9V, V_2^+=9V)

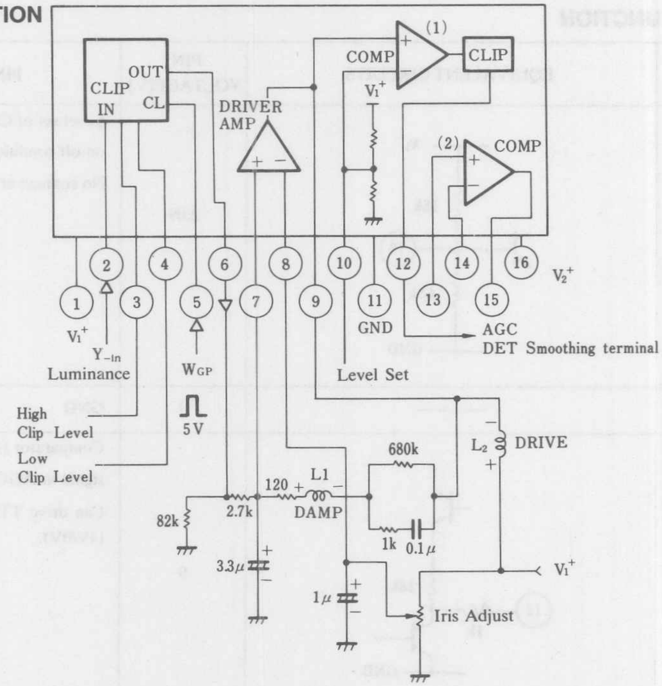
PIN NO.	PIN SYMBOL	EQUIVALENT CIRCUITS	PIN VOLTAGE[V]	PIN DESCRIPTION
1	V_1^+	—	9.0	Operating Voltage
2	Y_{IN}		2.38	Luminance signal input. Lum. sig. level: 0.5Vp-p.
3	HC		2.35	Setting clip level (High). No connect at V^+=9V.
4	LC		0.6	Setting clip level (Low). No connect at V^+=9V.
5	W_{GP}		0	Input window gate pulse. The pulse: 
6	Y_{OUT}		2.35	Clipped luminance signal Output.
7	D_{IN}^+		—	Input driver amp signal (+) of luminance converted to DC level.
8	D_{IN}^-		—	Input driver amp signal (−) of iris motor threshold voltage.
9	D_{OUT}		—	Driver amp output which drive driver coil of iris motor.

■ TERMINAL FUNCTION

(V_1^+=9V, V_2^+=9V)

PIN NO.	PIN SYMBOL	EQUIVALENT CIRCUITS	PIN VOLTAGE[V]	PIN DESCRIPTION
10	C_{IN}^-		2.09	Level set of COMP (1) which judges on-off condition of iris. No connect at V^+=9V.
11	GND	—	0	GND
12	C_{OUT}		0	Comparator (1) output which is signal to AGC circuit. Can drive TTL with 15kΩ load (4V/0V).
13	E_{IN}^+		—	Comparator (2) input (+)
14	E_{IN}^-		—	Comparator (2) input (−)
15	E_{OUT}		—	Comparator (2) output
16	V_2^+	—	9.0	Supply terminal to comparator (2)

■ TYPICAL APPLICATION



■ BRIEF OPERATION PRINCIPLE

Input luminance signal to clip circuit. (Pin 2)	Luminance signal clamped at 1.9V.
↓	
Clip with Pin 3 level, and output to. (Pin 6)	Pin 3 level LOW→2.35V HIGH→2.90V
↓	
Integration with external R,C. X → DC level conversion	Ext. circuit R : 2.7kΩ C : 3.3μF
↓	
Input to driver amp. (Pin 7)	
↓ ↓	Adjust Pin 8 level with external variable resistor. (Iris threshold)
Pin 8 level > X: DAMP (L1) OFF, DRIVER (L2) ON, Iris Open / Pin 8 level < X: DAMP (L1) ON, DRIVER (L2) OFF, Iris Close	DAMP (L1) DRIVER (L2) Iris Motor
↓ ↓	
To comparator (1) AGC output LOW → 0V / To comparator (1) AGC output HIGH → 4V (Pin 12)	AGC Output level: LOW 0V HIGH 4V (at 15kΩ load)

■ EXTERNAL CIRCUIT

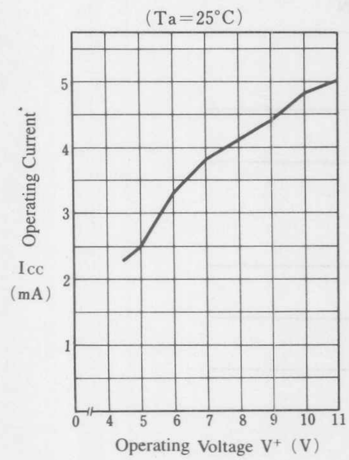
EXTERNAL DEVICE	OPERATION DESCRIPTION
Pin6–Pin7 resistor 2.7kΩ Pin7-GND capacitor 3.3μF	Integrating video luminance signal, and convert to DC level.
Pin7-L1 resistor 120Ω	Control iris motor speed.
Pin8 –Pin9 RC 680kΩ, 1kΩ, 0.1μF	To prevent miss operation of motor by vertical synchronous signal, low-pass filter acts as negative feedback circuit.
Pin8-GND capacitor 1μF	AC ground
V_1^+-GND Variable resistor	Set threshold value of iris-motor start.

■ NOTE

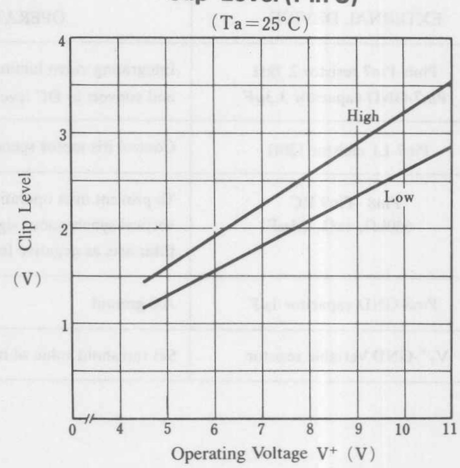
- When used at $V_1^+=9V$, not connect pin3, pin4, pin10.

■ TYPICAL CHARACTERISTICS

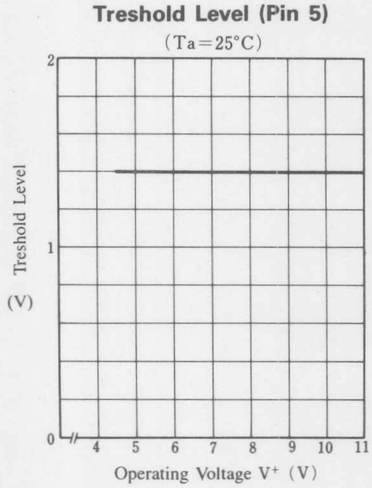
Operating Current



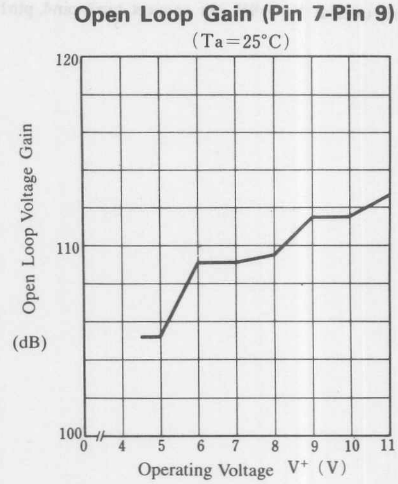
Clip Level (Pin 3)



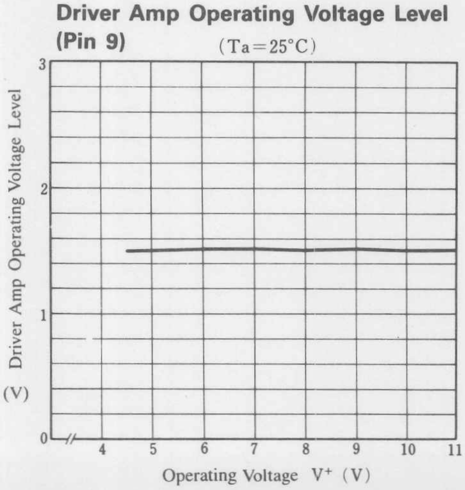
Treshold Level (Pin 5)



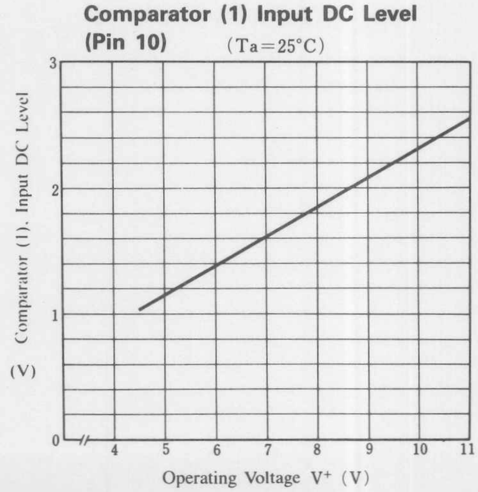
Open Loop Gain (Pin 7-Pin 9)



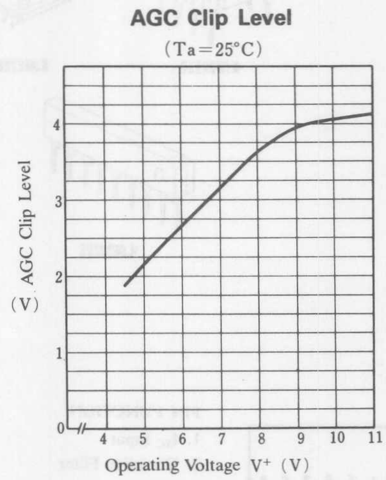
Driver Amp Operating Voltage Level (Pin 9)

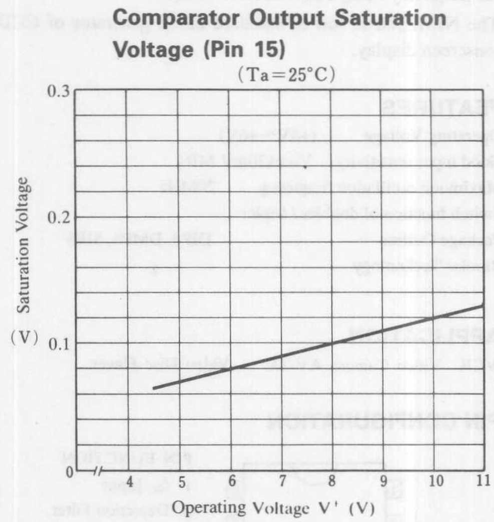


Comparator (1) Input DC Level (Pin 10)



■ TYPICAL CHARACTERISTICS





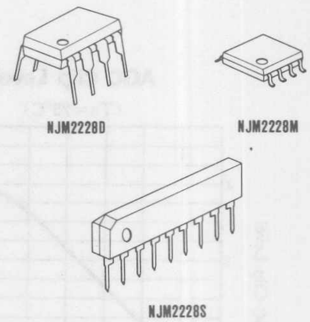
VIDEO SUB-CARRIER SIGNAL DOUBLER/TRIPLER

■ GENERAL DESCRIPTION

The NJM2228 is a doubler/tripler oscillator based on video sub-carrier frequency using PLL circuit technique.

The NJM2228 is suit to standard clock generator of CCD clock and onscreen display.

■ PACKAGE OUTLINE



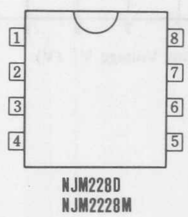
■ FEATURES

- Operating Voltage (+4V~+6V)
- Good input sensitivity V_{IN}=120mV MIN.
- Maximuon oscillation frequency 20MHz.
- Switch function of doubler / tripler
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

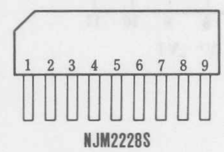
■ APPLICATION

- VCR Video Camera AV-TV Video Disc Player

■ PIN CONFIGURATION

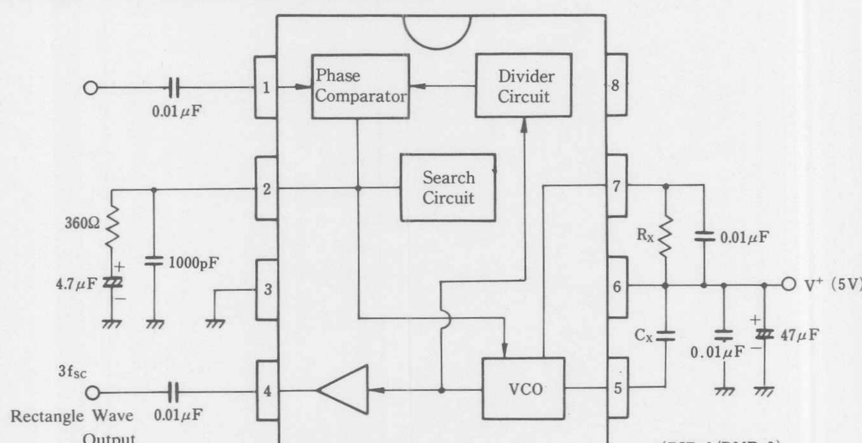


PIN FUNCTION
1. f_{SC} Input
2. Detection Filter
3. GND
4. Oscillator Output
5. Oscillator C
6. V^+
7. Oscillator R
8. 2/3 Switch



PIN FUNCTION
1. f_{SC} Input
2. Detection Filter
3. GND 1
4. Oscillator Output
5. GND 2
6. Oscillator C
7. V^+
8. Oscillator R
9. 2/3 Switch

■ BLOCK DIAGRAM & EXTERNAL COMPONENTS



(DIP-8/DMP-8)

There is stray capacity assembled on PC board, and so select Rx, Cx to the value which pin 2 voltage (search voltage at VCO locked) becomes about 2V. Cx>5pF, 5.6k>Rx>3.3kΩ.

	NTSC		PAL	
	3 multiplier	2 multiplier	3 multiplier	2 multiplier
Cx	10 p	22p	8 p	15p
Rx	4.7 k	4.6k	3.9k	4.6k

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

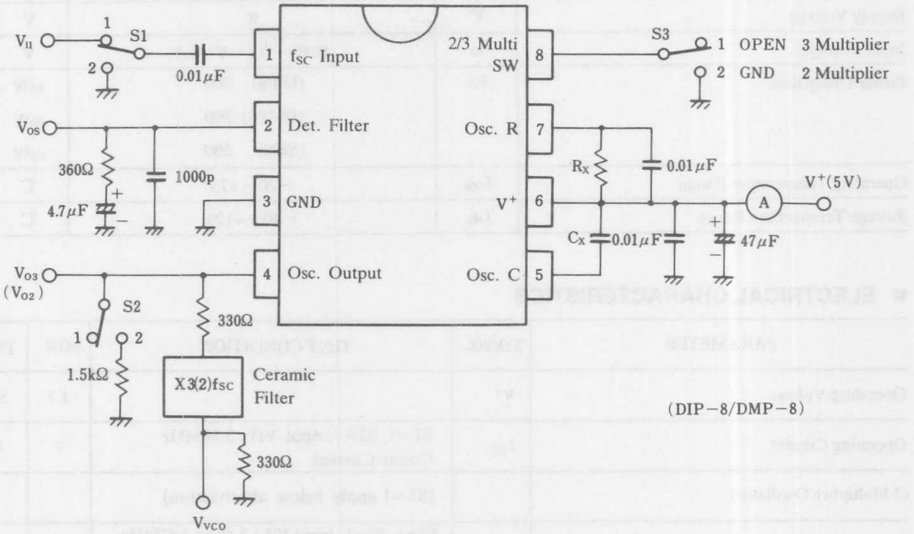
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Input Voltage	I_O	GND−0.3～V^++0.3	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(SIP8) 500	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

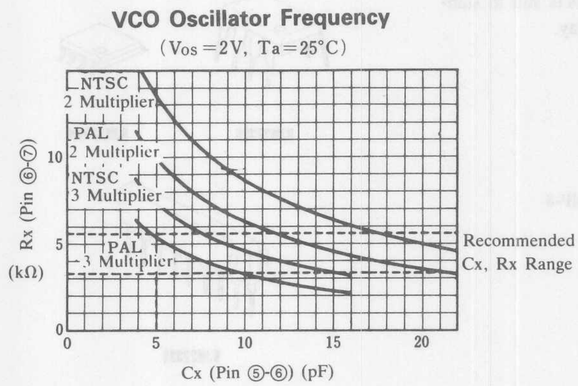
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		4.7	5.0	5.3	V
Operating Current	I_{CC}	S1=1, S2=1,input Vi1 : 3.58MHz Count Current	7	10	13	mA
(3 Multiplier Oscillator)		(S3=1 apply below abbriviation)				
Input Voltage Swing Range	V_{fsc3}	S1=1, S2=1, input Vi1 : 3.58 or 4.43MHz (sine wave), guaranteed Vi1 voltage range.	0.12	1.0	2.0	Vp-p
Input Sensitivity	V_{Is3}	S1=1, S2=1, input Vi1 : 3.58 or 4.43MHz (sine wave), actually tested minimum Vi1 voltage.	—	0.05	—	Vp-p
VCO Oscillation Swing	V_{O3}	S1=1, S2=2, input Vi1 : 3.58MHz, 1.0Vp-p. V_{O3} Oscillation Swing	0.7	0.9	1.1	Vp-p
fsc Leakage	L_{fsc3}	S1=1, S2=2, input Vi1 : 3.58MHz, V_{O3} (fsc level/3fsc level)	—	−50	—	dB
3fsc Output Duty	D_{3fsc}	S1=1, S2=2, input Vi1 : 3.58MHz, 1.0Vp-p, Vos output signal duty.	45	50	55	%
(2 Multiplier Oscillator)		(S3=2 apply below)				
Input Voltage Swing Range	V_{fsc2}	S1=1, S2=1, input Vi1 : 3.58 or 4.43MHz (sine wave), guaranteed Vi1 voltage range.	0.12	1.0	2.0	Vp-p
Input Sensitivity	V_{Is2}	S1=1, S2=1, input Vi1 : 3.58 or 4.43MHz (sine wave), actually tested minimum Vi1 voltage.	—	0.05	—	Vp-p
VCO Oscillation Swing	V_{O2}	S1=1, S2=2, input Vi1 : 3.58MHz, 1.0Vp-p. V_{O2} Oscillation Swing	0.7	0.9	1.1	Vp-p
fsc Leakage	L_{fsc2}	S1=1, S2=2, input Vi1 : 3.58MHz, 1.0Vp-p. V_{O2} (fsc level/2fsc level)	—	−50	—	dB
2fsc Output Duty	D_{2fsc}	S1=1, S2=2, input Vi1 : 3.58MHz, 1.0Vp-p. V_{OS} Output signal duty.	45	50	55	%

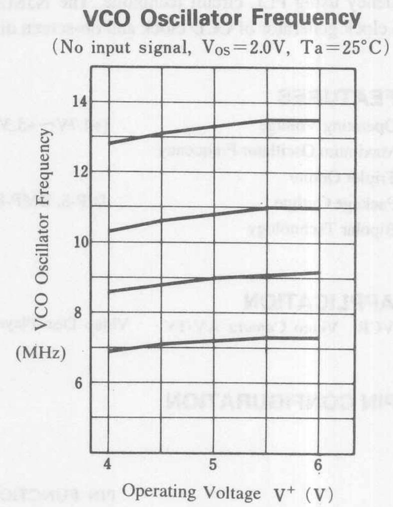
■ TEST CIRCUIT

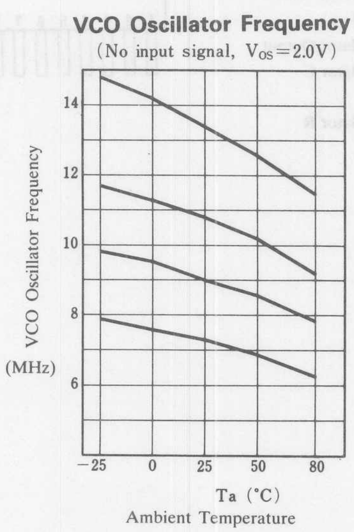


(note 1): Rx, Cx accuracy: less than ±1%.
(note 2): Cx is not considered pin 5 stray capacitance. VCO free-run frequency is affected by stray capacitance of P.C board, socket and others.
(note 3): The NJM2228 is produced by high frequency wafer process and some of pin may be weak against surge voltage.
(note 4): Pin 2 filter must be connected to ground.

■ TYPICAL CHARACTERISTICS





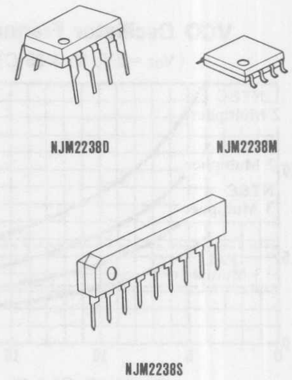


VIDEO SUB-CARRIER SIGNAL TRIPLER

■ GENERAL DESCRIPTION

The NJM2238 is a tripler oscillator based on video subcarrier frequency using PLL circuit technique. The NJM2238 is suit to standard clock generator of CCD clock and on-screen display.

■ PACKAGE OUTLINE



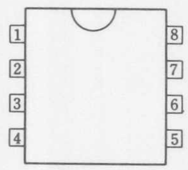
■ FEATURES

- Operating Voltage (+4.7V~+5.3V)
- Maximum Oscillator Frequency
- Tripler Output
- Package Outline DIP-8, DMP-8, SIP-8
- Bipolar Technology

■ APPLICATION

- VCR Video Camera AV-TV Video Disc Player

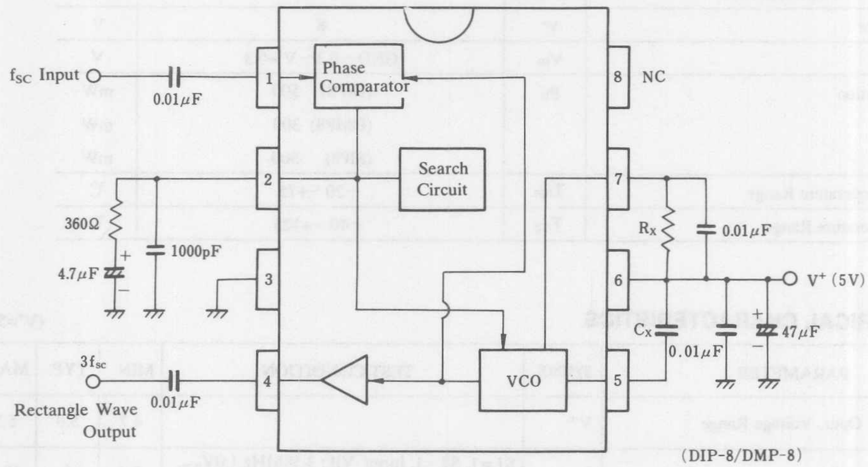
■ PIN CONFIGURATION



PIN FUNCTION
1. f_{SC} Input
2. Detection Filter
3. GND
4. Oscillator Output
5. Oscillator C
6. V^+
7. Oscillator R
8. NC

PIN FUNCTION
1. f_{SC} Input
2. Detection Filter
3. GND 1
4. Oscillator Output
5. GND 2
6. Oscillator C
7. V^+
8. Oscillator R
9. NC

■ BLOCK DIAGRAM & EXTERNAL COMPONENTS



(DIP-8/DMP-8)

There is stray capacity assembled on PC board, and so select Rx, Cx to the value which pin 2 voltage (search voltage at VCO locked) becomes about 2V. Cx>5pF, 5.6kΩ>Rx>3.3kΩ

	NTSC	PAL
Cx	10p	8p
Rx	5.2k	4.4k

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

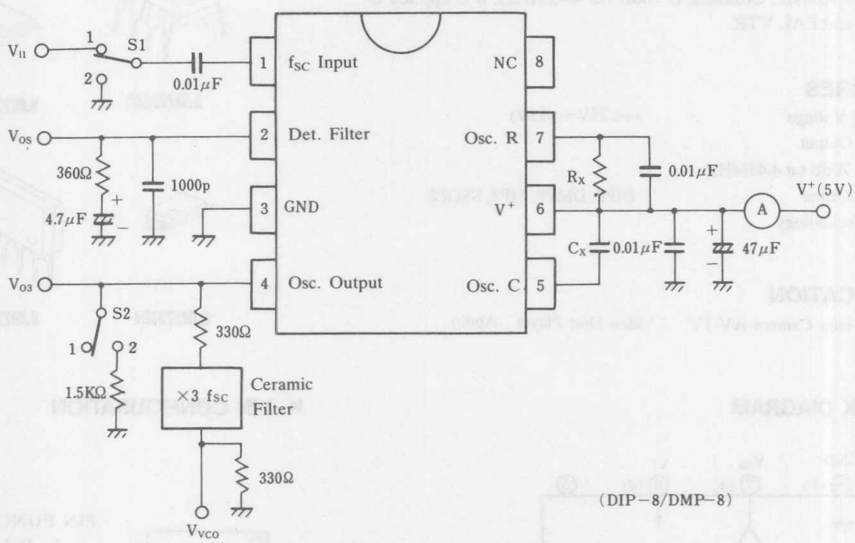
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Input Voltage	V_{IN}	GND−0.3~V^++0.3	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(SIP8) 500	mW
Operating Temperature Range	T_{opr}	−20~+75	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Recommended Oper. Voltage Range	V^+		4.7	5.0	5.3	V
Operating Current	I_{CC}	S1=1, S2=1, input Vi1 : 3.58MHz 1.0V_{P-P}. Count Current	5.6	8	10.4	mA
Input Voltage Swing Range	V_{fsc}	S1=1, S2=1, input Vi1 : 3.58 or 4.43MHz (sine wave), guaranteed Vi1 voltage range.	0.5	1.0	2.0	Vp-p
Input Sensitivity	V_{is}	S1=1, S2=1, input Vi1 : 3.58 or 4.43MHz (sine wave), actually tested minimum Vi1 voltage.	—	0.2	—	Vp-p
VCO Oscillation Swing	V_{O3}	S1=1, S2=2, input Vi1 : 3.58MHz, 1.0Vp-p.	0.7	0.9	1.1	Vp-p
fsc Leakage	L_{fsc}	S1=1, S2=2, input Vi1: 3.58MHz, 1.0Vp-p. V_{O3} (fsc level/3fsc level)	—	−50	—	dB
3fsc Output Duty	D_{3fsc}	S1=1, S2=2, input Vi1 : 3.58MHz, 1.0Vp-p, V_{O3} output signal duty.	45	50	55	%

■ TEST CIRCUIT



(note 1): Rx, Cx accuracy: less than ±1%

(note 2): Cx is not considered pin 5 stray capacitance. VCO free-run frequency is affected by stray capacitance of PC board, socket and others.

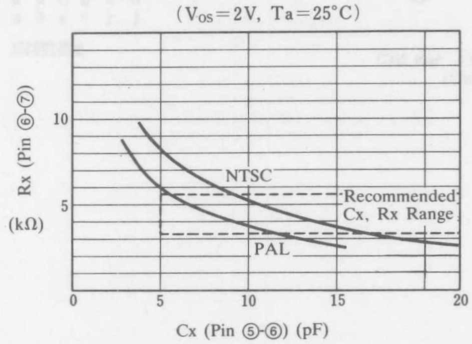
(note 3): The NJM2238 is produced by high frequency wafer process and some of pin may be weak against surge voltage.

(note 4): Pin 2 filter must be connected to ground.

■ TYPICAL CHARACTERISTICS

VCO Oscillator Frequency

(V_{OS}=2V, Ta=25°C)

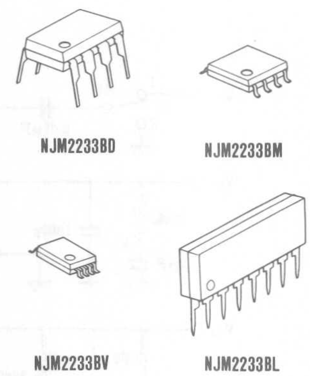


2-INPUT SINGLE VIDEO SWITCH

■ GENERAL DESCRIPTION

The NJM2233B is 2-input signal video switch selecting one of two video or audio signals. Its operating voltage is 4.75 to 13V and bandwidth is 10MHz. Crosstalk is 70dB (at 4.43MHz). It is applied to both NTSC and PAL VTR.

■ PACKAGE OUTLINE



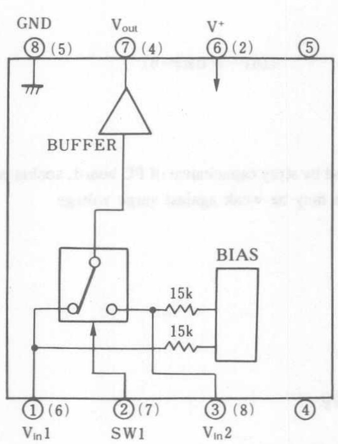
■ FEATURES

- Operating Voltage (+4.75V～+13V)
- 2 Input-1 Output
- Crosstalk 70dB (at 4.43MHz)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

■ APPLICATION

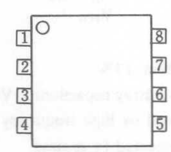
- VCR Video Camera AV-TV Video Disc Player Audio

■ BLOCK DIAGRAM



○ DIP－8, DMP－8 (4, 5pin NC)
( ) SIP－8 (1, 3pin NC)

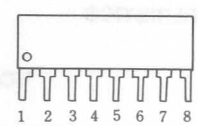
■ PIN CONFIGURATION



NJM2233BD
NJM2233BM
NJM2233BV

PIN FUNCTION

1. $V_{in}1$
2. SW1
3. $V_{in}2$
4. N.C.
5. N.C.
6. V^+
7. V_{out}
8. GND



NJM2233BL

PIN FUNCTION

1. N.C.
2. V^+
3. N.C.
4. V_{out}
5. GND
6. $V_{in}1$
7. SW1
8. $V_{in}2$

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^{+}	15	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(SIP8) 800	mW
		(SSOP8) 250	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

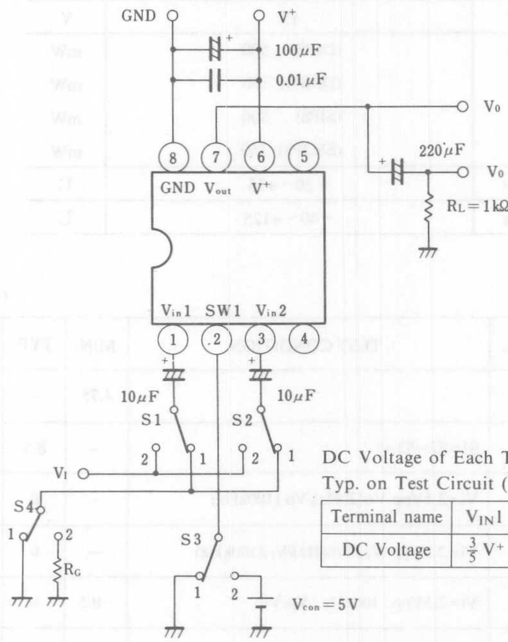
(V^{+}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^{+}		4.75	—	13.0	V
Operating Current	I_{CC}	S1=S2=S3=1	—	8.5	11.0	mA
Frequency Characteristic (1)	G_{f1}	Vi=2.5Vpp Vo(20Hz)/Vo (100kHz)	—	0	±1.0	dB
Frequency Characteristic (2)	G_{f2}	Vi=2.0Vpp V_O(10MHz)/V_O(100kHz)	—	0	±1.0	dB
Voltage Gain	G_V	Vi=2.5Vpp, 100kHz, Vo/Vi	-0.5	0	—	dB
Total Harmonic Distortion	THD	Vi=2.5Vpp, 1kHz	—	0.01	—	%
Differential Gain	DG	Vi=2Vpp standard staircase signal	—	0	—	%
Differential Phase	DP	Vi=2Vpp standard staircase signal	—	0	—	deg
Output Offset Voltage	V_{off}	S1=S2=1, S3=1→2, Vo voltage change	—	0	±15	mV
Crosstalk	CT	(S1=S3=1, S2=2) and (S1=S3=2, S2=1) Vi=2.0Vpp, 4.43MHz, Vo/Vi	—	−70	—	dB
Switch Change Voltage	V_{CH}	Garanteed voltage of all switch on	2.4	—	—	V
	V_{CL}	Garanteed voltage of all switch off	—	—	0.8	V
Input Impedance	R_I		—	15	—	kΩ
Output impedance	R_O		—	10	—	Ω

■ CONTROL SIGNAL - OUTPUT SIGNAL

SW 1	OUTPUT SIGNAL
L	$V_{IN}1$
H	$V_{IN}2$

■ TEST CIRCUIT

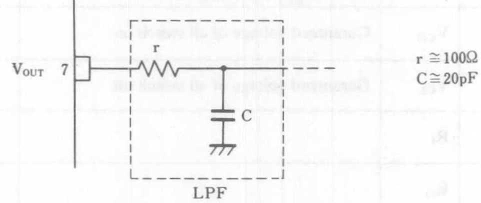


DC Voltage of Each Terminal
Typ. on Test Circuit (Ta=25℃).

Terminal name	$V_{IN}1$	SW1	$V_{IN}2$	V^+	V_{OUT}	GND
DC Voltage	$\frac{3}{5}V^+$	—	$\frac{3}{5}V^+$	—	$\frac{3}{5}V^+-0.7$	—

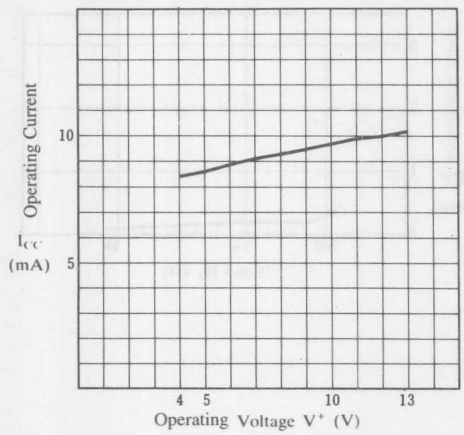
■ APPLICATION

Oscillation Pervention on light loading conditions
Recommended under circuit

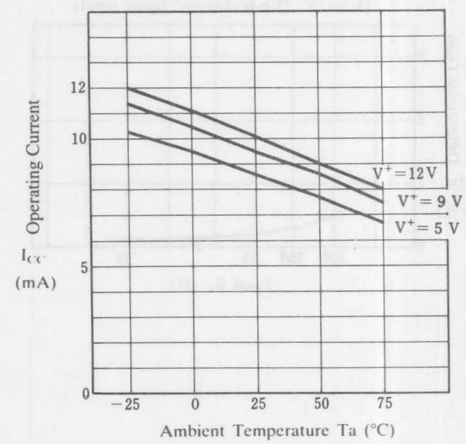


■ TYPICAL CHARACTERISTICS

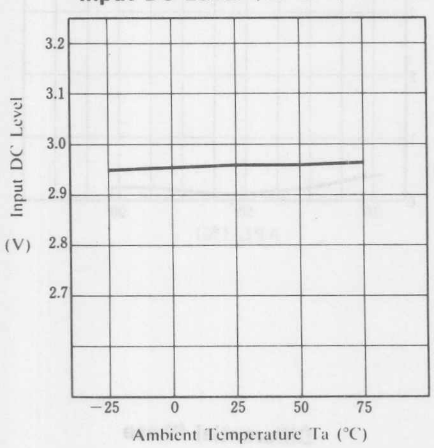
Operating Current (Ta=25°C)



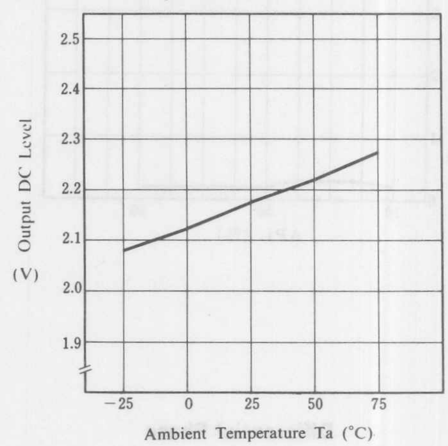
Operating Current (Ta=25°C)



Input DC Level (Ta=25°C, V^+=5V)

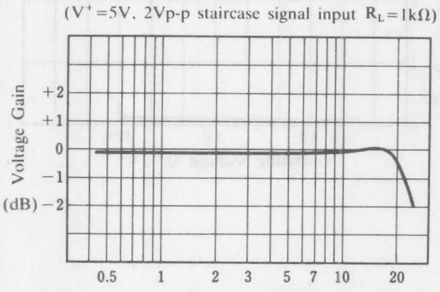


Output DC Level (V^+=5V)



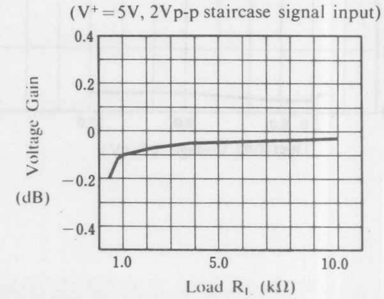
Voltage Gain

(V^+=5V, 2Vp-p staircase signal input R_L=1kΩ)



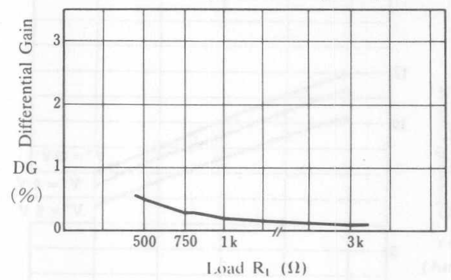
Voltage Gain

(V^+=5V, 2Vp-p staircase signal input)

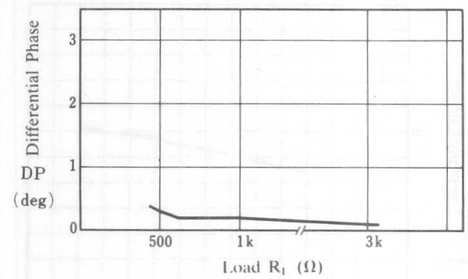


■ TYPICAL CHARACTERISTICS

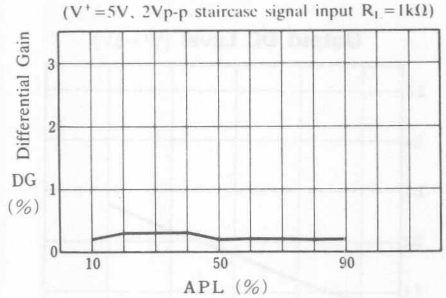
Differential Gain
(V⁺=5V, 2Vp-p staircase signal input)



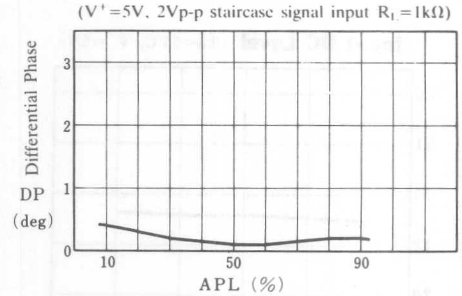
Differential Gain
(V⁺=5V, 2Vp-p staircase ignal input)



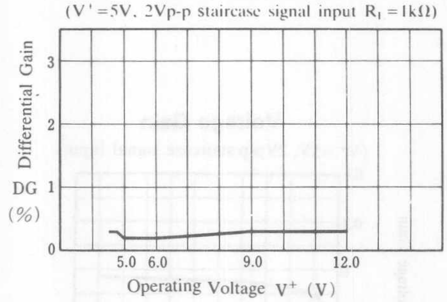
Differential Gain
(V⁺=5V, 2Vp-p staircase signal input R_L=1kΩ)



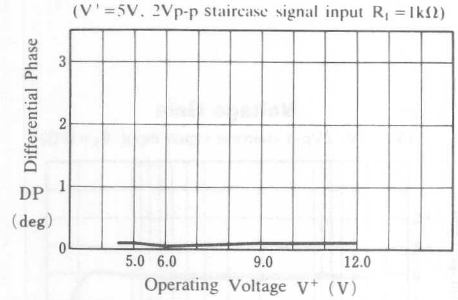
Differential Phase
(V⁺=5V, 2Vp-p staircase signal input R_L=1kΩ)



Differential Phase
(V⁺=5V, 2Vp-p staircase signal input R_L=1kΩ)



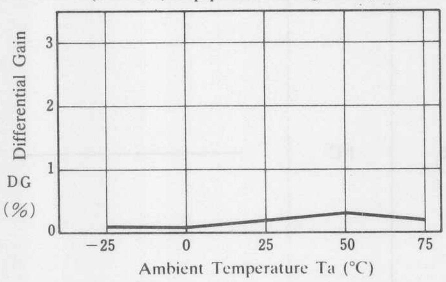
Differential Phase
(V⁺=5V, 2Vp-p staircase signal input R_L=1kΩ)



■ TYPICAL CHARACTERISTICS

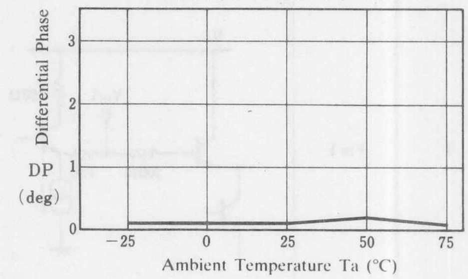
Differential Gain

($V^+=5V$, 2Vp-p staircase signal input)



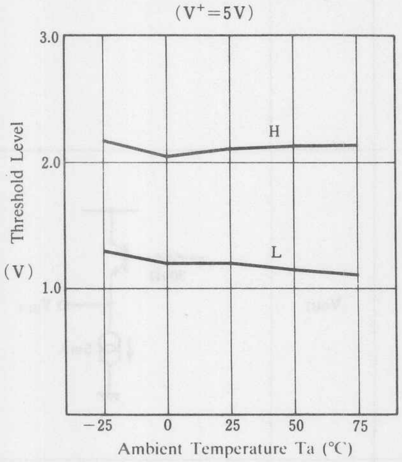
Differential Phase

($V^+=5V$, 2Vp-p staircase signal input)



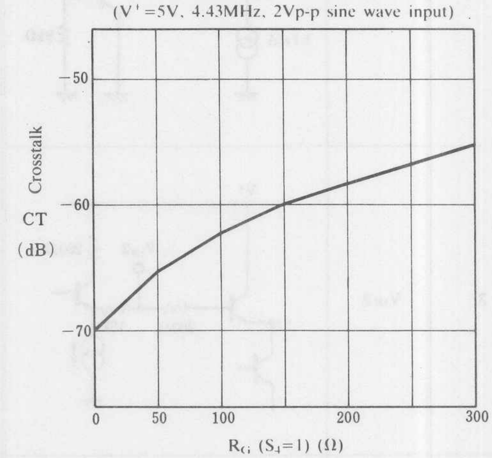
Differential Level

($V^+=5V$)



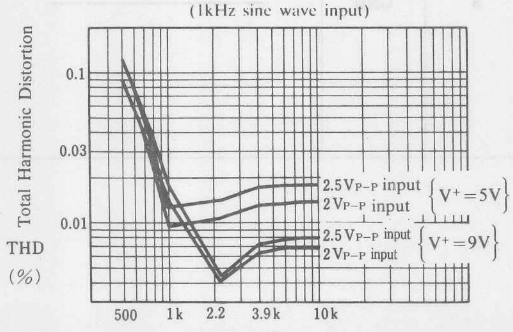
Crosstalk vs. R_G

($V^+=5V$, 4.43MHz, 2Vp-p sine wave input)

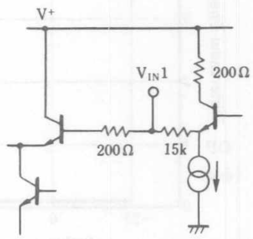
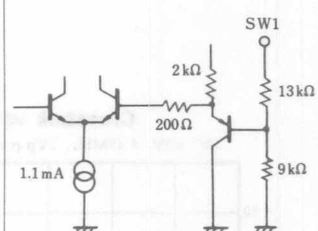
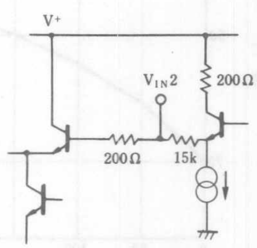
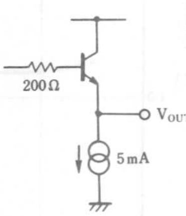


Total Harmonic Distortion

(1kHz sine wave input)



■ EQUIVALENT CIRCUIT

PIN NO.	SYMBOL	INSIDE EQUIVALENT CIRCUIT	PIN NO.	SYMBOL	INSIDE EQUIVALENT CIRCUIT
1	V_{IN} 1		5	NC	
2	SW 1		6	V^+	
3	V_{IN} 2		7	V_{OUT}	
4	NC		8	GND	

3-INPUT VIDEO SWITCH

■ GENERAL DESCRIPTION

The NJM2234 is 3-input video switch selecting one of three iuput video or audio signals. Its operating supply voltage range is 5 to 12V and bandwidth is 10MHz. Crosstalk is 70dB (at 4.43MHz).

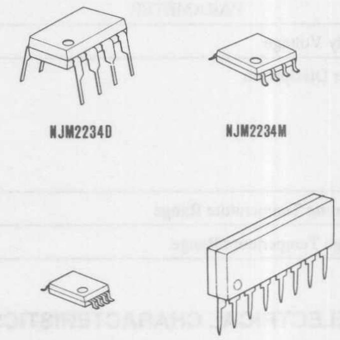
■ FEATURES

- Operating Voltage (+4.75V~+13V)
- 3 Input-1 Output
- Muting Function available
- Wide Operating Supply Voltage Range 4.75~13V
- Cross-talk 70dB (at 4.43MHz)
- Muting Function available
- Package Outline DIP-8, DMP-8, SIP-8, SSOP-8
- Bipolar Technology

■ APPLICATION

- VCR Video Camera AV-TV Video Disc Player Audio

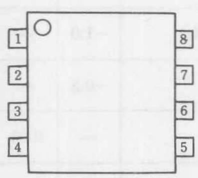
■ PACKAGE OUTLINE



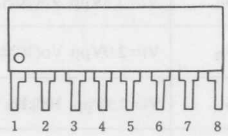
NJM2234D NJM2234M

NJM2234V NJM2234L

■ PIN CONFIGURATION



NJM2234D
NJM2234M
NJM2234V

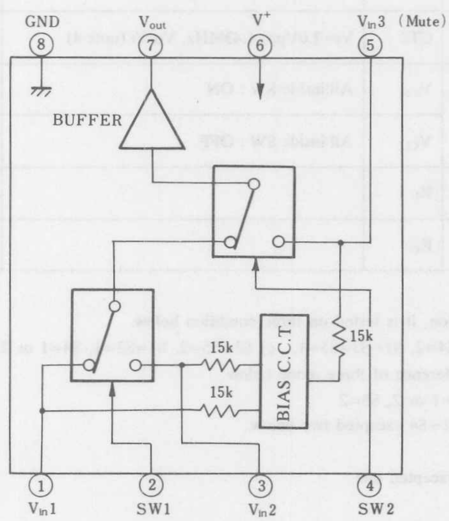


NJM2234L

PIN FUNCTION

1. $V_{in}1$
2. SW1
3. $V_{in}2$
4. SW2
5. $V_{in}3$
6. V^+
7. V_{out}
8. GND

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(SSOP8) 250	mW
		(SIP8) 800	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage	V^+		4.75	—	13.0	V
Operating Current	I_{CC}	S1=S2=S3=S4=S5=1	—	11.0	14.5	mA
Frequency Characteristics (1)	G_{f1}	Vi=2.5Vpp Vo(20Hz)/Vo(100kHz)	−1.0	—	+1.0	dB
Frequency Characteristics (2)	G_{f2}	Vi=2.0Vpp Vo(10MHz)/Vo(100kHz)	−1.0	—	+1.0	dB
Voltage Gain	G_V	Vi=2.5Vpp, 100kHz Vo/Vi	−0.5	—	+0.5	dB
Total Harmonic Distortion	THD	Vi=2.5Vpp, 1kHz	—	0.03	—	%
Differential Gain	DG	Vi=2Vpp Staircase signal	—	0	—	%
Differential Phase	DP	Vi=2Vpp Staircase signal	—	0	—	deg
Output Offset Voltage	V_{off}	(note 2)	−30	—	+30	mV
Crosstalk (1)	CT1	Vi=2.0Vpp. 4.43MHz, Vo/Vi(note 3)	—	−70	—	dB
Crosstalk (2)	CT2	Vi=2.0Vpp, 4.43MHz, Vo/Vi (note 4)	—	−70	—	dB
Switch Change Voltage	V_{CH}	All inside SW : ON	2.4	—	—	V
	V_{CL}	All inside SW : OFF	—	—	0.8	V
Input Impedance	R_I		—	15	—	kΩ
Output Impedance	R_O		—	10	—	Ω

(note 1): If it is not shown about switch condition, it is tested on three condition below.
a) S1=2, S2=S3=S4=S5=1 b) S2=S4=2, S1=S3=S5=1, c) S3=S5=2, S1=S2=1, S4=1 or 2.

(note 2): S1=S2=S3=1. Output DC voltage difference of three mode below.
a) S4=S5=1 b) S4=2, S5=1 c) S4=1 or 2, S5=2

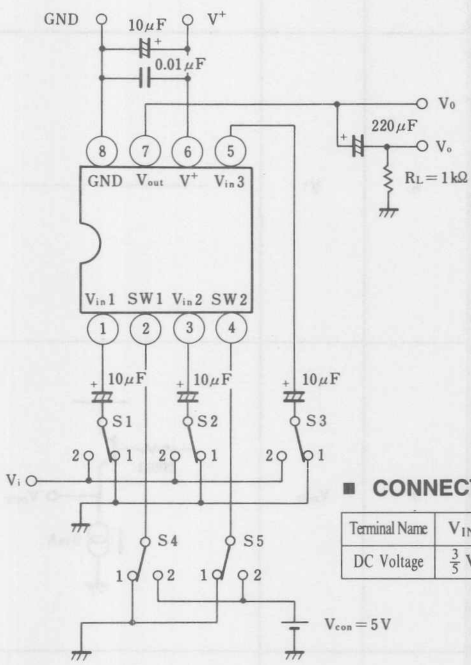
(note 3): S5=1, Tested on all combination of S1~S4 excepted two below.
a) S1=2, S4=1 b) S2=S4=2

(note 4): Tested on all combination of S1~S4 excepted one.
a) S5=2, S3=2

■ INPUT CONTROL SIGNAL - OUTPUT SIGNAL

SW 1	SW 2	OUTPUT SIGNAL
L	L	$V_{IN}1$
H	L	$V_{IN}2$
L/H	H	$V_{IN}3$

■ TEST CIRCUIT



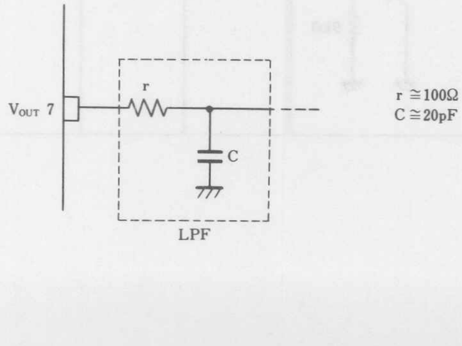
■ CONNECTION DIAGRAM

Terminal Name	$V_{IN}1$	SW1	$V_{IN}2$	SW2	$V_{IN}3$	V^+	V_{OUT}	GND
DC Voltage	$\frac{3}{5}V^+$	—	$\frac{3}{5}V^+$	—	$\frac{3}{5}V^+$	—	$\frac{3}{5}V^+-0.7$	—

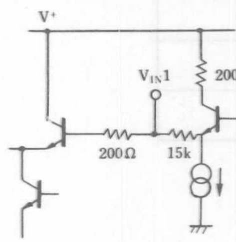
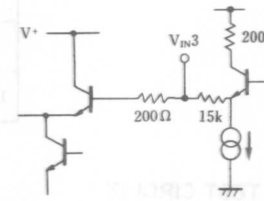
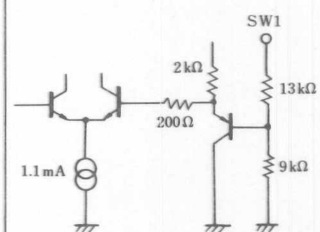
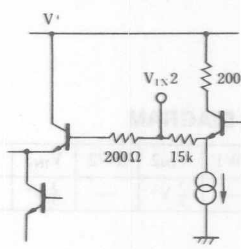
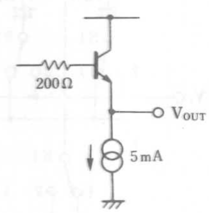
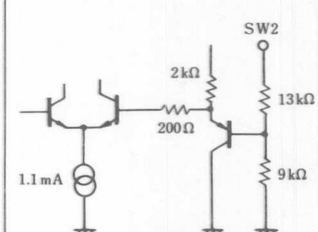
■ APPLICATION

Oscillation Prevention on light loading conditions

Recommended under circuit



■ EQUIVALENT CIRCUIT

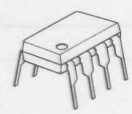
PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT	PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	V_{IN} 1		5	V_{IN} 3 (Mute)	
2	SW 1		6	V^+	——
3	V_{IN} 2		7	V_{OUT}	
4	SW 2		8	GND	——

3-INPUT VIDEO SWITCH

■ GENERAL DESCRIPTION

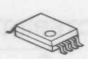
The NJM2235 is 3-input video switch for video and audio signal. It has clamp function and so is applied to fixed DC level of video signal. Its operating supply voltage range is 5 to 12V and bandwidth is 10MHz. Crosstalk is 70dB (at 4.43MHz).

■ PACKAGE OUTLINE

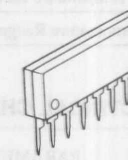


NJM2235D

NJM2235M



NJM2235V



NJM2235L

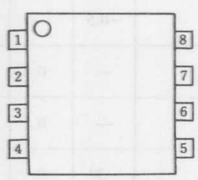
■ FEATURES

- Operating Voltage (+4.75V～+13V)
- 3 Input-1 Output
- Internal Clamp Function
- Wide Operating Supply Voltage Range 4.75～13V
- Cross-talk 70dB (at 4.43MHz)
- Wide Frequency Range 10MHz
- Muting Function available
- Package Outline DIP-8, DMP-8, SIP-8, SSOP-8
- Bipolar Technology

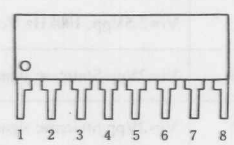
■ APPLICATION

- VCR Video Camera AV-TV Video Disc Player

■ PIN CONFIGURATION



NJM2235D
NJM2235M
NJM2235V

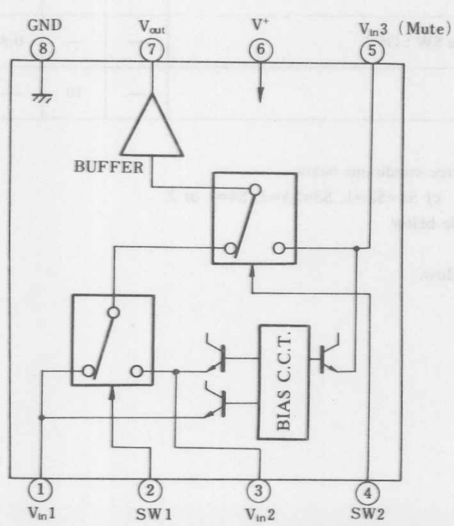


NJM2235L

PIN FUNCTION

1. $V_{in}1$
2. SW1
3. $V_{in}2$
4. SW2
5. $V_{in}3$
6. V^+
7. V_{out}
8. GND

■ BLOCK DIAGRAM



■ INPUT CONTROL SIGNAL - OUTPUT SIGNAL

SW 1	SW 2	OUTPUT SIGNAL
L	L	$V_{IN}1$
H	L	$V_{IN}2$
L/H	H	$V_{IN}3$

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(SSOP8) 250	mW
		(SIP8) 800	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage	V^+		4.75	—	13.0	V
Operating Current	I_{CC}	S1=S2=S3=S4=S5=1	—	10.5	14.0	mA
Frequency Characteristics	G_{f2}	Vi=2.0Vpp Vo(10Hz)/Vo(100kHz)	−1.0	—	+1.0	dB
Voltage Gain	G_V	Vi=2.5Vpp, 100kHz Vo/Vi	−0.5	—	+0.5	dB
Differential Gain	DG	Vi=2Vpp Staircase signal	—	0	—	%
Differential Phase	DP	Vi=2Vpp Staircase signal	—	0	—	deg
Output Offset Voltage	V_{off}	(note 2)	−30	0	+30	mV
Input Clamp Voltage	V_{IC}	(note 5)	—	2.0	—	V
Crosstalk (1)	CT1	Vi=2.0Vpp, 4.43MHz, Vo/Vi (note 3)	—	−70	—	dB
Crosstalk (2)	CT2	Vi=2.0Vpp, 4.43MHz, Vo/Vi (note 4)	—	−70	—	dB
Switch Change Voltage	V_{CH}	All inside SW : ON	2.4	—	—	V
	V_{CL}	All inside SW : OFF	—	—	0.8	V
Output Impedance	R_O		—	10	—	Ω

(note 1): If it is not shown about switch condition, it is tested on three conditions below.
a) S1=2, S2=S3=S4=S5=1 b) S2=S4=2, S1=S3=S5=1, c) S1=S2=1, S3=S5=2, S4=1 or 2.

(note 2): S1=S2=S3=1, Output DC voltage difference of three mode below.
a) S4=S5=1 b) S4=2, S5=1 c) S4=1 or 2, S5=2

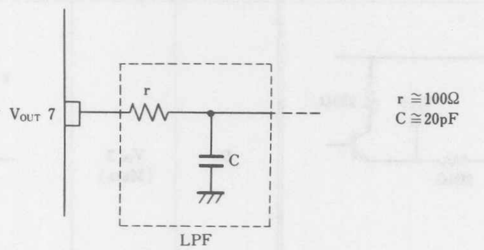
(note 3): S5=1, Tested on all combination of S1~S4 except two below.
a) S1=2, S4=1 b) S2=S4=2

(note 4): Tested on all combination of S1~S4 except one.
a) S5=2, S3=2

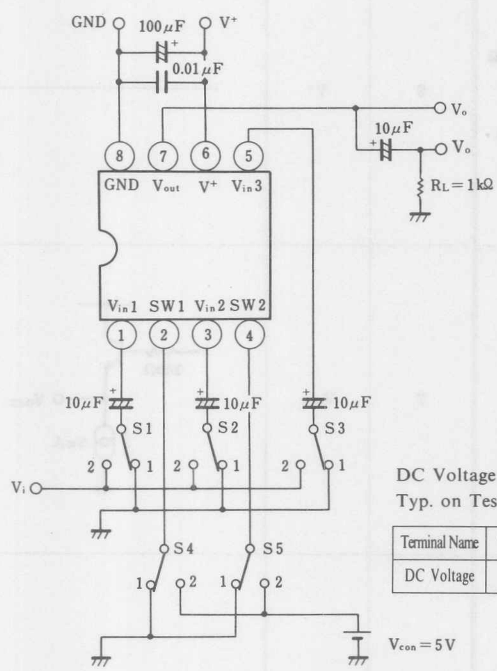
(note 5): Input clamp voltage is about 2/5 of supply voltage.

■ APPLICATION

Oscillation Prevention on light loading conditions
Recommended under circuit



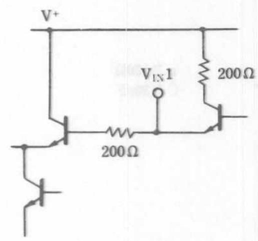
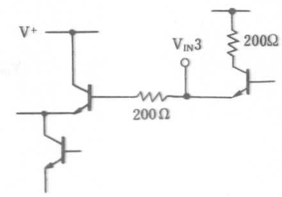
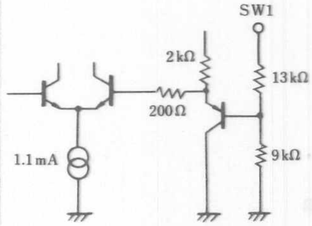
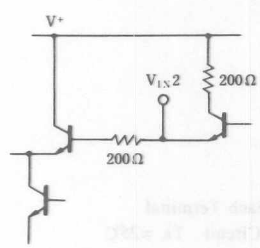
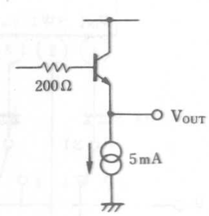
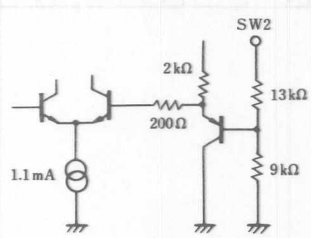
■ TEST CIRCUIT



DC Voltage Each Terminal
Typ. on Test Circuit Ta = 25℃

Terminal Name	$V_{IN}1$	SW1	$V_{IN}2$	SW2	$V_{IN}3$	V^+	V_{OUT}	GND
DC Voltage	$\frac{2}{5}V^+$	—	$\frac{2}{5}V^+$	—	$\frac{2}{5}V^+$	—	$\frac{2}{5}V^+-0.7$	—

■ EQUIVALENT CIRCUIT

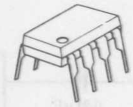
PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT	PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	V_{IN} 1		5	V_{IN} 3 (Mute)	
2	SW 1		6	V^+	
3	V_{IN} 2		7	V_{OUT}	
4	SW 2		8	GND	

VIDEO SUB-CARRIER SIGNAL QUADRUPLER

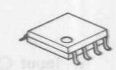
■ GENERAL DESCRIPTION

The NJM2240 is the quadruple oscillator of video band subcarrier frequency with PLL circuit technique. The NJM2240 is suit to standard clock generator of CCD clock and on-screen display.

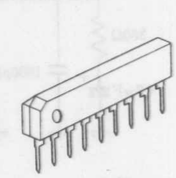
■ PACKAGE OUTLINE



NJM2240D



NJM2240M



NJM2240S

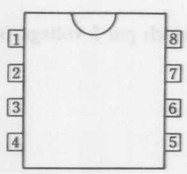
■ FEATURES

- Operating Voltage (+4.7V~+5.3V)
- High Input Sensitivity
- Maximum Oscillator Frequency
- Ouadrupler Output
- Package Outline DIP8, DMP8, SIP9
- Bipolar Technology

■ APPLICATION

- VCR Video Camera AV-TV Video Disc Player

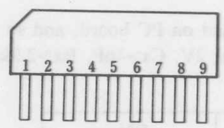
■ PIN CONFIGURATION



NJM2240D
NJM2240M

PIN FUNCTION

1. f_{SC} Input
2. Detection Filter
3. GND
4. Oscillator Output
5. Oscillator C
6. V+
7. Oscillator R
8. NC

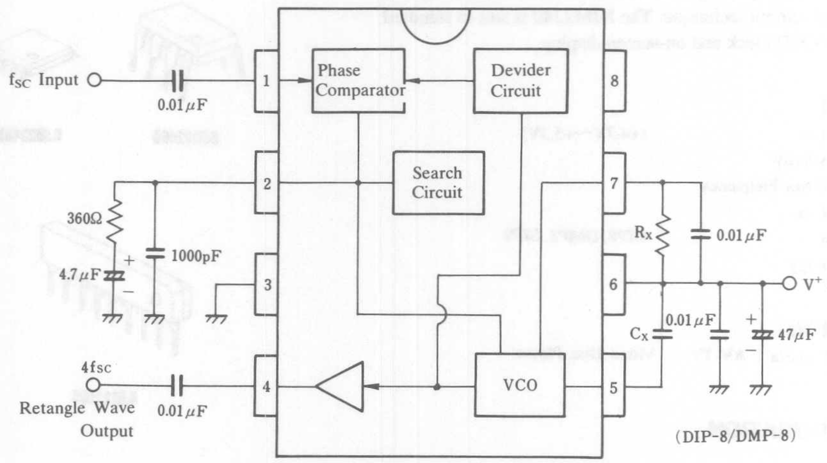


NJM2240S

PIN FUNCTION

1. f_{SC} Input
2. Detection Filter
3. GND 1
4. Oscillator Output
5. GND 2
6. Oscillator C
7. V+
8. Oscillator R
9. NC

■ BLOCK DIAGRAM & EXTERNAL COMPONENTS



(DIP-8/DMP-8)

There is stray capacity assembled on PC board, and so select Rx, Cx to the value which pin 2 voltage (search voltage at VCO locked) becomes about 2V. Cx>4pF, Rx>2.7kΩ.

	NTSC	PAL
	4 Multiplier	4 Multiplier
Cx	6 p	5 p
Rx	4.3k	3.3k

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

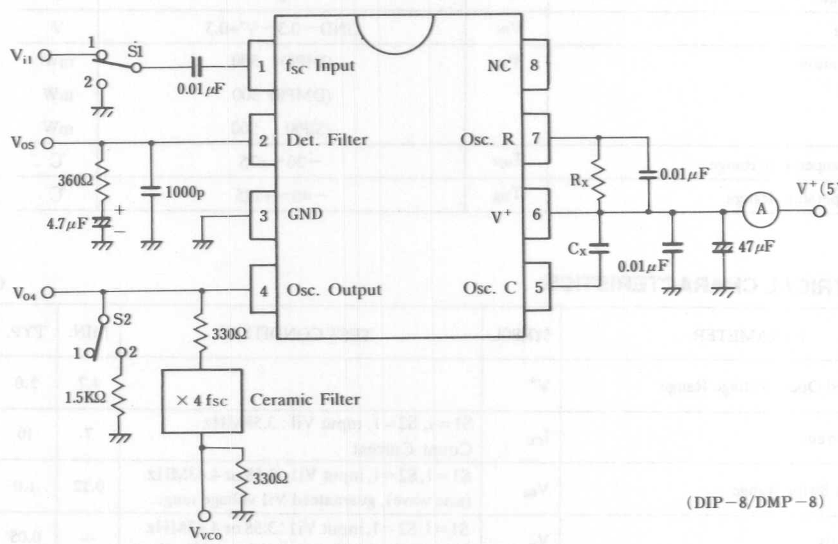
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Input Voltage	V_{IN}	GND−0.3~V^++0.3	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(SIP8) 500	mW
Operating Temperature Range	T_{opr}	−20~+75	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Recommended Oper. Voltage Range	V^+		4.7	5.0	5.3	V
Operating Current	I_{CC}	S1=1, S2=1, input Vi1 : 3.58MHz Count Current	7	10	13	mA
Input Voltage Swing Range	V_{fsc}	S1=1, S2=1, input Vi1 : 3.58 or 4.43MHz (sine wave), guaranteed Vi1 voltage range.	0.12	1.0	2.0	Vp-p
Input Sensitivity	V_{is}	S1=1, S2=1, input Vi1 : 3.58 or 4.43MHz (sine wave), actually tested minimum Vi1 voltage.	—	0.05	—	Vp-p
VCO Oscillation Swing	V_{O4}	S1=1, S2=2, input Vi1 : 3.58MHz, 1.0V_{p-p}	0.7	0.9	1.1	Vp-p
fsc Leakage	L_{fsc}	S1=1, S2=2, input Vi1 : 3.58MHz, 1.0V_{p-p} V_{O4} (fsc level/4fsc level)	—	−50	—	dB
4fsc Output Duty	D_{4fsc}	S1=1, S2=2, input Vi1 : 3.58MHz, 1.0Vp-p, V_{O4} output signal duty.	45	50	55	%

■ TEST CIRCUIT



(DIP−8/DMP−8)

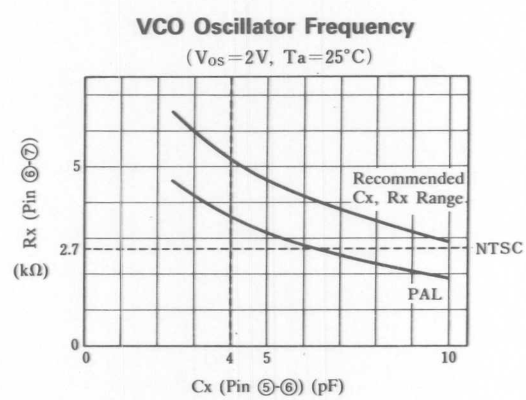
(note 1): Rx, Cx accuracy: less than ±1%

(note 2): Cx is not considered pin5 stray capacitance. VCO free-run frequency is affected by stray capacitance of PC board, socket and others.

(note 3): The NJM2240 is produced by high frequency wafer process and some of pin may be weak against surge voltage.

(note 4): Pin 2 filter must be connected to ground.

■ TYPICAL CHARACTERISTICS

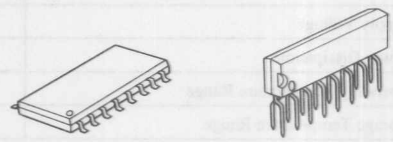


SYNCHRONOUS SEPARATION WITH AFC

■ GENERAL DESCRIPTION

The NJM2229 has functions of getting the horizontal and vertical synchronous signal from the composit video signal by the synchronous separation circuit. Also the NJM2229 has a detective terminal of the input signal through the synchronous circuit.

■ PACKAGE OUTLINE



NJM2229M NJM2229S

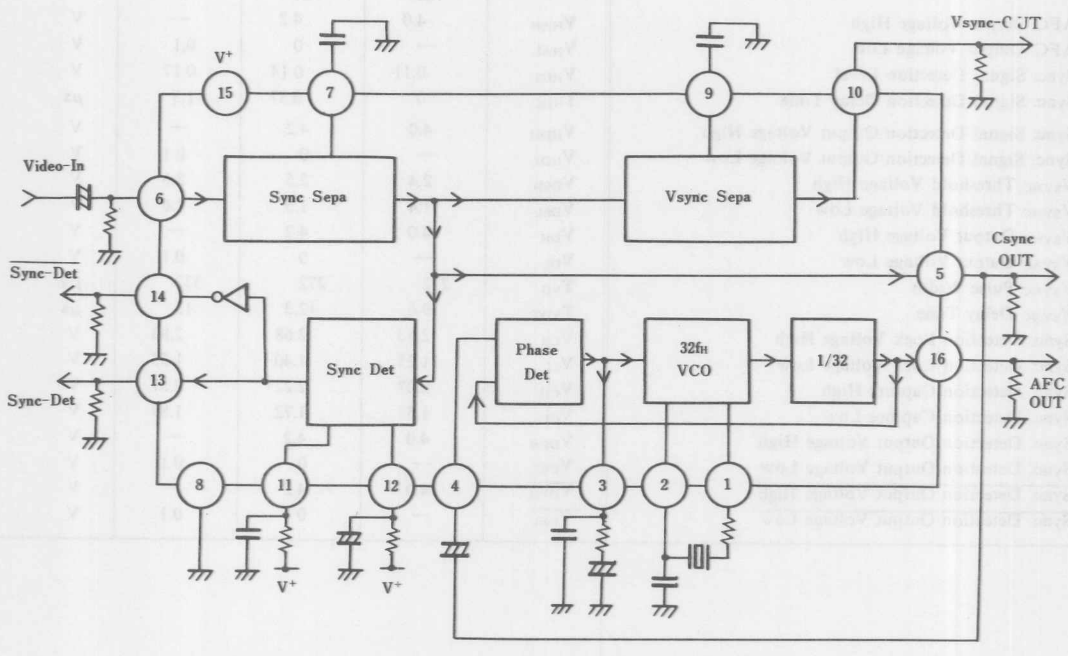
■ FEATURES

- Operating Voltage (+4.7V~+5.3V)
- Internal AFC circuit (Horizontal sync. signal)
- No adjustment of free run frequency.
- Internal detective circuit of sync. signal.
- Package Outline DIP16, ZIP-16
- Bipolar Technology

■ RECOMMENDED OPERATING CONDITION

- Operating Voltage 4.7~5.3V

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

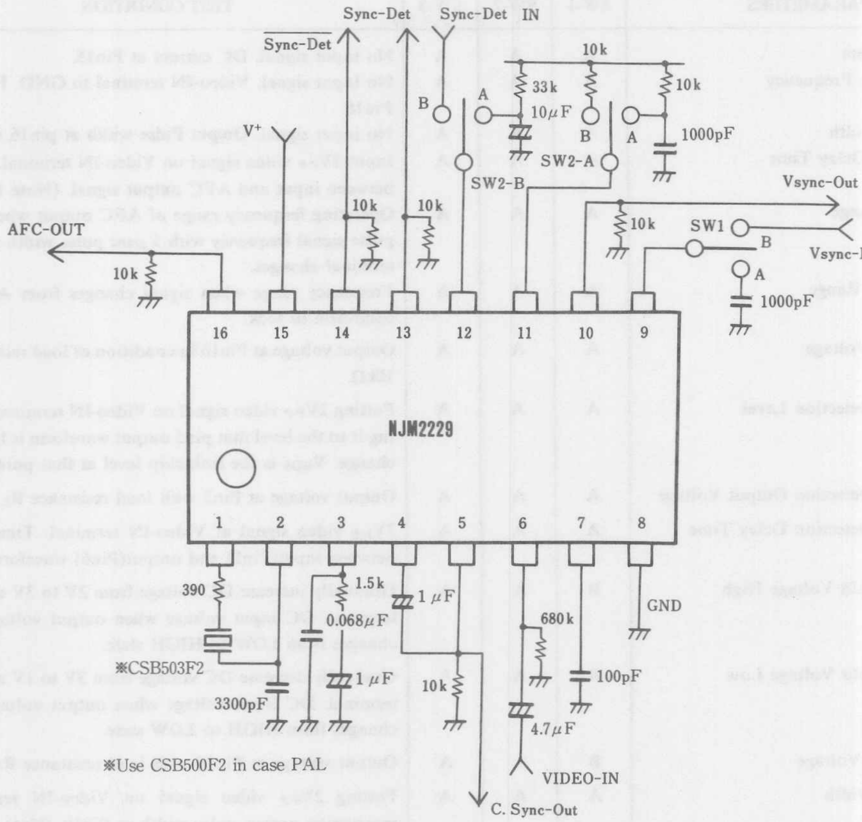
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	7	V
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{opr}	−20〜+75	℃
Storage Temperature Range	T_{stg}	−40〜+125	℃

■ ELECTRICAL CHARACTERISTICS

($Ta=25℃, V^+=5V$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	—	20	26	mA
AFC Free-run Frequency	f_{OH}	15.534	15.734	15.934	kHz
AFC Pulse Width	T_{HD}	3.7	3.9	4.1	μs
AFC Delay	T_{HA}	0.7	1.7	2.7	μs
AFC Lock Range	Δf_{HL}	+600	+700	—	Hz
		−900	−1000	—	
AFC Capture Range	Δf_{HP}	+400	+600	—	Hz
		−700	−900	—	
AFC Output Voltage High	V_{HAH}	4.0	4.2	—	V
AFC Output Voltage Low	V_{HAL}	—	0	0.1	V
Sync. Signal Detection Level	V_{HDS}	0.11	0.14	0.17	V
Sync. Signal Detection Delay Time	T_{HDC}	0	0.57	1.5	μs
Sync. Signal Detection Output Voltage High	V_{HDH}	4.0	4.2	—	V
Sync. Signal Detection Output Voltage Low	V_{HDL}	—	0	0.1	V
V_{SYNC} Threshold Voltage High	V_{DSH}	2.4	2.5	2.6	V
V_{SYNC} Threshold Voltage Low	V_{DSL}	1.4	1.5	1.6	V
V_{SYNC} Output Voltage High	V_{DH}	4.0	4.2	—	V
V_{SYNC} Output Voltage Low	V_{DL}	—	0	0.1	V
V_{SYNC} Pulse Width	T_{VD}	212	272	332	μs
V_{SYNC} Delay Time	T_{VDT}	9.6	12.3	15	μs
Sync. Detection Lock Voltage High	V_{LH}	2.53	2.68	2.83	V
Sync. Detection Lock Voltage Low	V_{LL}	1.25	1.40	1.55	V
Sync. Detection Capture High	V_{CH}	2.07	2.22	2.37	V
Sync. Detection Capture Low	V_{CL}	1.57	1.72	1.87	V
Sync. Detection Output Voltage High	V_{DEH}	4.0	4.2	—	V
Sync. Detection Output Voltage Low	V_{DEL}	—	0	0.1	V
Sync. Detection Output Voltage High	V_{DEH}	4.0	4.2	—	V
Sync. Detection Output Voltage Low	V_{DEL}	—	0	0.1	V

■ TEST CIRCUIT

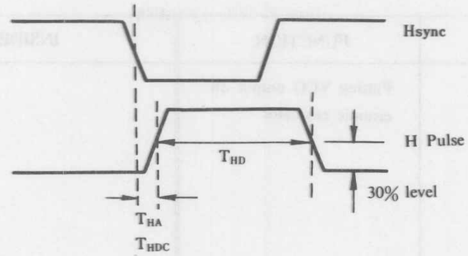


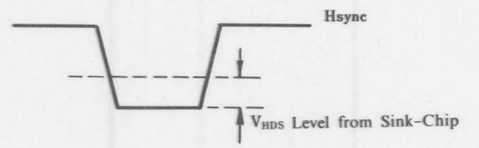
※Use CSB500F2 in case PAL

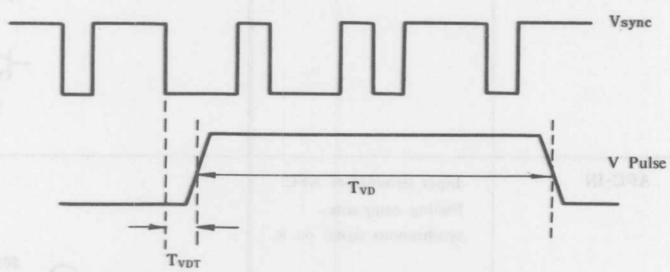
■ ELECTRICAL PARAMETER TEST METHOD

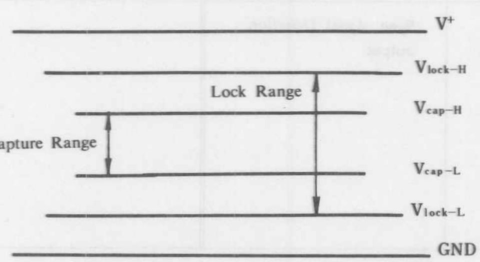
Test Circuit:

PARAMETERS	SW-1	SW-2	SW-3	TEST CONDITION
Operating Current	A	A	A	No input signal. DC current at Pin15.
AFC Free-run Frequency	A	A	A	No input signal. Video-IN terminal to GND. Frequency at Pin16.
AFC Pulse Width	A	A	A	No input signal. Output Pulse width at pin16. (Note 1)
AFC Output Delay Time	A	A	A	Input $2V_{P-P}$ video signal on Video-IN terminal. Delay time between input and AFC output signal. (Note 1)
AFC Lock Range	A	A	A	Operating ferquency range of AFC output when the input pulse signal frequency with 5 μsec pulse width at Video-IN terminal changes.
AFC Capture Range	A	A	A	Frequency range when signal changes from AFC unlock condition to lock.
AFC Output Voltage	A	A	A	Output voltage at Pin16 in condition of load resistance R_L= 10kΩ.
Sync. Signal Detection Level	A	A	A	Putting $2V_{P-P}$ video signal on Video-IN terminal and reducing it to the level that pin5 output waveform is beginning to change. V_{HDS} is the sink-chip level at that point. (Note 2)
Sync. Signal Detection Output Voltage	A	A	A	Output voltage at Pin5 with load resistance R_L=10kΩ.
Sync. Signal Detection Delay Time	A	A	A	$2V_{P-P}$ video signal at Video-IN terminal. Time difference between input(Pin5) and output(Pin6) waveform.
V_{SYNC} Threshold Voltage High	B	A	A	Gradually increase DC voltage from 2V to 3V at V_{SYNC}-IN terminal. DC input voltage when output voltage at Pin10 changes from LOW to HIGH state.
V_{SYNC} Threshold Voltage Low	B	A	A	Gradually decrease DC voltage from 3V to 1V at V_{SYNC}-IN terminal. DC input voltage when output voltage at Pin10 changes from HIGH to LOW state.
V_{SYNC} Output Voltage	B	A	A	Output voltage at Pin10 with load resistance R_L=10kΩ.
V_{SYNC} Pulse Width	A	A	A	Putting $2V_{P-P}$ video signal on Video-IN terminal and measurring output pulse width at Pin10. (Note 3)
V_{SYNC} Delay Time	A	A	A	Putting $2V_{P-P}$ video signal on Video-IN terminal. Delay time between output at Pin10 and V_{SYNC} at Pin6. (Note 3)
Sync. Detection Lock Voltage High	A	B	B	Increase DC voltage from 2V to 4V put on Sync-Det-IN terminal and measure its DC voltage when output voltage at Pin13 changes from HIGH to LOW. (Note 4)
Sync. Detection Lock Voltage Low	A	B	B	Decrease DC voltage from 2V to 1V put on Sync-Det-IN terminal and measure its DC voltage when output voltage at Pin13 changes from HIGH to LOW. (Note 4)
Sync. Detection Capture High	A	B	B	Decrease DC voltage from 3V to 1V put on Sync-Det-IN terminal and measure its DC voltage when output voltage at Pin13 changes from LOW to HIGH. (Note 4)
Sync. Detection Capture Low	A	B	B	Increase DC voltage from 1V to 2V put on Sync-Det-IN terminal and measure its DC voltage when output voltage at Pin13 changes from LOW to HIGH. (Note 4)
Sync. Detection Output Voltage	A	B	B	Output voltage at Pin13 with load resistance R_L=10kΩ.
Sync. Detection Output Voltage	A	B	B	Output voltage at Pin14 with load resistance R_L=10kΩ.

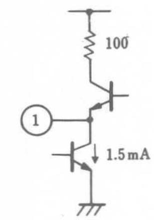
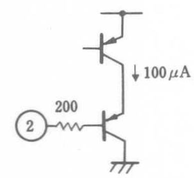
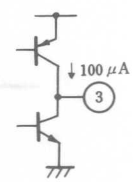
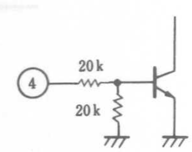
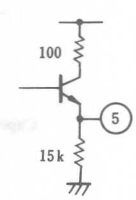

Hsync
H Pulse
T_{HD}
30% level
T_{HA}
T_{HDC}

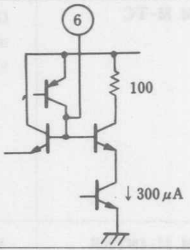
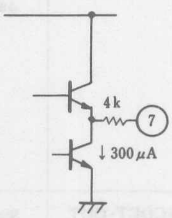
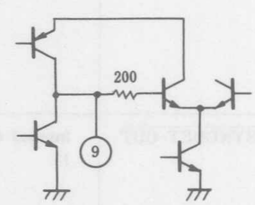
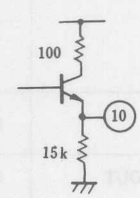

Hsync
V_{HDS} Level from Sink-Chip

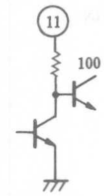
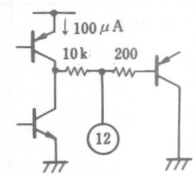
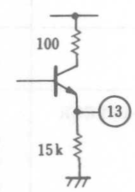
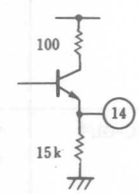
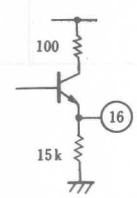

Vsync
V Pulse
T_{VD}
T_{VDT}


V^+
V_{lock-H}
Lock Range
V_{cap-H}
Capture Range
V_{cap-L}
V_{lock-L}
GND

■ PIN FUNCTION

PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	VCO-OUT	Putting VCO output on ceramic resonator.	
2	VCO-FILTER	Deciding phase of ceramic resonator.	
3	AFC-FILTER	Low pass filter of AFC.	
4	AFC-IN	Input terminal of AFC. Putting composite. synchronous signal on it.	
5	C. SYNC-OUT	Sync. signal Detection output	

PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
6	VIDEO-IN	Input composite video signal.	
7	L. P. F	Low pass filter for chroma signal.	
8	GND	Ground.	
9	SYNC-INTEGR	Integrating composite synchronous signal and putting vertical synchronous reproducing circuit.	
10	VSYNC-OUT	Vertical synchronous output.	

PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
11	M. M-TC	Deciding time constant of M. M. V. (monomulti vibrator)	
12	M. M-INTER	Smoothing M. M. V. output.	
13	SYNCDET-OUT	Signal detective output.	
14	$\overline{\text{SYNCDET-OUT}}$	Inversed output of Pin 13.	
15	V^+	Power supply.	
16	AFC-OUT	AFC output.	

3-INPUT VIDEO SWITCH WITH 75Ω DRIVER

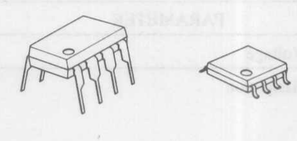
■ GENERAL DESCRIPTION

The NJM2243 is a three input integrated video switch which selects one video or audio signal from three input signals.

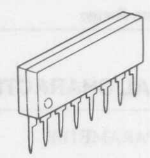
It contains driver circuit for 75 Ω load and is able to connect to TV monitor.

Its operating supply voltage range is 9 to 12V and bandwidth is 10MHz. Crosstalk is 70dB (at 4.43MHz).

■ PACKAGE OUTLINE



NJM2243D NJM2243M



NJM2243L

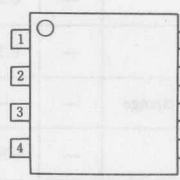
■ FEATURES

- Operating Voltage 9~13V
- 3 Input-1 Output
- Internal Driver Circuit for 75 Ω Impedance
- Muting Function available
- Low power Dissipation 15mA
- Cross-talk 70dB(at 4.43MHz)
- Wide Frequency Range 10MHz
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

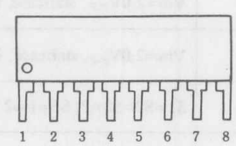
■ APPLICATION

- VCR Video Camera AV-TV Video Disc Player

■ PIN CONFIGURATION



NJM2243D
NJM2243M



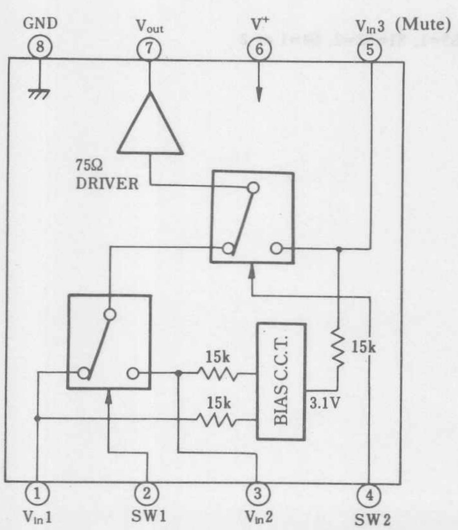
NJM2243L

PIN FUNCTION

1 . $V_{in}1$
2 . SW1
3 . $V_{in}2$
4 . SW2
5 . $V_{in}3$
6 . V^+
7 . V_{out}
8 . GND

■ BLOCK DIAGRAM

Pin Connection



■ INPUT CONTROL SIGNAL-OUTPUT SIGNAL

SW 1	SW 2	OUTPUT SYGNAL
L	L	$V_{IN}1$
H	L	$V_{IN}2$
L/H	H	$V_{IN}3$

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DIP8) 500 (DMP8) 300 (SIP8) 800	mW mW mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

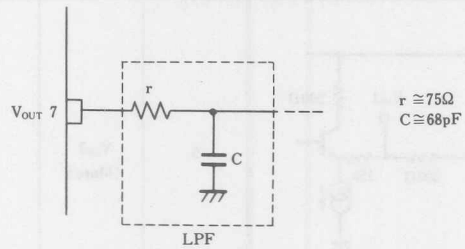
(V^+=9V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage	V^+		8.5	—	13.0	V
Operating Current	I_{CC}	S1=S2=S3=S4=S5=2	13.0	18.5	25.0	mA
Voltage Gain	G_V	Vin=2.0V_{P-P}, 100kHz, Vo/Vi, R_L =150Ω	−0.8	−0.3	+0.2	dB
Frequency Characteristics	G_f	Vin=2.0V_{P-P}, V_0(10MHz)/V_0(100kHz),R_L=1kΩ	−1.0	—	+1.0	dB
Differential Gain	DG	Vin=2.0V_{P-P}, staircase, R_L =150Ω	—	0.3	—	%
Differential Phase	DP	Vin=2.0V_{P-P}, staircase, R_L=150Ω	—	0.3	—	deg.
Output Offset Voltage	V_{off}	S1=S2=S3=2, S5=1→2 V_O:Voltage change	—	—	±30	mV
Crosstalk	CT	Vin=2V_{P-P}, 4.43MHz, Vo/Vi	—	−70	—	dB
Switch Change Voltage	V_{CH}	All inside Sw:ON	2.4	—	—	V
	V_{CL}	All inside Sw:OFF	—	—	0.8	V
Input Impedance	R_I		—	15	—	kΩ

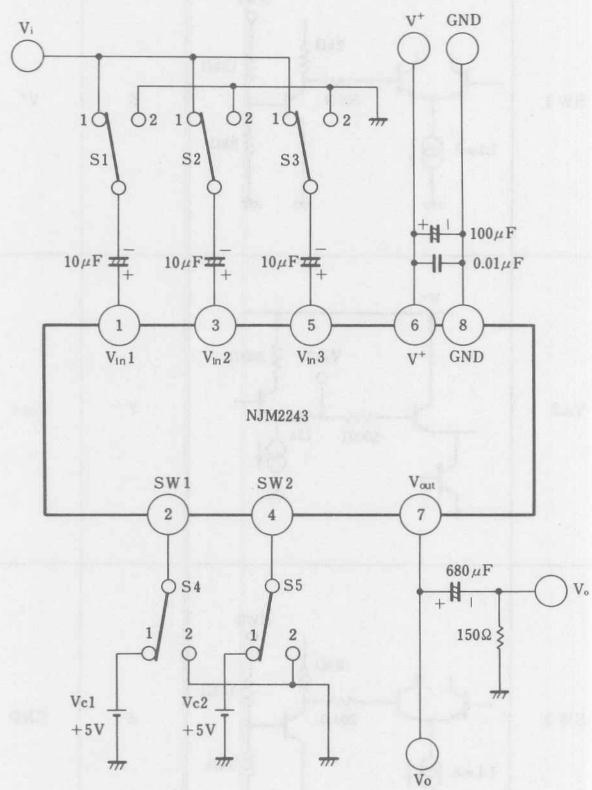
(note) Unless specified, tested with three mode below.
a) S1=1, S2=S3=S4=S5=2 b) S2=S4=1, S1=S3=S5=2 c) S3=S5=1, S1=S2=2, S4=1 or 2

■ APPLICATION

Oscillation Prevention on light loading conditions
Recommended under circuit



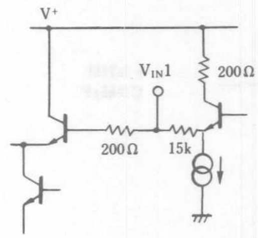
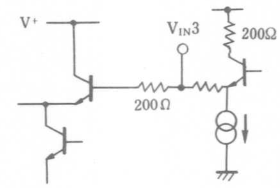
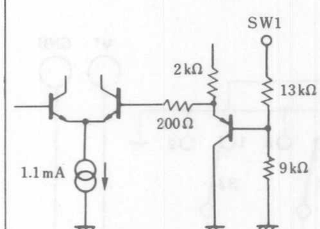
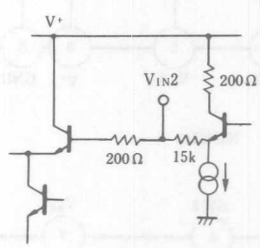
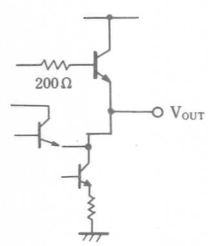
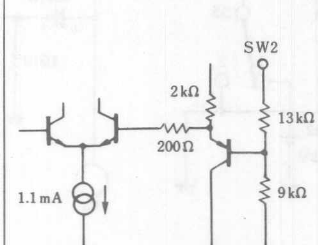
■ TEST CIRCUIT



DC Voltage Each Terminal
Typ. on Test Circuit   Ta =25℃

Terminal Name	$V_{IN}1$	SW1	$V_{IN}2$	SW2	$V_{IN}3$	V^+	V_{OUT}	GND
DC Voltage	$\frac{3}{5}V^+$	—	$\frac{3}{5}V^+$	—	$\frac{3}{5}V^+$	—	$\frac{2}{5}V^+-0.7$	—

■ EQUIVALENT CIRCUIT

PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT	PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	$V_{IN}1$		5	$V_{IN}3$ (Mute)	
2	SW 1		6	V^+	—
3	$V_{IN}2$		7	V_{OUT}	
4	SW 2		8	GND	—

3-INPUT VIDEO SWITCH WITH 75Ω DRIVER

■ GENERAL DESCRIPTION

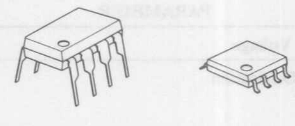
The NJM2244 is a three input integrated video switch witch selects one video or audio signal from three input signals.

It contains driver circuit for 75Ω load and is able to connect to TV monitor.

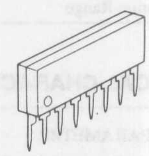
Its operating supply voltage range is 5 to 12V and bandwidth is 10MHz. Crosstalk is 70dB (at 4.43MHz).

NJM2244 contains clamp function and it can be operated while setting DC level fixed in position of the video signal.

■ PACKAGE OUTLINE



NJM2244D NJM2244M



NJM2244L

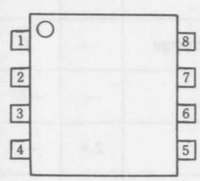
■ FEATURES

- Operating Voltage 4.75～13V
- 3 Input-1 Output
- Internal Driver Circuit for 75Ω Impedance
- Muting Function available
- Internal Clamp Function
- Low power Dissipation 16.5mA
- Cross-talk 70dB(at 4.43MHz)
- Wide Frequency Range 10MHz(2V_{P-P} Input)
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

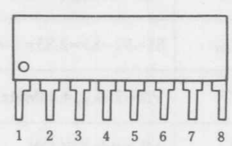
■ APPLICATION

- VCR Video Camera AV-TV Video Disc Player

■ PIN CONFIGURATION



NJM2244D
NJM2244M



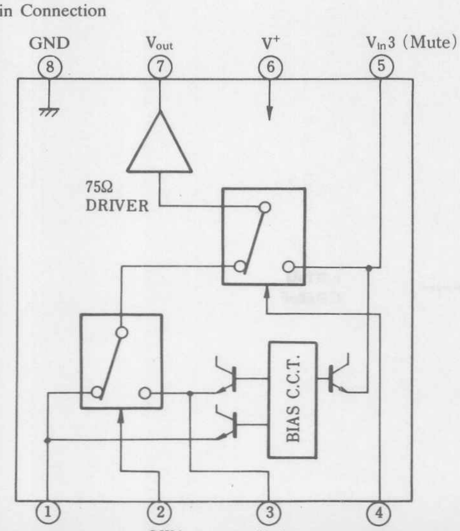
NJM2244L

PIN FUNCTION

1. $V_{in}1$
2. SW1
3. $V_{in}2$
4. SW2
5. $V_{in}3$
6. V^+
7. V_{out}
8. GND

■ BLOCK DIAGRAM

Pin Connection



■ INPUT CONTROL SIGNAL-OUTPUT SIGNAL

SW 1	SW 2	OUTPUT SIGNAL
L	L	$V_{IN}1$
H	L	$V_{IN}2$
L/H	H	$V_{IN}3$

note): Input clamp voltage is about 2/5 of supply voltage.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DIP8) 500 (DMP8) 300 (SIP8) 800	mW mW mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

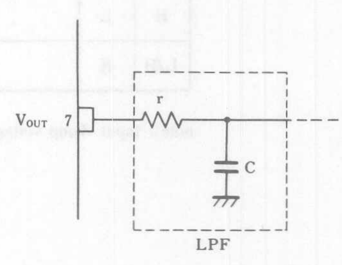
(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage	V^+		4.75	—	13.0	V
Operating Current	I_{CC}	S1=S2=S3=S4=S5=2	11.5	16.5	22.0	mA
Voltage Gain	G_V	Vin=2.0V_{P-P}, 100kHz, Vo/Vi, R_L=150Ω	−0.8	−0.3	+0.2	dB
Frequency Characteristic	G_f	Vin=2.0V_{P-P}, V_O(10MHz)/V_O(100kHz) R_L=150Ω	−1.0	—	+1.0	dB
Differential Gain	DG	Vin=2.0V_{P-P}, staircase, R_L=150Ω	—	0.3	—	%
Differential Phase	DP	Vin=2.0V_{P-P}, staircase, R_L=150Ω	—	0.3	—	deg.
Output Offset Voltage	V_{off}	S1=S2=S3=2,S5=1→2 V_O:voltage change	—	0	±30	mV
Crosstalk	CT	Vin=2V_{P-P}, 4.43MHz, V_O/Vi	—	−70	—	dB
Switch Change Voltage	V_{CH}	All inside SW:ON	2.4	—	—	V
	V_{CL}	All inside SW:OFF	—	—	0.8	V

(note) Unless specified, tested with three mode below.
a) S1=1, S2=S3=S4=S5=2 b) S2=S4=1, S1=S3=S5=2 c) S1=S2=2, S3=S5=1, S4=1 or 2

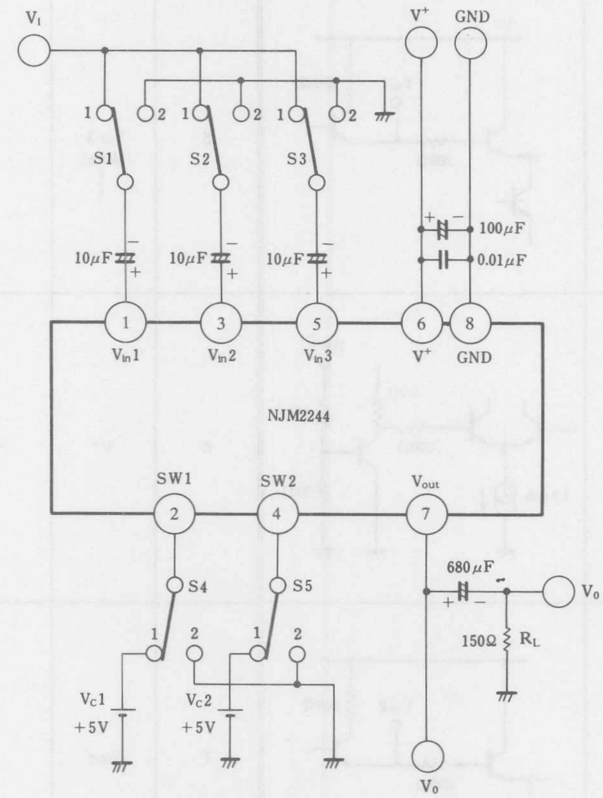
■ APPLICATION

Oscillation Prevention on light loading conditions
Recommended under circuit



r ≅ 75Ω
C ≅ 68pF

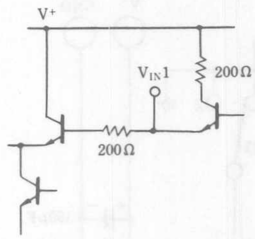
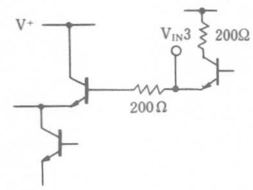
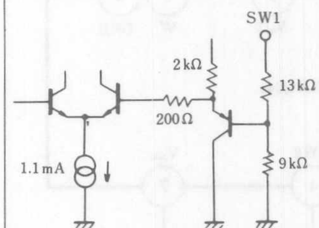
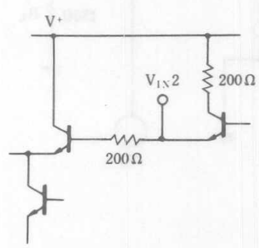
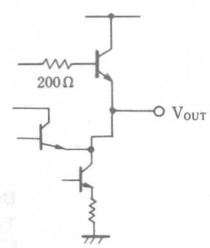
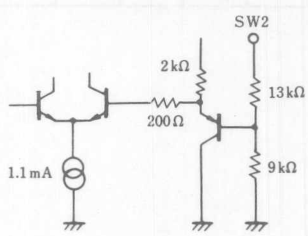
■ TEST CIRCUIT



DC Voltage Each Terminal
Typ. on Test Circuit Ta =25℃

Terminal Name	$V_{IN}1$	SW1	$V_{IN}2$	SW2	$V_{IN}3$	V^+	V_{OUT}	GND
DC Voltage	$\frac{2}{5}V^+$	—	$\frac{2}{5}V^+$	—	$\frac{2}{5}V^+$	—	$\frac{2}{5}V^+-0.7$	—

■ EQUIVALENT CIRCUIT

<table>
<tr><th>PIN NO.
PIN</th><th>FUNCTION</th><th>INSIDE EQUIVALENT CIRCUIT</th><th>PIN NO.
PIN</th><th>FUNCTION</th><th>INSIDE EQUIVALENT CIRCUIT</th></tr>
<tr><td>1</td><td>V_{IN} 1</td><td>
</td><td>5</td><td>V_{IN} 3
(Mute)</td><td>
</td></tr>
<tr><td>2</td><td>SW 1</td><td>
</td><td>6</td><td>V^+</td><td></td></tr>
<tr><td>3</td><td>V_{IN} 2</td><td>
</td><td>7</td><td>V_{OUT}</td><td>
</td></tr>
<tr><td>4</td><td>SW 2</td><td>
</td><td>8</td><td>GND</td><td></td></tr>
</table>

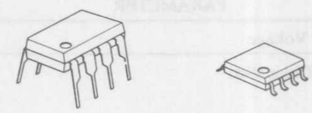
3-INPUT VIDEO SWITCH WITH 6dB AMPLIFIER

■ GENERAL DESCRIPTION

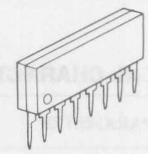
The NJM2245 is a three input integrated video switch witch selects one video or audio signal from three input signals.

It contains 6dB amplifier and its operating supply voltage range is 8.5 to 13V and bandwidth is 5MHz. Crosstalk is 65dB (at 4.43MHz).

■ PACKAGE OUTLINE



NJM2245D NJM2245M



NJM2245L

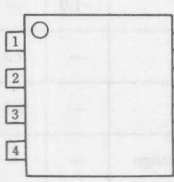
■ FEATURES

- Operating Voltage 8.5～13V
- 3 Input-1 Output
- Internal 6dB Amplifier
- Muting Function available
- Cross-talk 65dB(at 4.43MHz)
- Wide Frequency Range 5MHz(1V_{P-P} Input)
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

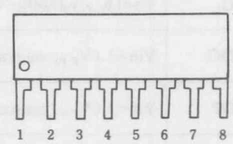
■ APPLICATION

- VCR AV-TV Video Disc Player

■ PIN CONFIGURATION



NJM2245D
NJM2245M

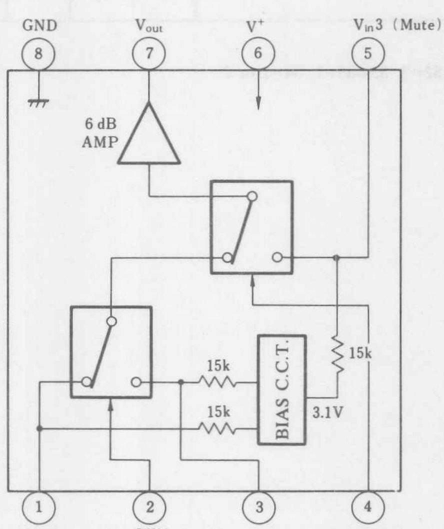


NJM2245L

PIN FUNCTION

1. $V_{in}1$
2. SW1
3. $V_{in}2$
4. SW2
5. $V_{in}3$
6. V^+
7. V_{out}
8. GND

■ BLOCK DIAGRAM



■ INPUT CONTROL SIGNAL-OUTPUT SIGNAL

SW 1	SW 2	OUTPUT SIGNAL
L	L	$V_{IN}1$
H	L	$V_{IN}2$
L/H	H	$V_{IN}3$

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(SIP8) 800	mW
Operating Temperature Range	T_{opr}	−20〜+75	℃
Storage Temperature Range	T_{stg}	−40〜+125	℃

■ ELECTRICAL CHARACTERISTICS

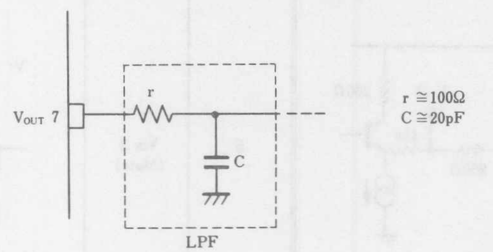
(V^+=9V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage	V^+		8.5	—	13.0	V
Operating Current	I_{CC}	S1=S2=S3=S4=S5=2	10.0	16.5	23.0	mA
Voltage Gain	Gv	Vin=1.0V_{P-P}, 100kHz, Vo/Vi, R_L=1kΩ	5.7	6.2	6.7	dB
Frequency Characteristic	G_f	Vin=1.0$_{P-P}$, V_O(10MHz)/V_O(100kHz) R_L=1kΩ	−1.0	—	+1.0	dB
Differential Gain	DG	Vin=1.0V_{P-P}, staircase, R_L=1kΩ	—	0.3	—	%
Differential Phase	DP	Vin=1.0V_{P-P}, staircase, R_L=1kΩ	—	0.3	—	deg.
Output Offset Voltage	V_{off}	S1=S2=S3=2, S5=1→2 V_O:voltage change	—	—	±60	mV
Crosstalk	CT	Vin=1V_{P-P}, 4.43MHz, V_O/Vi	—	−65	—	dB
Switch Change Voltage	V_{CH}	All inside SW:ON	2.4	—	—	V
	V_{CL}	All inside SW:OFF	—	—	0.8	V
Input Impedance	R_I		—	15	—	kΩ

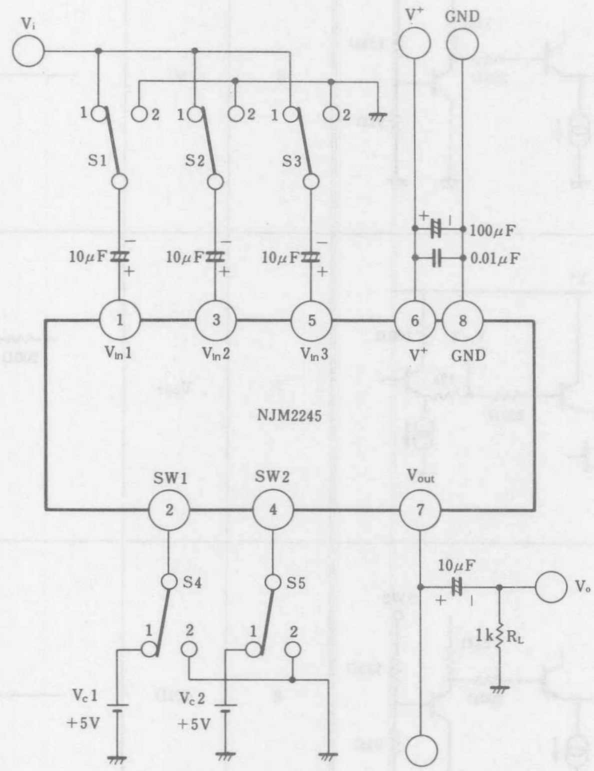
(note) Unless specified, tested with three mode below.
a) S1=1, S2=S3=S4=S5=2 b) S2=S4=1, S1=S3=S5=2 c) S1=S2=2, S3=S5=1, S4=1 or 2

■ APPLICATION

Oscillation Prevention on light loading conditions Recommended under circuit.



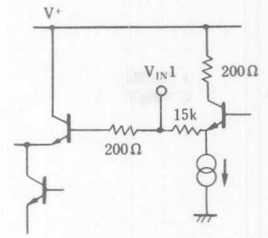
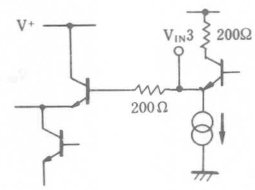
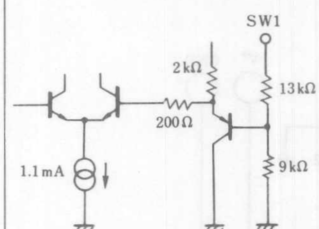
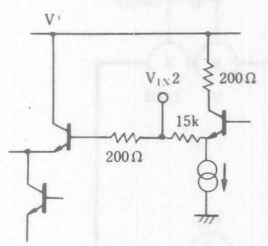
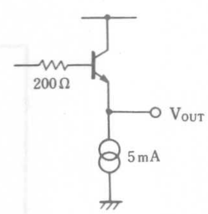
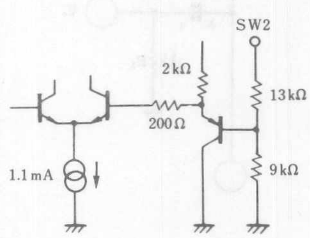
■ TEST CIRCUIT



DC Voltage Each Terminal
Typ. on Test Circuit   Ta = 25℃

Terminal Name	$V_{IN}1$	SW1	$V_{IN}2$	SW2	$V_{IN}3$	V^+	V_{OUT}	GND
DC Voltage	$\frac{2}{5}V^+$	—	$\frac{2}{5}V^+$	—	$\frac{2}{5}V^+$	—	$\frac{2}{5}V^+-2.1$	—

■ EQUIVALENT CIRCUIT

PIN NO. PIN	FUNCTION	INSIDE EQUIVALENT CIRCUIT	PIN NO. PIN	FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	V_{IN} 1		5	V_{IN} 3 (Mute)	
2	SW 1		6	V^+	
3	V_{IN} 2		7	V_{OUT}	
4	SW 2		8	GND	

3-INPUT VIDEO SWITCH WITH 6dB AMPLIFIER

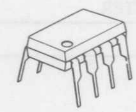
■ GENERAL DESCRIPTION

The NJM2246 is three input integrated video switch witch selects one video or audio signal from three input signals

It contains 6dB ampplifier and its operating supply voltage range is 4.75 to 13V and bandwidth is 5MHz.

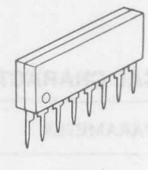
Crosstalk is 65dB (at 4.43MHz).

■ PACKAGE OUTLINE



NJM2246D

NJM2246M



NJM2246L

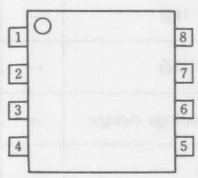
■ FEATURES

- Operating Voltage 4.75～13V
- 3 Input-1 Output
- Internal 6dB Amplifier
- Muting Function available
- Internal Clamp Function
- Cross-talk 65dB(at 4.43MHz)
- Wide Frequency Range 5MHz(1V_{P-P} Input)
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

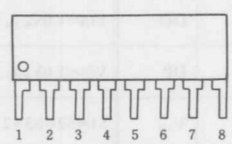
■ APPLICATION

- VCR. AV-TV Video Disc Player

■ PIN CONFIGURATION



NJM2246D
NJM2246M

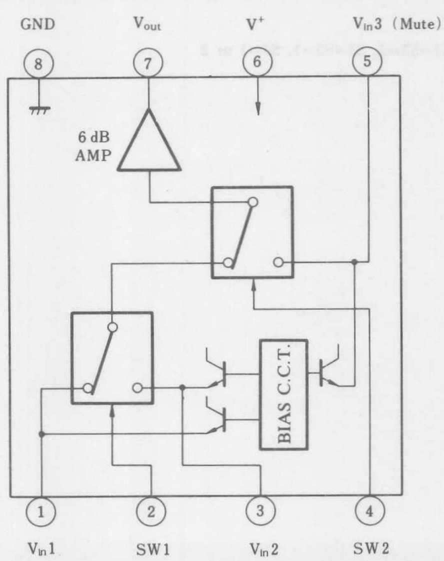


NJM2246L

PIN FUNCTION

1. $V_{in}1$
2. SW1
3. $V_{in}2$
4. SW2
5. $V_{in}3$
6. V^+
7. V_{out}
8. GND

■ BLOCK DIAGRAM



■ INPUT CONTROL SIGNAL-OUTPUT SIGNAL

SW 1	SW 2	OUTPUT SIGNAL
L	L	$V_{IN}1$
H	L	$V_{IN}2$
L/H	H	$V_{IN}3$

note): Input clamp voltage is about 2/5 of supply voltage.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(SIP8) 800	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

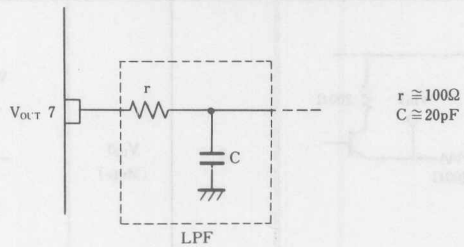
(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage	V^+		4.75	—	13.0	V
Operating Current	I_{CC}	S1=S2=S3=S4=S5=2	9.5	14.0	21.0	mA
Voltage Gain	Gv	Vin=1.0V_{p-p}, 1MHz, Vo/Vi, R_L=1kΩ	5.5	6.0	6.5	dB
Frequency Characteristic	Gf	Vin=1.0V_{p-p}, V_0(10MHz)/V_0(1MHz)R_L=1kΩ	−1.0	—	+1.0	dB
Differential Gain	DG	Vin=1.0V_{P-P}, staircase, R_L=1kΩ	—	0.3	—	%
Differential Phase	DP	Vin=1.0V_{P-P}, staircase, R_L=1kΩ	—	0.3	—	deg.
Output Offset Voltage	V_{off}	S1=S2=S3=2, S5=1→2 V_O:voltage change	—	—	±60	mV
Crosstalk	CT	Vin=1V_{P-P}, 4.43MHz, V_O/Vi	—	−65	—	dB
Switch Change Voltage	V_{CH}	All inside SW:ON	2.4	—	—	V
	V_{CL}	All inside SW:OFF	—	—	0.8	V

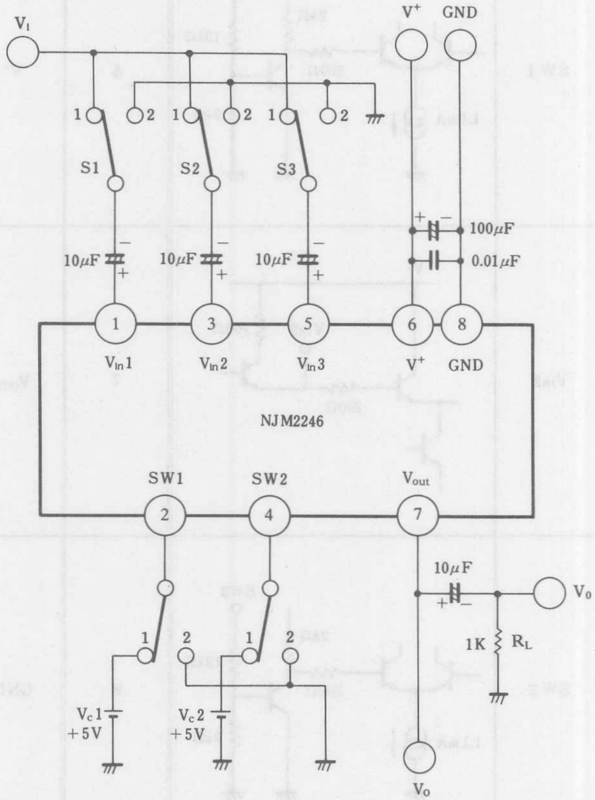
(note) Unless specified, tested with three mode below.
a) S1=1, S2=S3=S4=S5=2 b) S2=S4=1, S1=S3=S5=2 c) S1=S2=2, S3=S5=1, S4=1 or 2

■ APPLICATION

Oscillation Prevention on light loading conditions Recommended under circiut.



■ TEST CIRCUIT

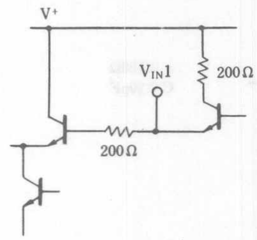
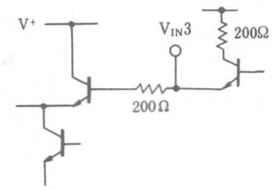
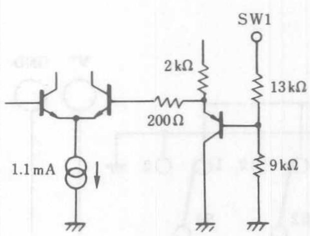
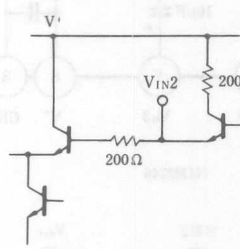
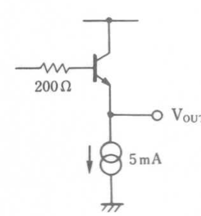
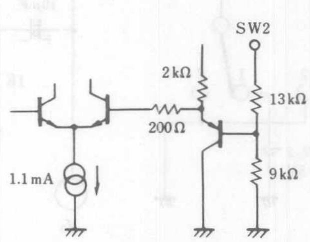


DC Voltage Each Terminal

Typ. on Test Circuit Ta = 25℃

Terminal Name	$V_{IN}1$	SW1	$V_{IN}2$	SW2	$V_{IN}3$	V^+	V_{OUT}	GND
DC Voltage	$\frac{2}{5}V^+$	—	$\frac{2}{5}V^+$	—	$\frac{2}{5}V^+$	—	$\frac{2}{5}V^+-0.7$	—

■ EQUIVALENT CIRCUIT

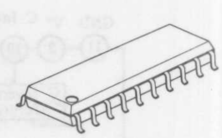
PIN NO PIN	FUNCTION	INSIDE EQUIVALENT CIRCUIT	PIN NO. PIN	FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	$V_{IN}1$		5	$V_{IN}3$ (Mute)	
2	SW 1		6	V^+	———
3	$V_{IN}2$		7	V_{OUT}	
4	SW 2		8	GND	———

VIDEO COLOR SUPERIMPOSER

■ GENERAL DESCRIPTION

NJM2247 A/B is the multi-functional color superimposer IC for video base band (Y. R-Y, B-Y). Various type of Y, R-Y, B-Y output signals can be made by the digital controlled signals. The signal control at the base band, made it possible on operation with less external parts, as well as for non adjustment on opertaion.

■ PACKAGE OUTLINE



NJM2247AM/BM

■ FEATURES

- 5V Single Power Supply
- 8 Types Color Superimposer
- Burst Flag Insert Function
- Y Inversion, C Inversion Function
- NTSC/PAL Matching
- Non Operational Adjustment
- Less External Parts
- Package Outline DMP20
- Bipolar Technology

■ RECOMMENDED INPUT CONDITIONS

- Y Signal 0.7 V_{P-P}
- R-Y Signal 1.0 V_{P-P}
- B-Y Signal 0.7 V_{P-P}
- Control Voltage
- Low Level 0~0.25 V
- High Level 4.75~5 V

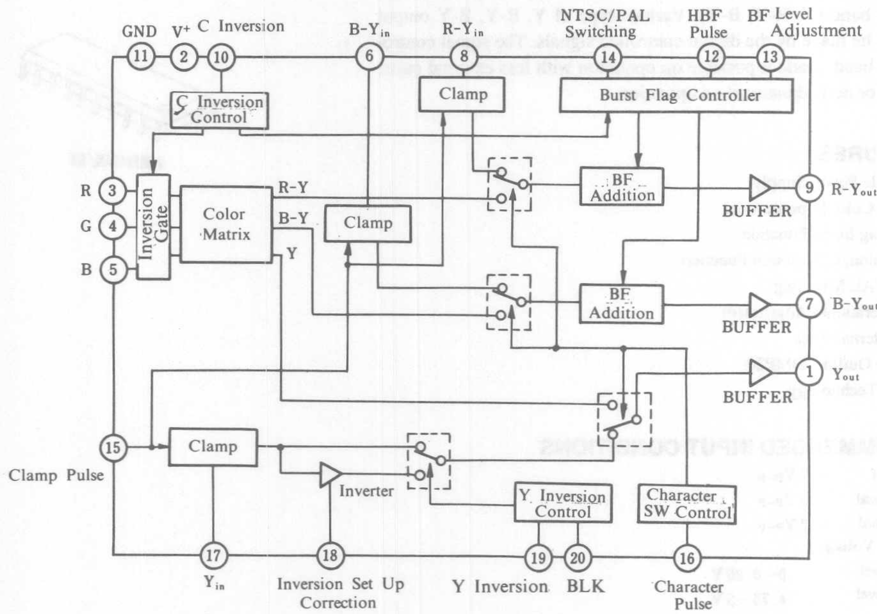
■ PIN CONFIGURATION

NJM2247AM/BM

PIN FUNCTION

1. Y_{out}	11. GND
2. V^+	12. HBF Pulse
3. R	13. BF
4. G	14. NTSC/PAL Switching
5. B	15. Clamp Pulse
6. $B-Y_{in}$	16. Character Pulse
7. $B-Y_{out}$	17. Y_{in}
8. $R-Y_{in}$	18. Inversion Set up Correction
9. $R-Y_{out}$	19. Y Inversion
10. C Inversion	20. BLK Pulse

■ BLOCK DIAGRAM

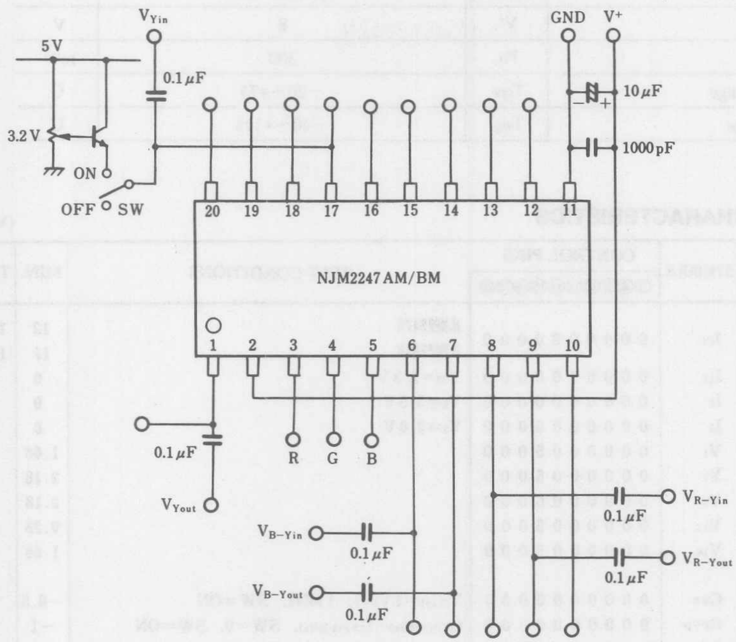


■ CONTROL PIN CHARACTERISTICS

(V^+=5V)

PIN NO.	PIN FUNCTIONS	THRESHOLD LEVEL(V)		SINK/SOURCE CURRENT(μA)	
		LOW	HIGH	0V	5V
3 4 5	R G B	0.7	0.8	−500	500
3 4 5	(at C Inversion)	2.5	2.6	−100	100
10	C Inversion	3.5	4.5	−200	400
12	HBF Pulse	0.5	2.0	−2	1
14	NTSC/PAL	0.7	0.8	0	150
15	Clamp Pulse	2.5	2.8	−2	0
16	Character Pulse	0.5	0.9	−0.5	0
19	Y Inversion	0.4	0.8	−0.5	0
20	BLK Pulse	0.4	0.8	−0.5	0

■ TEST CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta= 25°C)

PARAMETERS	SYMBOLS	CONTROL PINS ③④⑤⑩⑫⑭⑮⑯⑲⑳	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	0 0 0 0 0 0 0 0 0 0	NJM2247A	12	16.5	22	mA
			NJM2247B	12	18.5	26	mA
Terminal Sink Current 1	I_{17}	0 0 0 0 0 0 0 0 0 0	$V_{17}=2.5V$	0	−	10	μA
Terminal Sink Current 2	I_6	0 0 0 0 0 0 0 0 0 0	$V_6=3.0V$	0	−	6	μA
Terminal Sink Current 3	I_8	0 0 0 0 0 0 0 0 0 0	$V_8=3.0V$	0	−	6	μA
Terminal Voltage 1	V_1	0 0 0 0 0 0 5 0 0 0		1.68	−	1.92	V
Terminal Voltage 2	V_7	0 0 0 0 0 0 5 0 0 0		2.18	−	2.42	V
Terminal Voltage 3	V_9	0 0 0 0 0 0 5 0 0 0		2.18	−	2.42	V
Terminal Voltage 4	V_{13}	0 0 0 0 0 0 5 0 0 0		0.23	−	0.37	V
Terminal Voltage 5	V_{18}	0 0 0 0 0 0 5 0 0 0		1.68	−	1.92	V
Y Non Inversion							
Voltage Gain	G_{YP}	0 0 0 0 0 0 0 0 0 0	$V_{(Yin)}=1V_{P-P}$, 1MHz, SW=ON	−0.5	0	0.5	dB
Frequency Characteristics	G_{FYP}	0 0 0 0 0 0 0 0 0 0	$G_{YP(6MHz)}-G_{YP(1MHz)}$, SW=0, SW=ON	−1	0	1	dB
Differential Gain	DG_P	0 0 0 0 0 0 0 0 0 0	$V_{(Yin)}=1V_{P-P}$, Staircase , SW=ON	−3	0	3	%
Differential Phase	DP_P	0 0 0 0 0 0 0 0 0 0	$V_{(Yin)}=1V_{P-P}$, Staircase , SW=ON	−3	0	3	deg
Y Inversion							
Voltage Gain	G_{YN}	0 0 0 0 0 0 0 0 5 5	$V_{(Yin)}=0.6V_{P-P}$, 1MHz, SW=ON	−2.3	−1.3	0.3	dB
Frequency Characteristics	G_{FYN}	0 0 0 0 0 0 0 0 5 5	$G_{YN(6MHz)}-G_{YN(1MHz)}$, SW=ON	−2	−0.1	1	dB
Differential Gain	DG_N	0 0 0 0 0 0 0 0 5 5	$V_{(Yin)}=0.5V_{P-P}$, Staircase , SW=ON	−8	−	8	%
Differential Phase	DP_P	0 0 0 0 0 0 0 0 5 5	$V_{(Yin)}=0.5V_{P-P}$, Staircase , SW=ON	−3	0	3	deg
Inversion Black Level	BL_N	0 0 0 0 0 0 5 0 5 5 0 0 0 0 0 0 5 0 0 0	① Voltage ; a, $BL_N=a-b$ ① Voltage ; b, $BL_N=a-b$	0.59	0.68	0.77	V
Inversion BLK	BLK	0 0 0 0 0 0 5 0 5 0	① Voltage ; c, BLK=c−b	−0.1	0	0.1	V
R-Y							
Voltage Gain	G_{R-Y}	0 0 0 0 0 0 5 0 0 0	$V_{(R-Yin)}=1V_{P-P}$, 1MHz	−0.5	0	0.5	dB
Burst Level Non Inversion	BF_{RP}	0 0 0 0 0 0 5 0 0 0 0 0 0 0 5 0 5 0 0 0	⑨ Voltage ; d, $BF_{RP}=e-d$ ⑨ Voltage ; e, $BF_{RP}=e-d$	135	150	165	mV
Burst Level Inversion	BF_{RN}	0 0 0 5 5 0 5 0 0 0	⑨ Voltage ; f, $BF_{RN}=f-d$	−165	−150	−135	mV
B-Y							
Voltage Gain	G_{B-Y}	0 0 0 0 0 0 5 0 0 0	$V_{(B-Yin)}=1V_{P-P}$, 1MHz	−0.5	0	0.5	dB
Burst Level Non Inversion	BF_{BP}	0 0 0 0 0 5 5 0 0 0 0 0 0 0 5 5 5 0 0 0	⑦ Voltage ; g, $BF_{BP}=g-h$ ⑦ Voltage ; h, $BF_{BP}=g-h$	135	150	165	mV
Burst Level Inversion	BF_{BN}	0 0 0 5 5 5 5 0 0 0	⑦ Voltage ; i, $BF_{BN}=g-i$	−165	−150	−135	mV

■ NJM2247A ELECTRICAL CHARACTERISTICS (CONTINUED)

(V^+=5V, Ta=25°C)

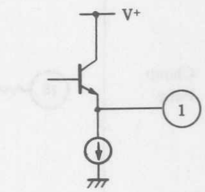
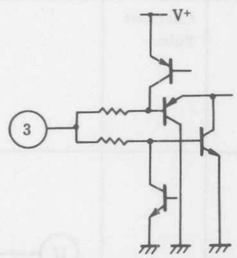
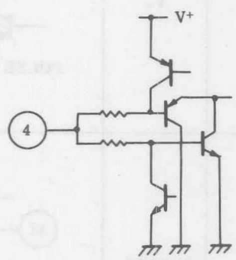
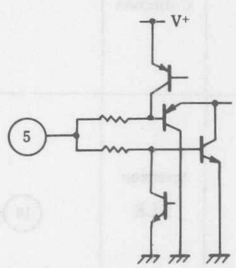
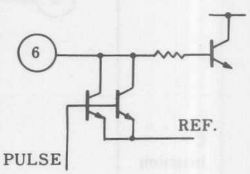
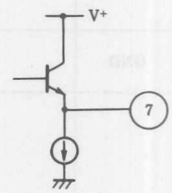
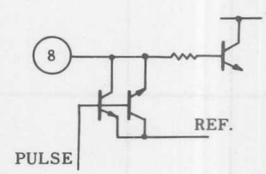
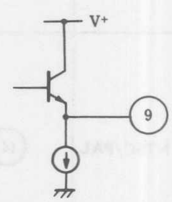
PARAMETERS		SYMBOLS	CONTROL PINS ③④⑤⑩⑫⑭⑮⑯⑲⑳	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Character Output Level 1 C Non Inversion								
White	Y	M_{PWY}	5 5 5 0 0 0 5 5 0 0	① Voltage ; A, $M_{PWY}=A-V_1$	482	530	583	mV
	R−Y	M_{PWR}	5 5 5 0 0 0 5 5 0 0	⑨ Voltage ; B, $M_{PWR}=B-V_9$	−14	0	14	mV
	B−Y	M_{PWB}	5 5 5 0 0 0 5 5 0 0	⑦ Voltage ; C, $M_{PWB}=C-V_7$	−12	0	12	mV
Yellow	Y	M_{PYY}	5 5 0 0 0 0 5 5 0 0	① Voltage ; A, $M_{PYY}=A-V_1$	427	470	517	mV
	R−Y	M_{PYR}	5 5 0 0 0 0 5 5 0 0	⑨ Voltage ; B, $M_{PYR}=B-V_9$	22	42	62	mV
	B−Y	M_{PYB}	5 5 0 0 0 0 5 5 0 0	⑦ Voltage ; C, $M_{PYB}=C-V_7$	−206	−186	−166	mV
Cyan	Y	M_{PCY}	0 5 5 0 0 0 5 5 0 0	① Voltage ; A, $M_{PCY}=A-V_1$	335	370	410	mV
	R−Y	M_{PCR}	0 5 5 0 0 0 5 5 0 0	⑨ Voltage ; B, $M_{PCR}=B-V_9$	−289	−266	−243	mV
	B−Y	M_{PCB}	0 5 5 0 0 0 5 5 0 0	⑦ Voltage ; C, $M_{PCB}=C-V_7$	40	63	87	mV
Green	Y	M_{PGY}	0 5 0 0 0 0 5 5 0 0	① Voltage ; A, $M_{PGY}=A-V_1$	285	313	334	mV
	R−Y	M_{PGR}	0 5 0 0 0 0 5 5 0 0	⑨ Voltage ; B, $M_{PGR}=B-V_9$	−243	−224	−205	mV
	B−Y	M_{PGB}	0 5 0 0 0 0 5 5 0 0	⑦ Voltage ; C, $M_{PGB}=C-V_7$	−145	−123	−105	mV
Magenta	Y	M_{PMY}	5 0 5 0 0 0 5 5 0 0	① Voltage ; A, $M_{PMY}=A-V_1$	198	218	240	mV
	R−Y	M_{PMR}	5 0 5 0 0 0 5 5 0 0	⑨ Voltage ; B, $M_{PMR}=B-V_9$	205	224	243	mV
	B−Y	M_{PMB}	5 0 5 0 0 0 5 5 0 0	⑦ Voltage ; C, $M_{PMB}=C-V_7$	105	123	145	mV
Red	Y	M_{PRY}	5 0 0 0 0 0 5 5 0 0	① Voltage ; A, $M_{PRY}=A-V_1$	145	160	176	mV
	R−Y	M_{PRR}	5 0 0 0 0 0 5 5 0 0	⑨ Voltage ; B, $M_{PRR}=B-V_9$	243	266	289	mV
	B−Y	M_{PRB}	5 0 0 0 0 0 5 5 0 0	⑦ Voltage ; C, $M_{PRB}=C-V_7$	−87	−63	−40	mV
Blue	Y	M_{PBY}	0 0 5 0 0 0 5 5 0 0	① Voltage ; A, $M_{PBY}=A-V_1$	40	58	76	mV
	R−Y	M_{PBR}	0 0 5 0 0 0 5 5 0 0	⑨ Voltage ; B, $M_{PBR}=B-V_9$	−62	−42	−22	mV
	B−Y	M_{PBB}	0 0 5 0 0 0 5 5 0 0	⑦ Voltage ; C, $M_{PBB}=C-V_7$	166	186	206	mV
Black	Y	M_{PPY}	0 0 0 0 0 0 5 5 0 0	① Voltage ; A, $M_{PPY}=A-V_1$	−20	0	20	mV
	R−Y	M_{PPR}	0 0 0 0 0 0 5 5 0 0	⑨ Voltage ; B, $M_{PPR}=B-V_9$	−14	0	14	mV
	B−Y	M_{PPB}	0 0 0 0 0 0 5 5 0 0	⑦ Voltage ; C, $M_{PPB}=C-V_7$	−12	0	12	mV
Character Output Level 2 C Inversion								
White	Y	M_{NWY}	5 5 5 5 0 0 5 5 0 0	① Voltage ; A, $M_{NWY}=A-V_1$	482	530	583	mV
	R−Y	M_{NWR}	5 5 5 5 0 0 5 5 0 0	⑨ Voltage ; B, $M_{NWR}=B-V_9$	−14	0	14	mV
	B−Y	M_{NWB}	5 5 5 5 0 0 5 5 0 0	⑦ Voltage ; C, $M_{NWB}=C-V_7$	−12	0	12	mV
Yellow	Y	M_{NYY}	5 5 0 5 0 0 5 5 0 0	① Voltage ; A, $M_{NYY}=A-V_1$	427	470	517	mV
	R−Y	M_{NYR}	5 5 0 5 0 0 5 5 0 0	⑨ Voltage ; B, $M_{NYR}=B-V_9$	−62	−42	−22	mV
	B−Y	M_{NYB}	5 5 0 5 0 0 5 5 0 0	⑦ Voltage ; C, $M_{NYB}=C-V_7$	166	186	206	mV
Cyan	Y	M_{NCY}	0 5 5 5 0 0 5 5 0 0	① Voltage ; A, $M_{NCY}=A-V_1$	335	370	410	mV
	R−Y	M_{NCR}	0 5 5 5 0 0 5 5 0 0	⑨ Voltage ; B, $M_{NCR}=B-V_9$	243	266	289	mV
	B−Y	M_{NCB}	0 5 5 5 0 0 5 5 0 0	⑦ Voltage ; C, $M_{NCB}=C-V_7$	−87	−63	−40	mV
Green	Y	M_{NGY}	0 5 0 5 0 0 5 5 0 0	① Voltage ; A, $M_{NGY}=A-V_1$	285	313	334	mV
	R−Y	M_{NGR}	0 5 0 5 0 0 5 5 0 0	⑨ Voltage ; B, $M_{NGR}=B-V_9$	205	224	243	mV
	B−Y	M_{NGB}	0 5 0 5 0 0 5 5 0 0	⑦ Voltage ; C, $M_{NGB}=C-V_7$	105	123	145	mV
Magenta	Y	M_{NMY}	5 0 5 5 0 0 5 5 0 0	① Voltage ; A, $M_{NMY}=A-V_1$	198	218	240	mV
	R−Y	M_{NMR}	5 0 5 5 0 0 5 5 0 0	⑨ Voltage ; B, $M_{NMR}=B-V_9$	−243	−224	−205	mV
	B−Y	M_{NMB}	5 0 5 5 0 0 5 5 0 0	⑦ Voltage ; C, $M_{NMB}=C-V_7$	−145	−123	−105	mV
Red	Y	M_{NRY}	5 0 0 5 0 0 5 5 0 0	① Voltage ; A, $M_{NRY}=A-V_1$	145	160	176	mV
	R−Y	M_{NRR}	5 0 0 5 0 0 5 5 0 0	⑨ Voltage ; B, $M_{NRR}=B-V_9$	−289	−266	−243	mV
	B−Y	M_{NRB}	5 0 0 5 0 0 5 5 0 0	⑦ Voltage ; C, $M_{NRB}=C-V_7$	40	63	87	mV
Blue	Y	M_{NBY}	0 0 5 5 0 0 5 5 0 0	① Voltage ; A, $M_{NBY}=A-V_1$	40	58	76	mV
	R−Y	M_{NBR}	0 0 5 5 0 0 5 5 0 0	⑨ Voltage ; B, $M_{NBR}=B-V_9$	22	42	62	mV
	B−Y	M_{NBB}	0 0 5 5 0 0 5 5 0 0	⑦ Voltage ; C, $M_{NBB}=C-V_7$	−206	−186	−166	mV
Black	Y	M_{NPY}	0 0 0 5 0 0 5 5 0 0	① Voltage ; A, $M_{NPY}=A-V_1$	−20	0	20	mV
	R−Y	M_{NPR}	0 0 0 5 0 0 5 5 0 0	⑨ Voltage ; B, $M_{NPR}=B-V_9$	−14	0	14	mV
	B−Y	M_{NPB}	0 0 0 5 0 0 5 5 0 0	⑦ Voltage ; C, $M_{NPB}=C-V_7$	−12	0	12	mV

■ NJM2247B ELECTRICAL CHARACTERISTICS (CONTINUED)

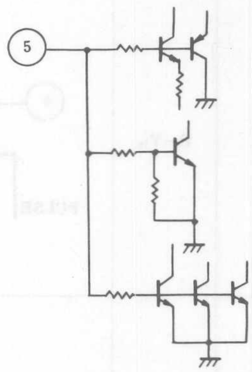
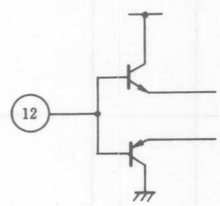
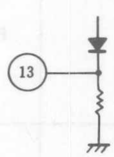
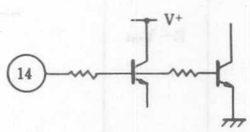
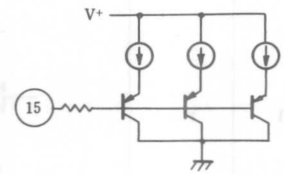
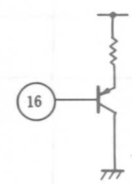
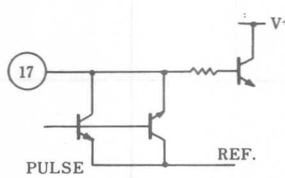
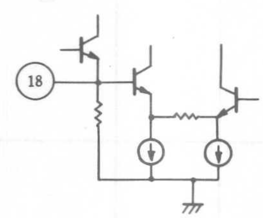
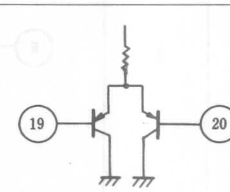
(V^+=5V, Ta=25°)

PARAMETERS		SYMBOLS	CONTROL PINS ③④⑤⑩⑫⑭⑮⑯⑲⑳	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Character Output Level 1								
C Non Inversion								
White	Y	M_{PWY}	5 5 5 0 0 0 5 5 0 0	① Voltage; A, $M_{PWY}=A-V_1$	630	700	770	mV
	R−Y	M_{PWR}	5 5 5 0 0 0 5 5 0 0	⑨ Voltage; B, $M_{PWR}=B-V_9$	−14	0	14	mV
	B−Y	M_{PWB}	5 5 5 0 0 0 5 5 0 0	⑦ Voltage; C, $M_{PWB}=C-V_7$	−12	0	12	mV
Yellow	Y	M_{PYY}	5 5 0 0 0 0 5 5 0 0	① Voltage; A, $M_{PYY}=A-V_1$	472	525	578	mV
	R−Y	M_{PYR}	5 5 0 0 0 0 5 5 0 0	⑨ Voltage; B, $M_{PYR}=B-V_9$	13	33	53	mV
	B−Y	M_{PYB}	5 5 0 0 0 0 5 5 0 0	⑦ Voltage; C, $M_{PYB}=C-V_7$	−165	−146	−127	mV
Cyan	Y	M_{PCY}	0 5 5 0 0 0 5 5 0 0	① Voltage; A, $M_{PCY}=A-V_1$	409	455	501	mV
	R−Y	M_{PCR}	0 5 5 0 0 0 5 5 0 0	⑨ Voltage; B, $M_{PCR}=B-V_9$	−232	−209	−186	mV
	B−Y	M_{PCB}	0 5 5 0 0 0 5 5 0 0	⑦ Voltage; C, $M_{PCB}=C-V_7$	28	50	72	mV
Green	Y	M_{PGY}	0 5 0 0 0 0 5 5 0 0	① Voltage; A, $M_{PGY}=A-V_1$	252	280	308	mV
	R−Y	M_{PGR}	0 5 0 0 0 0 5 5 0 0	⑨ Voltage; B, $M_{PGR}=B-V_9$	−197	−176	−155	mV
	B−Y	M_{PGB}	0 5 0 0 0 0 5 5 0 0	⑦ Voltage; C, $M_{PGB}=C-V_7$	−117	−97	−77	mV
Magenta	Y	M_{PMY}	5 0 5 0 0 0 5 5 0 0	① Voltage; A, $M_{PMY}=A-V_1$	378	420	462	mV
	R−Y	M_{PMR}	5 0 5 0 0 0 5 5 0 0	⑨ Voltage; B, $M_{PMR}=B-V_9$	155	176	197	mV
	B−Y	M_{PMB}	5 0 5 0 0 0 5 5 0 0	⑦ Voltage; C, $M_{PMB}=C-V_7$	77	97	117	mV
Red	Y	M_{PRY}	5 0 0 0 0 0 5 5 0 0	① Voltage; A, $M_{PRY}=A-V_1$	220	245	270	mV
	R−Y	M_{PRR}	5 0 0 0 0 0 5 5 0 0	⑨ Voltage; B, $M_{PRR}=B-V_9$	186	209	232	mV
	B−Y	M_{PRB}	5 0 0 0 0 0 5 5 0 0	⑦ Voltage; C, $M_{PRB}=C-V_7$	−72	−50	−28	mV
Blue	Y	M_{PBY}	0 0 5 0 0 0 5 5 0 0	① Voltage; A, $M_{PBY}=A-V_1$	156	175	194	mV
	R−Y	M_{PBR}	0 0 5 0 0 0 5 5 0 0	⑨ Voltage; B, $M_{PBR}=B-V_9$	−53	−33	−13	mV
	B−Y	M_{PBB}	0 0 5 0 0 0 5 5 0 0	⑦ Voltage; C, $M_{PBB}=C-V_7$	127	146	165	mV
Black	Y	M_{PPY}	0 0 0 0 0 0 5 5 0 0	① Voltage; A, $M_{PPY}=A-V_1$	−20	0	20	mV
	R−Y	M_{PPR}	0 0 0 0 0 0 5 5 0 0	⑨ Voltage; B, $M_{PPR}=B-V_9$	−14	0	14	mV
	B−Y	M_{PPB}	0 0 0 0 0 0 5 5 0 0	⑦ Voltage; C, $M_{PPB}=C-V_7$	−12	0	12	mV
Character Output Level 2								
C Inversion								
White	Y	M_{NWY}	5 5 5 5 0 0 5 5 0 0	① Voltage; A, $M_{NWY}=A-V_1$	630	700	770	mV
	R−Y	M_{NWR}	5 5 5 5 0 0 5 5 0 0	⑨ Voltage; B, $M_{NWR}=B-V_9$	−14	0	14	mV
	B−Y	M_{NWB}	5 5 5 5 0 0 5 5 0 0	⑦ Voltage; C, $M_{NWB}=C-V_7$	−12	0	12	mV
Yellow	Y	M_{NYY}	5 5 0 5 0 0 5 5 0 0	① Voltage; A, $M_{NYY}=A-V_1$	472	525	578	mV
	R−Y	M_{NYR}	5 5 0 5 0 0 5 5 0 0	⑨ Voltage; B, $M_{NYR}=B-V_9$	−53	−33	−13	mV
	B−Y	M_{NYB}	5 5 0 5 0 0 5 5 0 0	⑦ Voltage; C, $M_{NYB}=C-V_7$	127	146	165	mV
Cyan	Y	M_{NCY}	0 5 5 5 0 0 5 5 0 0	① Voltage; A, $M_{NCY}=A-V_1$	409	455	501	mV
	R−Y	M_{NCR}	0 5 5 5 0 0 5 5 0 0	⑨ Voltage; B, $M_{NCR}=B-V_9$	186	209	232	mV
	B−Y	M_{NCB}	0 5 5 5 0 0 5 5 0 0	⑦ Voltage; C, $M_{NCB}=C-V_7$	−72	−50	−28	mV
Green	Y	M_{NGY}	0 5 0 5 0 0 5 5 0 0	① Voltage; A, $M_{NGY}=A-V_1$	252	280	308	mV
	R−Y	M_{NGR}	0 5 0 5 0 0 5 5 0 0	⑨ Voltage; B, $M_{NGR}=B-V_9$	155	176	197	mV
	B−Y	M_{NGB}	0 5 0 5 0 0 5 5 0 0	⑦ Voltage; C, $M_{NGB}=C-V_7$	77	97	117	mV
Magenta	Y	M_{NMY}	5 0 5 5 0 0 5 5 0 0	① Voltage; A, $M_{NMY}=A-V_1$	378	420	462	mV
	R−Y	M_{NMR}	5 0 5 5 0 0 5 5 0 0	⑨ Voltage; B, $M_{NMR}=B-V_9$	−197	−176	−155	mV
	B−Y	M_{NMB}	5 0 5 5 0 0 5 5 0 0	⑦ Voltage; C, $M_{NMB}=C-V_7$	−117	−97	−77	mV
Red	Y	M_{NRY}	5 0 0 5 0 0 5 5 0 0	① Voltage; A, $M_{NRY}=A-V_1$	220	245	270	mV
	R−Y	M_{NRR}	5 0 0 5 0 0 5 5 0 0	⑨ Voltage; B, $M_{NRR}=B-V_9$	−232	−209	−186	mV
	B−Y	M_{NRB}	5 0 0 5 0 0 5 5 0 0	⑦ Voltage; C, $M_{NRB}=C-V_7$	28	50	72	mV
Blue	Y	M_{NBY}	0 0 5 5 0 0 5 5 0 0	① Voltage; A, $M_{NBY}=A-V_1$	156	175	194	mV
	R−Y	M_{NBR}	0 0 5 5 0 0 5 5 0 0	⑨ Voltage; B, $M_{NBR}=B-V_9$	13	33	53	mV
	B−Y	M_{NBB}	0 0 5 5 0 0 5 5 0 0	⑦ Voltage; C, $M_{NBB}=C-V_7$	−165	−146	−127	mV
Black	Y	M_{NPY}	0 0 0 5 0 0 5 5 0 0	① Voltage; A, $M_{NPY}=A-V_1$	−20	0	20	mV
	R−Y	M_{NPR}	0 0 0 5 0 0 5 5 0 0	⑨ Voltage; B, $M_{NPR}=B-V_9$	−14	0	14	mV
	B−Y	M_{NPB}	0 0 0 5 0 0 5 5 0 0	⑦ Voltage; C, $M_{NPB}=C-V_7$	−12	0	12	mV

■ **EQUIVALENT CIRCUIT**

PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	Y_{out}	
2	V^+	—
3	R	
4	G	
5	B	
6	$B-Y_{in}$	
7	$B-Y_{out}$	
8	$R-Y_{in}$	
9	$R-Y_{out}$	

■ EQUIVALENT CIRCUIT

PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT
10	C Inversion	
11	GND	
12	HBF Pulse	
13	BF Level	
14	NTSC/PAL	
15	Clamp Pulse	
16	Character Pulse	
17	Y_{in}	
18	Inversion Set up Correction	
19 20	Y Inversion BLK	

■ INFORMATIONS

Following four points are the outstanding function of the NJM2247A/B. These functions are to go through three input (Y, R-Y, B-Y) signals control by ten control pins.

1. Color Superimpose
   DC level of each equivalent colors shall be supplied to Y, R-Y and B-Y inputs.
2. Burst Flag Insertion
   150 mV burst flag shall be added to R-Y, B-Y input signals.
   Burst flag is selected by the NTSC/PAL switch.
3. C Inversion
   The color phase of the picture shall be inverted for one hundred and eighty degrees. The color phase of the imposed character shall not be altered. This function shall be proceeded when inverting the burst flag, and at the same time, the imposed character level shall be inverted too.
4. Y Inversion
   It is the brightness level inversion. The imposed character color shall not be changed. This function shall be proceeded the switching Y signal output to the inverter side.

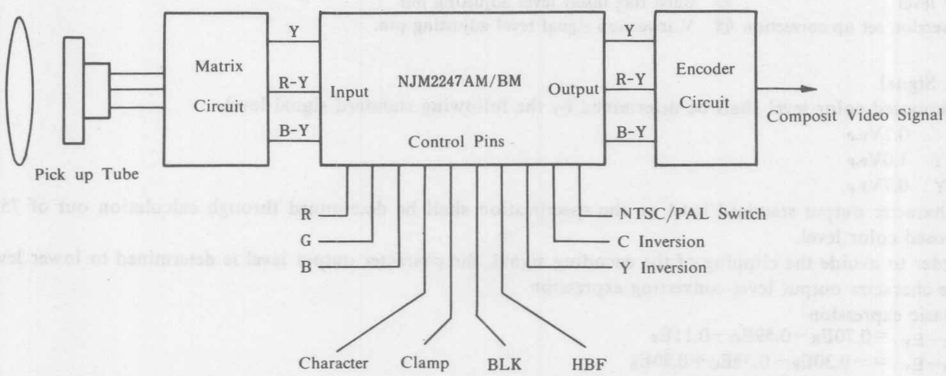


Fig. 1 Video Camera Application

■ APPLICATION NOTES

I/O Explanation

• Supply Voltage	V^+	5V	②
	GND		⑪
• Input Signals	Y	0.7 V_{P-P}	⑰
	R-Y	1.0 V_{P-P}	⑧
	B-Y	0.7 V_{P-P}	⑥
• Output Signals	Y	0.7 V_{P-P}	①
	R-Y	1.0 V_{P-P}	⑨
	B-Y	0.7 V_{P-P}	⑦

■ APPLICATION NOTES

I/O Explanation

- Control Pin Low=0V, HIGH=5V

R③		Superimposed color adjustment
G④		
B⑤		
Clamp Pulse	⑮	Y, R-Y, B-Y signal process pulse input
Character Pulse	⑯	
HBF Pulse	⑫	
BLK Pulse	⑳	
C Inversion	⑩	Color difference, brightness inverting pin
Y Inversion	⑲	
NTS/PAL Switch		

- Adjusting Pin (Normally open → non adjustment)

BF level	⑬	Burst flag insert level adjusting pin.
Inversion set up correction	⑱	Y inversion signal level adjusting pin.

1 Input Signal

Superimposed color level shall be determined by the following standard signal level.

Y	$0.7V_{P\text{-}P}$
R-Y	$1.0V_{P\text{-}P}$
B-Y	$0.7V_{P\text{-}P}$

The character output standard level on the specification shall be determined through calculation out of 75 % of superimposed color level.

(In order to avoide the clipping of the encoding signal, the character output level is determined to lower level)

- The character output level converting expression

The basic expression

$$E_R-E_Y=0.70E_R-0.59E_G-0.11E_B$$
$$E_B-E_Y=-0.30E_R-0.59E_G+0.89E_B$$
$$E_Y=0.30E_R+0.59E_G+0.11E_B$$

From standard level and practical input level, each color signal level imposed in R-Y, B-Y and Y signals are as in the following.

$$V_{R\text{-}Y}=0.75\times1[V_{P\text{-}P}]\times E_{R\text{-}Y}/1.4$$
$$=0.375E_R-0.316E_G-0.059E_B$$
$$V_{B\text{-}Y}=0.75\times0.7[V_{P\text{-}P}]\times E_{B\text{-}Y}/1.78$$
$$=-0.088E_R-0.174E_G+0.263E_B$$
$$V_Y=0.158E_R+0.310E_G+0.058E_B$$

(E_R, E_G, E_B は, LOW 0, HIGH 1)

2. Clamp Pulse

During the interval of blanking, input the pulse through clamp pulse pin ⑳ the blanking level (0 level) of input signal (Y, R-Y, B-Y) is to be fixed at the bias point within the IC.

Note) The pulse width of clamp pulse shall be set more than A version 6 μs and B version 3 μs. (see figure 2)

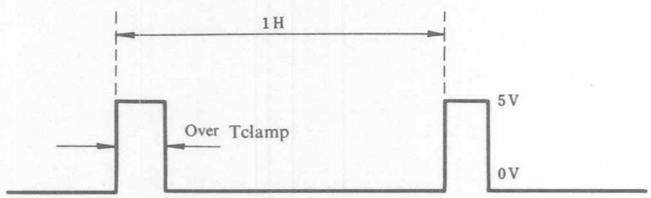


Fig. 2 Clamp Pulse Width

3. Character Color Adjustment

Superimposed color adjustment of the character can be determined in eight different colors, by choosing R, G, B input levels.

(LOW 0V, HIGH 5V)

R	G	B	COLOR
5	5	5	White
5	5	0	Yellow
0	5	5	Cyan
0	5	0	Green
5	0	5	Magenta
5	0	0	Red
0	0	5	blue
0	0	0	Black

Character Color Selecting Code

4. Character Insertion

Pulse informations from outside character generater shall be given input at the character pulse pin ⑯. During the period of pulse process, the selected color level shall be inserted into each Y, R-Y, B-Y.

5. Burst Flag Insertion

Inputting burst period pulse at the HBF pin ⑫, the burst flag (150mV) can be inserted in the B-Y, R-Y signals. At the same time, by putting NTSC/PAL switch ⑭, the burst flag can be altered to NTSC or PAL system.

	NTSC/PAL SWITCH⑭	
	LOW 0V (PAL)	HIGH 5V (NTSC)
R-Y Signal	+150mV	non insertion
B-Y Signal	−150mV	−150mV

Burst Flag Inserting

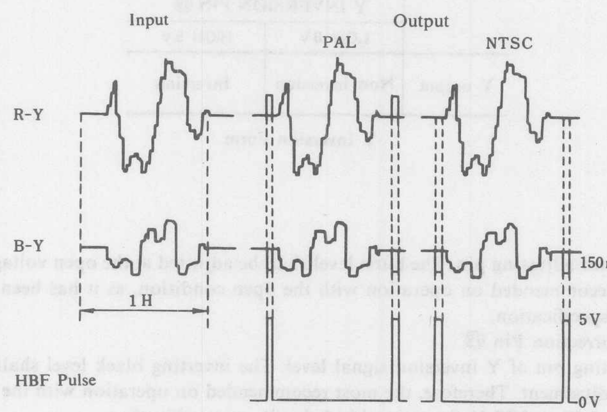


Fig.3 Burst Flag Inserting Example

6. C Inversion

The color phase of the picture shall be inverted for one hundred and eighty degrees setting C inversion pin ⑩. It is applied that the reference signal (burst flag) shall be inverted into one hundred and eighty degrees at the time of de-coding.

Superimposed character color do not change at the picture inversion.

	C INVERSION PIN ⑩	
	LOW 0 V	HIGH 5 V
Burst	Non Inversion	Inversion

C Inversion Form

7. Y Inversion

The brightness of the picture shall be inverted by setting Y inversion pin ⑲. It is that Y signal shall be inverted by the inverter, and then blanking period signal shall be adjusted to the black level with blanking pulse.

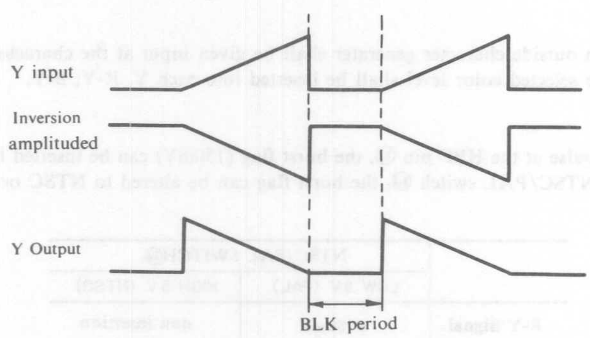


Figure 4. Y Inversion Output Example

	Y INVERSION PIN ⑲	
	LOW 0 V	HIGH 5 V
Y output	Non inversion	Inversion

Y Inversion Form

8. Adjusting pin

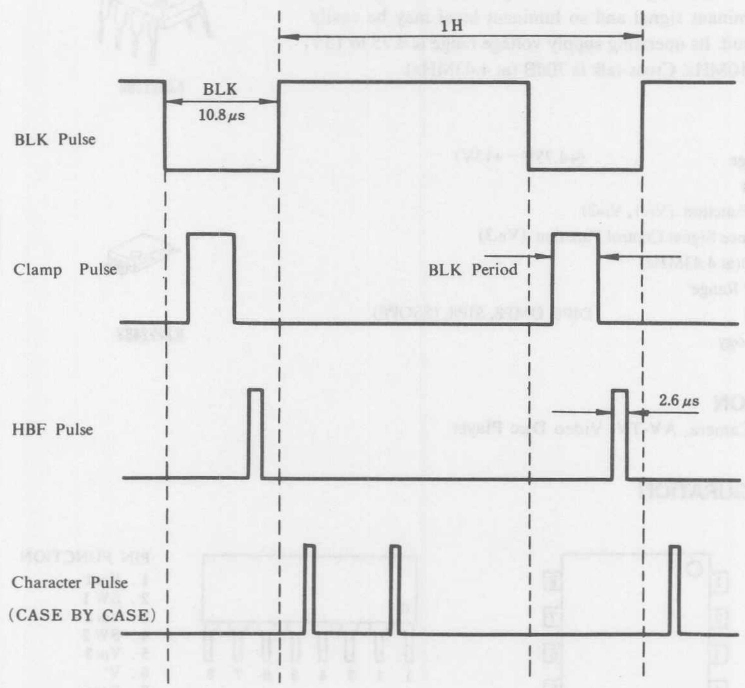
(1) BF Level Pin ⑬

It is the burst flag minor adjusting pin. The burst level shall be adjusted at the open voltage, 0.3V level adjustment. Therefore, the most recommended on operation with the open condition, as it has been controlled at 135 to 165 mV (burst level) on specification.

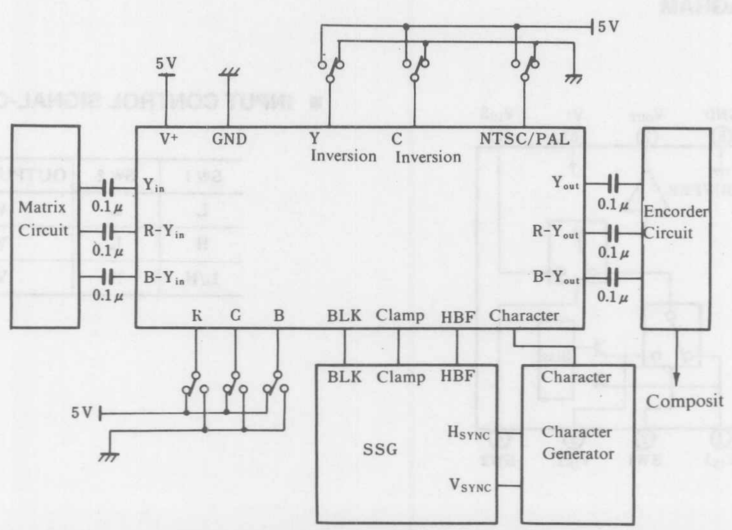
(2) Inversion Set Up Correction Pin ⑱

It is the minor adjusting pin of Y inversion signal level. The inverting black level shall be adjusted at the open voltage, 1.8 V level adjustment. Therefore, the most recommended on operation with the open condition, as it has been controlled with 0.59 to 0.77 V (inverting black level) on specification.

9. Pulse Timing
The pulse input timing should be proceeded as in the following.



■ TYPICAL APPLICATION

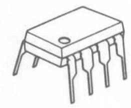


3-INPUT VIDEO SUPER IMPOSER

■ GENERAL DESCRIPTION

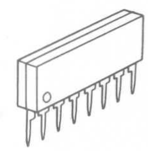
The NJM2248 is 3-input video switch for video and audio signal. Two input terminals have sink-chip clamp function and so it is applied to fixed DC level of video sighal. The other input terminal is transistor base input for luminant signal and so luminant level may be easily fixed by outer circuit. Its operating supply voltage range is 4.75 to 13V and bandwidth is 10MHz. Cross-talk is 70dB (at 4.43MHz).

■ PACKAGE OUTLINE


NJM2248D


NJM2248M


NJM2248V


NJM2248L

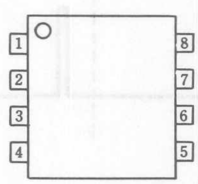
■ FEATURES

- Operating Voltage (+4.75V～+13V)
- 3 Input-1 Output
- Internal Clamp Function ($V_{IN}1$, $V_{IN}2$)
- Internal Luminance Signal Control Function ($V_{IN}3$)
- Cross-talk 70dB(at 4.43MHz)
- Wide Frequency Range
- Package Outline DIP8, DMP8, SIP8, (SSOP8)
- Bipolar Technology

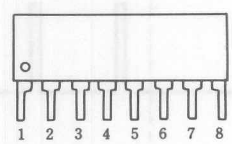
■ APPLICATION

- VCR, Video Camera, AV-TV, Video Disc Player

■ PIN CONFIGURATION



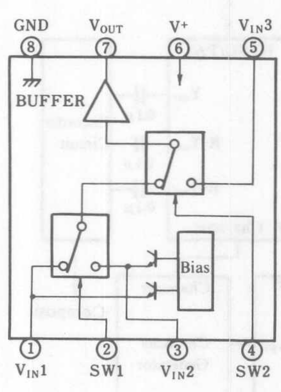
NJM2248D
NJM2248M
NJM2248V



NJM2248L

PIN FUNCTION
1. $V_{IN}1$
2. SW 1
3. $V_{IN}2$
4. SW 2
5. $V_{IN}3$
6. V^+
7. V_{OUT}
8. GND

■ BLOCK DIAGRAM



■ INPUT CONTROL SIGNAL-OUTPUT SIGNAL

SW 1	SW 2	OUTPUT SIGNAL
L	L	$V_{IN}1$
H	L	$V_{IN}2$
L/H	H	$V_{IN}3$

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(SSOP8) 250	mW
		(SIP8) 800	mW
Operating Temperature Range	T_{opr}	−20~+75	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETERS	SYMBOLS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage	V^+		4.75	—	13.0	V
Operating Current	I_{CC}	S1=S2=S3=S4=S5=1	—	10.5	14.0	mA
Voltage Gain	G_V	V_I=2.5V_{P-P},100kHz, V_O/V_I	−0.5	—	+0.5	dB
Frequency Characteristics	G_f	V_I=2.0V_{P-P}, V_O(10MHz)/V_O(100kHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_I=2V_{P-P}, Staircase Signal	—	0	—	%
Differential Phase	DP	V_I=2V_{P-P}, Staircase Signal	—	0	—	deg
Cross-talk	CT	V_I=2.0V_{P-P}, 4.43MHz, V_O/V_I (note 1)	—	−70	—	dB
Switch Change Voltage	V_{CH}	All inside SW: ON	2.4	—	—	V
	V_{CL}	All inside SW: OFF	—	—	0.8	V
Output Impedance	R_O		—	10	—	Ω

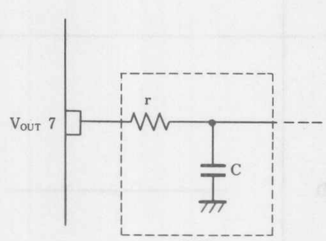
(Note 1) : Tested on all combination except three below.
a) S1=2, S4=S5=1 b) S2=2, S4=2, S5=1 C) S3=2, S5=2

(Note 2) : Unless specified, tested with V_{BIAS}=3V.

(Note 3) : If it is not shown about switch condition, it is tested on three condtion below.
a) S1=2, S2=S3=S4=S5=1 b) S1=1, S2=2, S3=1, S4=2, S5=1 c) S1=S2=1, S3=2, S4=1 or 2, S5=2

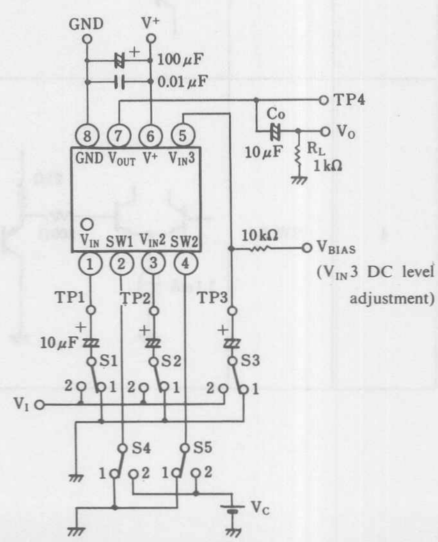
(Note 4) : Clamp voltage of Vin1 and Vin2 is about 2/5 of supply voltage (about 2.0V if V^+=5V).

■ SPECIAL CARES TO BE TAKEN WHEN APPLICATION

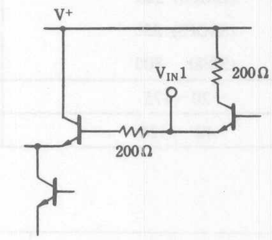
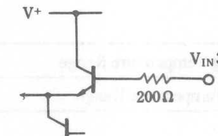
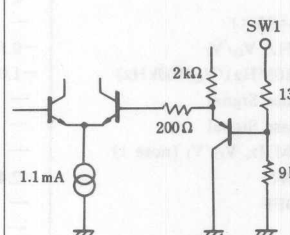
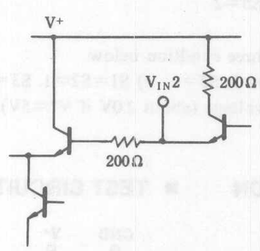
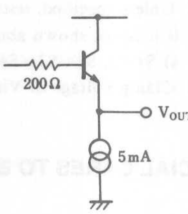
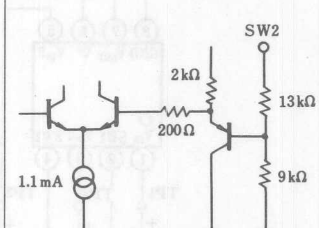


r ≅100Ω
C ≅20pF

■ TEST CIRCUIT



■ TERMINAL FUNCTION

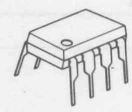
PIN NO.	PIN SYMBOL	EQUIVALENT CIRCUIT	PIN NO.	PIN SYMBOL	EQUIVALENT CIRCUIT
1	V_{IN} 1		5	V_{IN} 3	
2	SW 1		6	V+	
3	V_{IN} 2		7	V_{OUT}	
4	SW 2		8	GND	

3-INPUT VIDEO SWITCH

■ GENERAL DESCRIPTION

The NJM2249 is 3-input video switch for video and audio signal. One input terminals has sink-chip clamp function and so it is applied to fixed DC level of video sighal. Two other input terminals are transistor base input for luminant signal and so luminant level may be easily fixed by outer circuit. Its operating supply voltage range is 4.75 to 13V and bandwidth is 10MHz. Cross-talk is 70dB (at 4.43MHz).

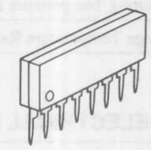
■ PACKAGE OUTLINE



NJM2249D

NJM2249M

NJM2249V



NJM2249L

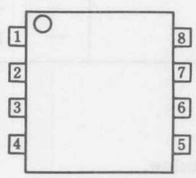
■ FEATURES

- Operating Voltage (V^{+}=+4.75V～+13V)
- 3 Input-1 Output
- Internal Clamp Function ($V_{IN}1$)
- Internal Luminance Signal Control Function ($V_{IN}2$, $V_{IN}3$)
- Cross-talk 70dB(at 4.43MHz)
- Wide Frequency Range
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

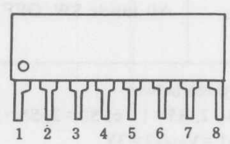
■ APPLICATION

- VCR, Video Camera, AV-TV, Video Disc Player

■ PIN CONFIGURATION



NJM2249D
NJM2249M
NJM2249V

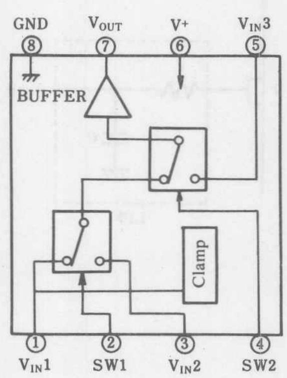


NJM2249L

PIN FUNCTION

1. $V_{IN}1$
2. SW1
3. $V_{IN}2$
4. SW2
5. $V_{IN}3$
6. V^{+}
7. V_{OUT}
8. GND

■ BLOCK DIAGRAM



■ INPUT CONTROL SIGNAL-OUTPUT SIGNAL

SW 1	SW 2	OUTPUT SIGNAL
L	L	$V_{IN}1$
H	L	$V_{IN}2$
L/H	H	$V_{IN}3$

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DIP8) 500 (DMP8) 300 (SSOP8) 250 (SIP8) 800	mW mW mW mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETERS	SYMBOLS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage	V^+		4.75	—	13.0	V
Operating Current	I_{CC}	S1=S2=S3=S4=S5=1	—	10.5	13.0	mA
Voltage Gain	G_v	V_I=2.5V_{P-P}, 100kHz, V_O/V_I	−0.5	—	+0.5	dB
Fequency Characteristics	G_f	V_I=2.0V_{P-P}, V_O(10MHz)/V_O(100kHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_I=2V_{P-P}, Staircase Signal	—	0	—	%
Differential Phase	DP	V_I=2V_{P-P}, Staircase Signal	—	0	—	deg
Cross-talk	CT	V_I=2.0V_{P-P}, 4.43MHz, V_O/V_I(note 1)	—	−70	—	dB
Switch Change Voltage	V_{CH}	All inside SW: ON	2.4	—	—	V
	V_{CL}	All inside SW: OFF	—	—	0.8	V
Output Impedance	R_O		—	10	—	Ω

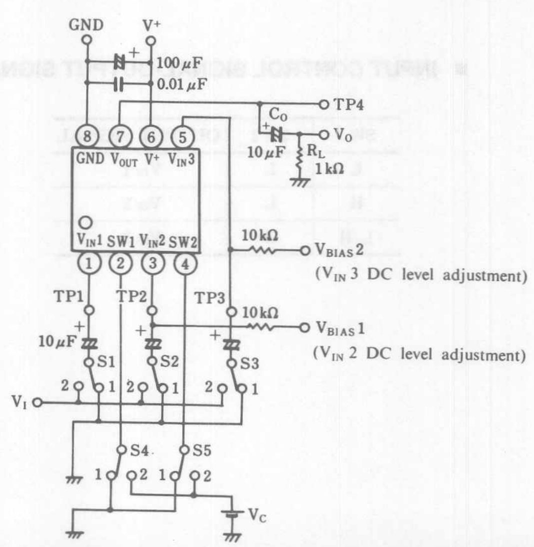
(Note 1): Tested on all combination except three below.
a) S1=2, S4=S5=1 b) S2=2, S4=2, S5=1 c) S3=2, S5=2

(Note2): Unless specified, tested with $V_{BIAS}1=V_{BIAS}2$=3V.

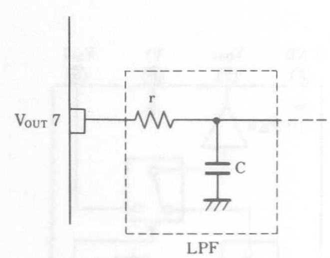
(Note 3): If it is not shown about switch condition, it is tested on three condition below.
a) S1=2, S2=S3=S4=S5=1 b) S1=1, S2=2, S3=1, S4=2, S5=1 c) S1=S2=1, S3=2, S4=1 or 2,S5=2

(Note 4): $V_{IN}1$ clamp voltage is about 2/5 of supply voltage (about 2.0V if V^+=5V).

■ TEST CIRCUIT

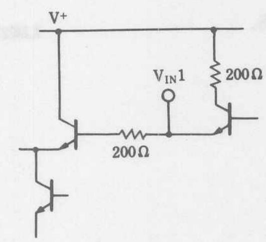
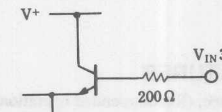
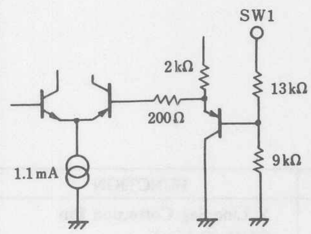
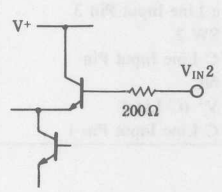
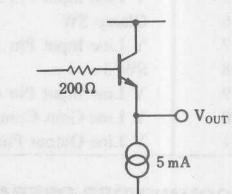
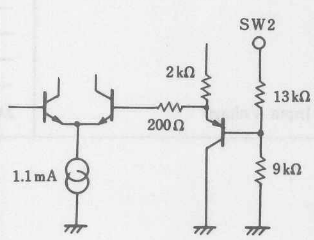


■ SPECIAL CARES TO BE TAKEN WHEN APPLICATION



r≅100Ω
C≅20pF

■ TERMINAL FUNCTION

PIN NO.	PIN SYMBOL	EQUIVALENT CIRCUIT	PIN NO.	PIN SYMBOL	EQUIVALENT CIRCUIT
1	V_{IN} 1		5	V_{IN} 3	
2	SW 1		6	V⁺	
3	V_{IN} 2		7	V_{OUT}	
4	SW 2		8	GND	

ON SCREEN DISPLAY MIX IC

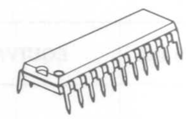
■ GENERAL DESCRIPTION

NJM2252 is the IC that has been developed for VCR application, which has the super-impose function as well as the function to drive the S-VHS, S-output pin by putting the extemal transistor.

NJM2252 has Y signal pin and C singal pin of each independent circuit in it. Y signal line is selectable of 4 inputs, and C signal line is selectable of 3 inpots, each by the inside switches.

Further more, it has function to adjust the output level of S-VHS, Spin.

■ PACKAGE OUTLINE



NJM2252L

■ FEATURES

- 9V spec, (Recommended operational voltage range 8.6~9.4V)
- Voltage gain can be controlled by the external resistor (Typ. ±3dB)
- Wide band (Y signal line 10MHz, C signal line 8MHz)
- Output sag. correction circuit incorporated (Y signal line)
- Video switch incorporated (Y signal line 4 input, C signal line 3 input)
- Clamp circuit (Y signal line) Bias circuit (C signal line) incorporated
- Package Outline SDIP20
- Bipolar Technology

■ APPLICATION

- VCR (Correspond to S-VHS)
- Laser Disc

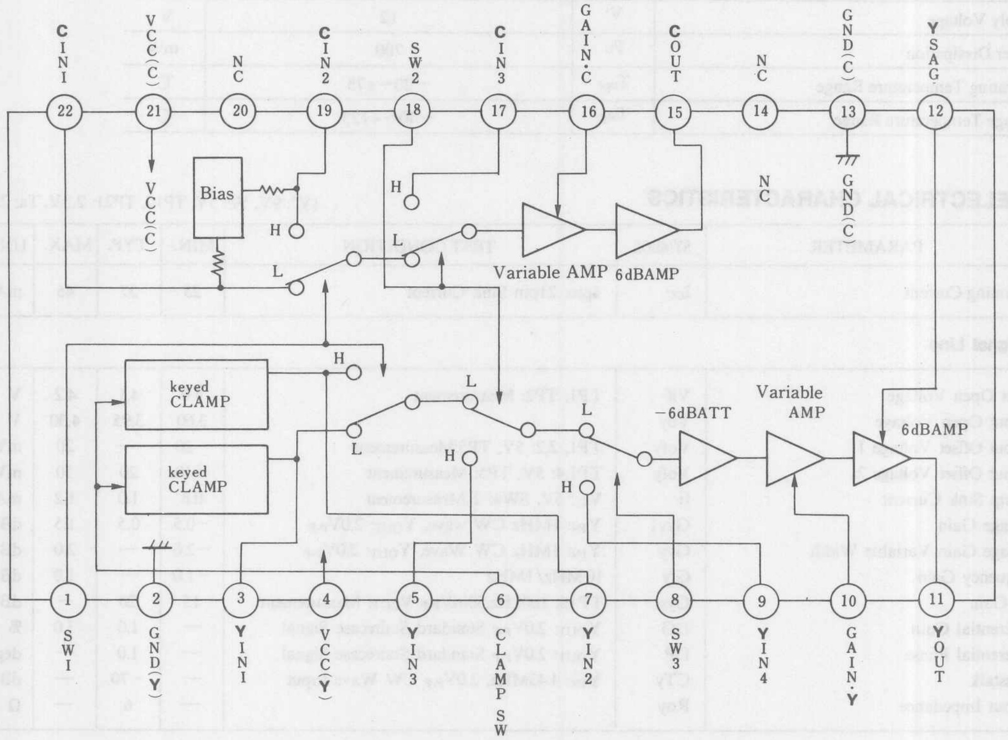
■ PIN FUNCTION

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	SW1	12	Y Line Sag Correction Pin
2	GND (Y Line)	13	GND (C Line)
3	Y Line Input Pin	14	NC
4	V+ (L Line)	15	C Line Output Pin
5	Y Line Input Pin 3	16	c Line Gain Control
6	Clamp SW	17	c Line Input Pin 3
7	Y Line Input Pin	18	SW 2
8	SW 3	19	C Line Input Pin
9	Y Line Input Pin 4	20	NC
10	Y Line Gain Control	21	V+ (C Line)
11	Y Line Output Pin	22	C Line Input Pin 1

■ RECOMMENDED OPERATING CONDITION

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Supply Voltage Range	V^+		8.6	9.0	9.4	V
Y Signal Input Amlitude Range		Y_{IN}	—	—	3.0	V_{P-P}
Y Signal Output Amplitude Range		Y_{OUT}	—	—	3.0	V_{P-P}
C Signal Input Amplitude Range		C_{IN}	—	—	2.0	V_{P-P}
C Signal Output Amplitude Range		C_{OUT}	—	—	2.5	V_{P-P}
Gain Control Voltage Range		TP10, TP21 Input Voltage	2.0	—	3.0	V

■ BLOCK DIAGRAM



NJM2252L

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

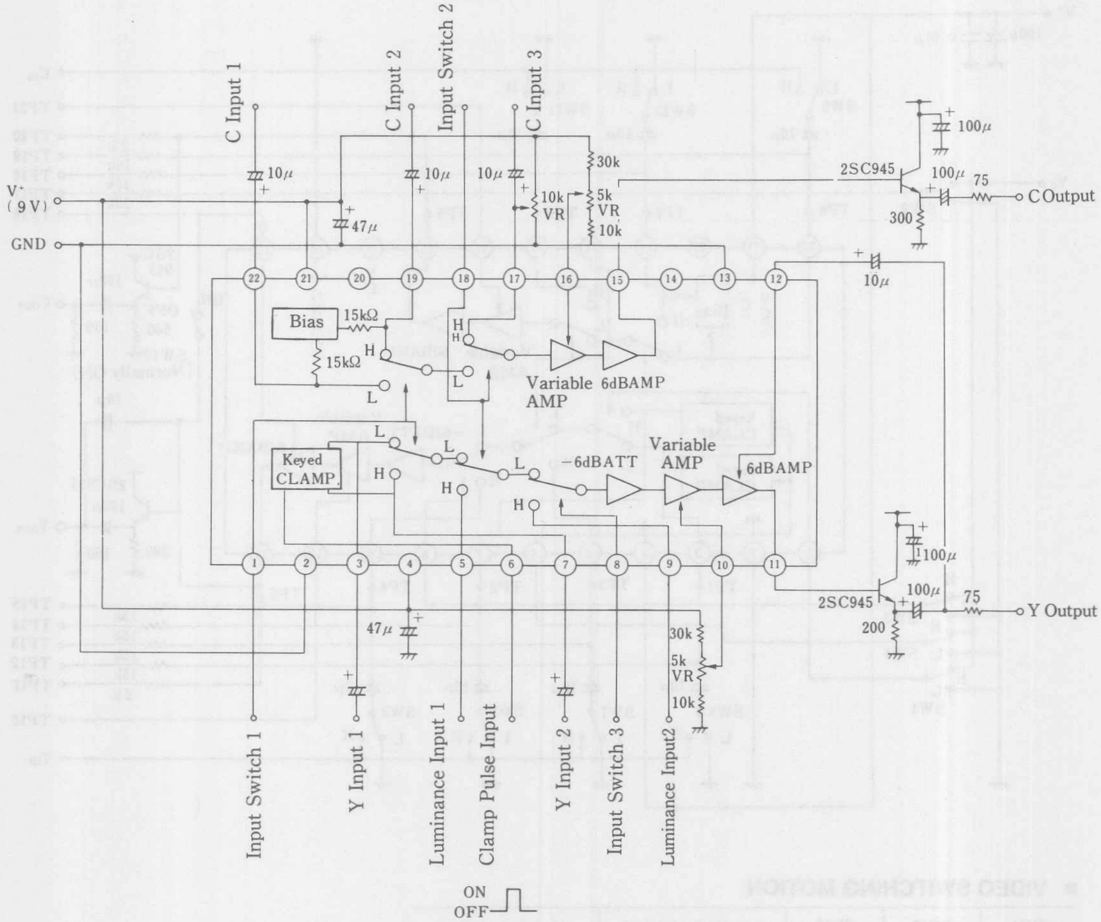
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	12	V
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	−20~+75	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

■ ELECTRICAL CHARACTERISTICS

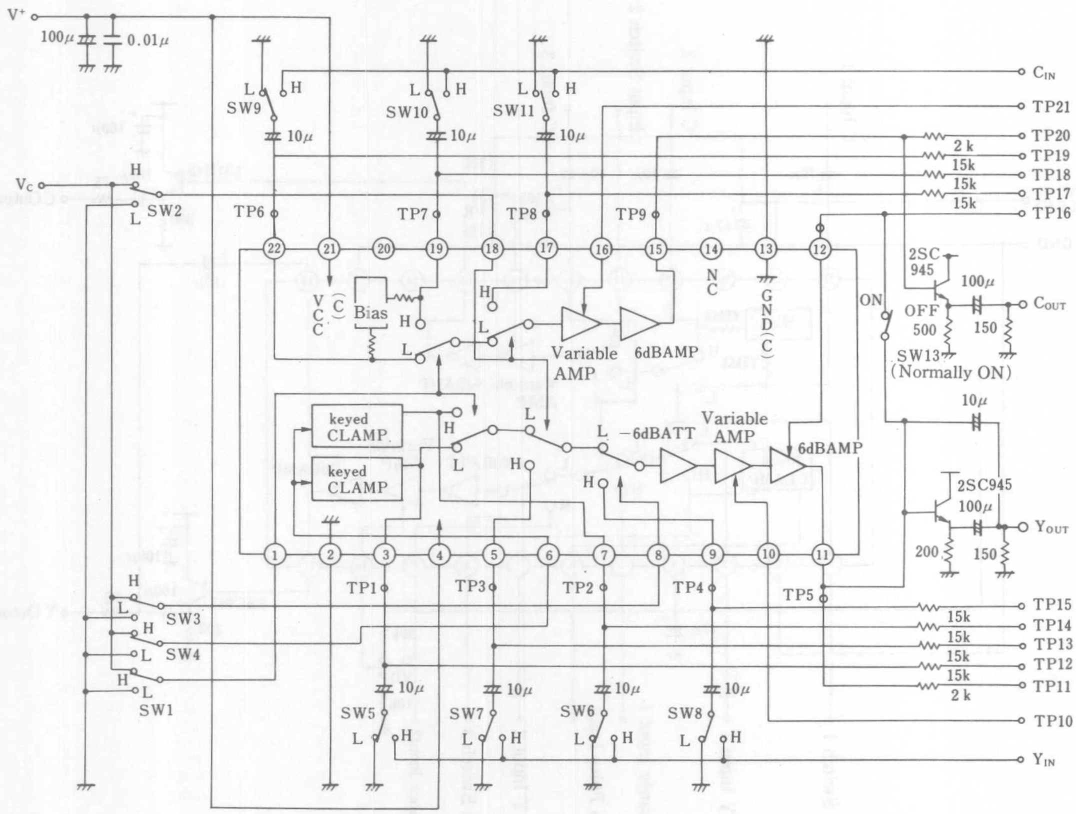
(V^+: 9V, V_C: 5V, TP10, TP21: 2.5V, Ta: 25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	4pin, 21pin Sink Current	25	37	45	mA
Y Signal Line						
Input Open Voltage	Vif	TP1, TP2: Measurement	4.0	4.1	4.2	V
Output Open Voltage	Voy		3.60	3.95	4.30	V
Output Offset Voltage 1	Vofy	TP1, 2,2: 5V, TP5:Measurement	−20	—	20	mV
Output Offset Voltage 2	Vofy	TP1,4: 5V, TP5: Measurement	−10	20	50	mV
Clamp Sink Current	Ii	V_C: 5V, SW4: 2 Measurement	0.8	1.0	1.2	mA
Voltage Gain	Gvy1	Y_{IN}: 1MHz CW wave, Y_{OUT}: 2.0V_{P-P}	−0.5	0.5	1.5	dB
Voltage Gain Variable Width	Gvy	Y_{IN}: 1MHz CW Wave, Y_{OUT}: 2.0V_{P-P}	−2.0	—	2.0	dB
Frequency Gain	Gfy	10MHz/1MHz	−1.0	—	1.0	dB
Sag Gain	Gys	TP16: 100kHz,50mV_{P-P} V_{OUT}: Measurement	15	20	—	dB
Differential Gain	DG	Y_{OUT}: 2.0V_{P-P} Standard Staircase Signal	—	1.0	3.0	%
Differential Phase	DP	Y_{OUT}: 2.0V_{P-P} Standard Staircase Signal	—	1.0	—	deg
Crosstalk	CTy	Y_{IN}: 4.43MHz, 2.0V_{P-P} CW Wave Input	—	−70	—	dB
Output Impedance	Roy		—	6	—	Ω
C Signal Line						
Input Open Voltage	Vic	TP6, TP7: Measurement	3.9	4.1	4.3	V
Output Open Voltage	Voc	TP21: 2.5V	5.05	5.35	5.65	V
Output Offset Voltage	Vofc	TP6, 7, 8: 5.0V, TP9: Measurement	−50	—	50	mV
Voltage Gain	Gvc1	C_{IN}: 1MHz CW Wave, C_{OUT}: 2V_{P-P}	6.0	7.0	8.0	dB
Voltage Gain Variable Width	Gvc	C_{IN}: 1MHz CW Wave, C_{OUT}: 2V_{P-P}	4.5	—	8.5	dB
Frequency Gain	Gfc	8MHz/1MHz	−1.0	—	1.0	dB
Crosstalk	Ctc	C_{IN}: 4.43MHz, 1.0V_{P-P} CW Wave Input	—	−70	—	dB
Input Impedance	Ric	19pin, 22pin Input Impedance	11	15	19	Ω
Output Impedance	Roc		—	6	—	Ω
Common Line						
Control On Voltage	Vc1	Inner Switch on Level Guarantee	2.5	—	—	V
Control Off Voltage	Vc2	Inner Switch Off Level Guarantee	—	—	1.5	V
Key Clamp Control Voltage	Vc3	1 Pin Threshold Voltage	1.5	2.0	2.5	V

■ APPLICATION CIRCUIT



■ TEST CIRCUIT



■ VIDEO SWITCHING MOTION

SW1	SW2	SW3	Y LINE OUTPUT	C LINE OUTPUT
L	L	L	Yin1	Cin1
H	L	L	Yin2	Cin2
*	H	L	Yin3	Cin3
L	L			Cin1
H	L	H	Yin4	Cin2
*	H			Cin3

*:H or L

■ TERMINAL FUNCTION

PIN	PIN NAME	SYMBOL	FUNCTION
1	SW1	SW1	Video switch channel change over input. The L level is identified to be input when being left on at open state.
2	GND (Y Line)	GND Y	
3	Y Line Input Pin	Yin1	Video signal input pin (Y line) Key Clamp circuit internalized. The clamp function goes on when the key clamp is on H timing. Kyed clamp at L position indicates the normal sink chip clamp on operatior. The clamp voltage is about 4.1V.
4	V_{CC} (Y Line)		Y line alone can not be used when C line supply voltage is off state.
5	Y Line Input Pin 3	Yin 3	Video signal input pin (Y line) The IC does not have bias or clamp function circuit in it, and its easy to have the external circuit, of the brightness level setting. It is most suitable for superinpose input.
6	Clamp Switch	Yin3	In case of L level, the sink chip clamp, Yin1, Yin2 on operation. In case of H level, Yin1, Yin2 become the clamp voltage compulsory. If the kye clamp function is not used, apply it with the L level on fixed condition.
7	Y Line Input Pin 2	Yin2	Video signal input pin (Y line) Key clamp circuit internalized. The clamp function goes on when the key clamp is on H timing. Keyed clamp at L position indicates the normal sink chip clamp on operatior. The clamp voltage is about 4.1V.
8	SW3	SW3	Video switch channel change over input. The L level is identified to be input when being left on open state.
9	Y Line Input Pin 4	Yin4	Video signal input pin (Y line) The IC does not have bias or clamp function circuit in it, and its easy to have the external circuit of the brightness level setting. It is most suitable for superimpose input.
10	Y Line Gain Control	GAIN Y	Y Line voltage gain can be adjusted when input of 2.0~3.0V. 2.0V input, at gain min. (−3.0dB) 3.0V input at gin max. (+3.0dB) In order to set the gain within the IC, the gain control circuit compares the voltage (Typ 2.5V), the one which was decided by the resistance the voltage (Typ 2.5V), the one which was decided by the resistance division, and the gain control pin voltage, and then it is advisable to apply voltage on the gain control pin after the process of the resistance division of the supply voltage.
11	Y Line Output Pin	Yout	Its the Y line video signal output pin. It can drive 75Ω line when connecting 25C945 & 2SC1815 directly. No sag output can be performed by applying Y line sag correction at 12 pin.
12	Y Line Sag Correcting Pin	Y SAGU	In case when applying as 75Ω driver by connecting 2SC945 to Yout, the sag can be generated by output coupling capacitance and load resistance. The output included the sag, when once again, being input at sag correctinn pin through coupling capacitance, and it can be done to take out the output from Y out in which that there is no sag at all. In case when the sag correction function is not required on operation, it is advisable to use it by connecting 11 pin directly.

■ TERMINAL FUNCTION

PIN	PIN NAME	SYMBOL	FUNCTION
13	GND (C Line)	GND C	
14	NC		
15	CLine Output Pin	Cout	It's the C line video signal output pin. It can drive 75Ω line when connecting 2SC945 & 2SC1815 directly.
16	C line Output Pin	GAIN C	C line voltage gain can be adjusted when input 2.0~3.0V. 2.0V input at gain min. (+3.0dB) 3.0V input at gain max. (+9.0dB) In order to set the gain within the IC, the gain control circuit compares the voltage (Typ 2.5V), the one which was decided by the resistance division, and the gain control pin voltage, and then it is advisable to apply voltage on the gain control pin, after the process of resistance division of the supply voltage.
17	C Line Input Pin 3	Cin3	Video signal input pin (C line) The IC does not have bias or clamp function circuit in it, and it's easy to set the brightness level with the external circuit. It is most suitable for superimpose input.
18	SW2	SW2	The L level is identified to be input when being left on open state.
19	C Line Input Pin 2	Cin2	Video signal input pin (C line) The bias voltage is about 4.1V, and the input impedance is about 15KΩ
20	NC		
21	V+ (C Line)	V+ C	C line alone can not be used while the Y line supply voltage is off state.
22	C Line Input Pin 1	Cin1	C line Input Pin 1. Video signal input pin (C line) Bias voltage is about 4.1V, input impedance is about 15KΩ

■ TEST CONDITION

(V^+: 9V, V_C : 5V, TP10, TP21: 2.5V, Ta: 25℃)

PARAMETER	SYMBOL	1	2	3	4	5	6	7	8	9	0	1	TEST CONDITION
Supply Current	I_{CC}	L	L	L	L	L	L	L	L	L	L	L	4pin, 21pin Total Current
Y Signal Line													
Input Open Voltage	V_{iy}	L H	L L	L L	L L	L L	L L	L L	L L	L L	L L	L L	Type1: Measurement TP2: Measurement
Output Open Voltage	Voy	L	L	L	L	L	L	L	L	L	L	L	TP5: Measurement
Output Offset Voltage 1	Vofy	L H L	L L H	L L L	L L L	L L L	L L L	L L L	L L L	L L L	L L L	L	TP1, 2, 3: 5V TP5: Measurement→V1 V2→ V3→ Vofy=V2−V1 Vofy=V=−V2 } Judgment Vofy=V3−V2
Output offset Voltage 2	Vofy	L L	L L	L H	L L	L L	L L	L L	L L	L L	L L	L L	tp1, 4: 5v tp5: MeasurementV1→ V4→ Vofy=V4−V1 Judgment
Clamp Sink Current	Ii	L L	L L	H H	L L	L L	L L	L L	L L	L L	L L	L L	③ pin Sink Current ⑦ pin Sink Current
Voltage Gain Width	Gvy1	L H L L	L L H L	L L L H	L L L L	H L L L	L H L L	L L H L	L L L H	L L L L	L L L L	L L L L	At left four switch conditions Tp10: 2.5V voltage gain→Gv1 TP10: 2.0V voltage gain→Gv2 TP10: 3.0V voltage gain→Gv3 Gvy=GV2−Gv1 } Judgment Gvy=Gv3−Gv1
Frequency Gain	Gfy	L H L L	L L H L	L L L H	L L L L	H L L L	L H L L	L L H L	L L L H	L LL L L	L L L L	L L L L	At left four switch Y_{IN}1MHz voltage gain→Gv4 Y_{IN} 10MHz voltage gain→Gv5 Gfy=gV5−Gv4 Judgment
Sag Gain	Gys	L	L	L	L	L	L	L	L	L	L	L	SW13: OFF TP16: 100kHz, 50mV_{P-P} input Y_{OUT}:Measurement Y_{OUT}/50mV_{PP} Judgment
Differential Gain	DG	L H L L	L L H L	L L L H	L L L L	H L L L	L H L L	L L H L	L L L H	L L L L	L L L L	L L L L	Y_{out}: 2.0v_{P-P}Standard Staircase Signal Judgment at left four switch conditions
Differential Phase	DP	L H L L	L L H L	L L L H	LH L L L	L L L L	L H L L	L L H L	L L L H	L L L L	L L L L	L L L L	Y_{OUT}: 2.0V_{P-P} Standard Staircase Signal Judgment at left four switch conditions

■ TEST CONDITION

(V^+: 9V, V_C : 5V, TP10, TP21: 2.5V, Ta: 25℃)

PARAMETER	SYMBOL	1	2	3	4	5	6	7	8	9	0	1	TEST CONDITION
Crostalk	CTy	H	L	L	L	H	L	L	L	L	L	L	Judgment by left 12 switch conditions
		L	H	L	L	H	L	L	L	L	L	L	Y_{IN}: 4.43MHz, 2.0$V_{P\text{-}P}$ CW wave input
		L	H	L	L	H	L	L	L	L	L	L	Y_{OUT}Measurement
		L	L	L	L	L	H	L	L	L	L	L	Y_{out}/y_{IN} Judgment
		H	L	L	L	H	L	L	L	L	L	L	
		L	L	H	L	L	H	L	L	L	L	L	
		L	L	L	L	L	L	H	L	L	L	L	
		H	L	L	L	L	L	H	L	L	L	L	
		L	L	H	L	L	L	H	L	L	L	L	
		L	L	L	L	L	L	L	H	L	L	L	
		H	L	L	L	L	L	L	H	L	L	L	
		L	H	L	L	L	L	L	H	L	L	L	
Output Impedance	Roy	L	L	L	L	H	L	L	L	L	L	L	
C Signal Line													
Input Open Voltage	Vic	L	L	L	L	L	L	L	L	L	L	L	TP6: Measurement
		H	L	L	L	L	L	L	L	L	L	L	TP7: Measurement
Output Open Voltage	Voc	L	L	L	L	L	L	L	L	L	L	L	TP9: Measurement
Output Offset Voltage	Vofc	L	L	L	L	L	L	L	L	L	L	L	TP6, 7,8: 5.0V, TP9: Measurement→V1
		H	L	L	L	L	L	L	L	L	L	L	→V2
		L	H	L	L	L		L	L	L	L	L	→V3
													Vofc=V2−V1
													Vofc=V3−V1
Voltage Gain	Gvcl	L	L	L	L	L	L	L	L	H	L	L	G_{IN}: 1MHz wave, C_{OUT}: 2.0$V_{P\text{-}P}$
		H	L	L	L	L	L	L	L	L	H	L	
		L	H	L	L	L	L	L	L	L	L	H	Judgment by left three conditions
Voltage Gain Variable Width	Gvc	L	L	L	L	L	L	L	L	H	L	L	TP21: 2.5V boltage gain→Vv1
		H	L	L	L	L	L	L	L	L	H	L	TP21: 2.0V voltage gain
		L	H	L	L	L	L	L	L	L	L	H	TP21: 2.0V voltage gain
													At left three switch conditions
													Gvc=Gv2−Gv1 } Judgment Gvc=Gv3−Gv1 }
Frequency Gain	Gfc	L	L	L	L	L	L	L	L	H	L	L	At left three switch conditions
		H	L	L	L	L	L	L	L	L	H	L	G_{IN}: 1MHz voltage gain→Gv4
		L	H	L	L	L	L	L	L	L	L	H	G_{IN}8MHz voltage gain→Gv5
													Gfc=Gv5-Gv4 Judgment
Crosstalk	CTc	H	L	L	L	L	L	L	L	H	L	L	C_{IN}: 4.43MHz, 1.0V～$_{P\text{-}P}$ CW wave input
		L	H	L	L	L	L	L	L	H	L	L	C_{OUT}: Measurement
		L	L	L	L	L	L	L	L	L	H	L	
		L	H	L	L	L	L	L	L	L	H	L	
		L	L	L	L	L	L	L	L	L	L	H	
		H	L	L	L	L	L	L	L	L	L	H	
Input Impedance	Ric	L	L	L	L	L	L	L	L	H	L	L	TP19: 3.0V applied voltage, TP6: voltage measurement TP19: 5.0V applied voltage, TP6: voltage measurement Ric=15[kΩ]∗(2−V19/(2−(V2−V1)) Judgment
		H	L	L	L	L	L	L	L	L	H	L	TP22: 3.0V applied voltage, TP7: voltage measurement→ V1 TP22: 5.0V applied voltage, TP7: voltage measurement→ V2 Ric=15[kΩ]∗(V2−V1)/(2−(V−V1)) Judgment
Output Impedance	Roc	L	L	L	L	L	L	L	L	H	L	L	

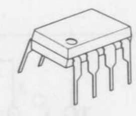
CHROMA SIGNAL HUE TINT CONTROLLER

■ GENERAL DESCRIPTION

NJM2255 is a Chroma signal Hue, Tint controller IC, to be used for VCR, LCD & AV equipments.

In play back operation of video signals of VCRs, Hue and Tint of Chroma signal can be adjusted independently and continuousely by the extemal DC voltage. NJM2255 internalizes the variable capacitor in it, so that it can be operated with minimal external components.

■ PACKAGE OUTLINE



NJM2255D

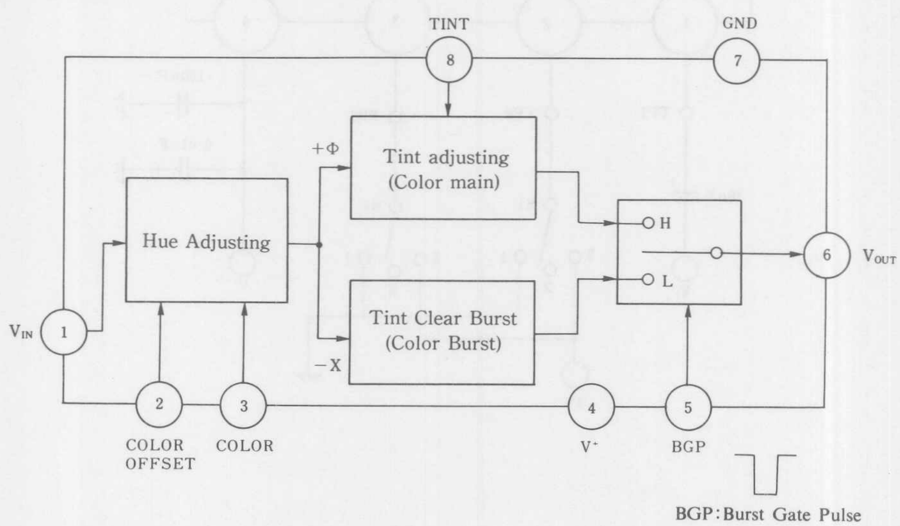
■ FEATURES

- Operating Voltage (+4.7V～+5.3V)
- Internalizing variable capacitor
- Internalizing changeable Gain Amplifier
- Hue and Tint of Chroma signals can be adjusted continuousely by DC voltage (0V－5V)
- Internalizing Dead Band Circuit
- Package Outline DIP8
- Bipolar Technology

■ APPLICATIONS

- VCR, LCD, AV equipments

■ BLOCK DIAGRAM

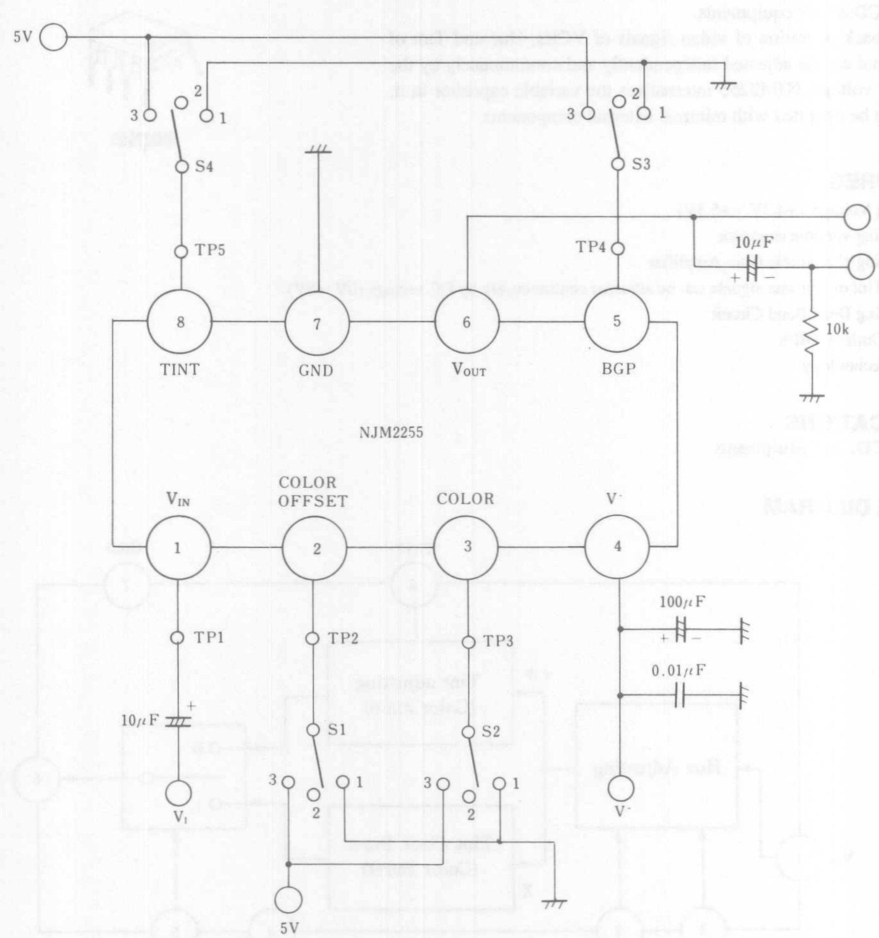


NJM2255D

■ CONTROL INPUT - OUTPUT SIGNAL

SW1	output Signal
H	Color Main
L	Color Burst

■ TEST CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	7	V
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

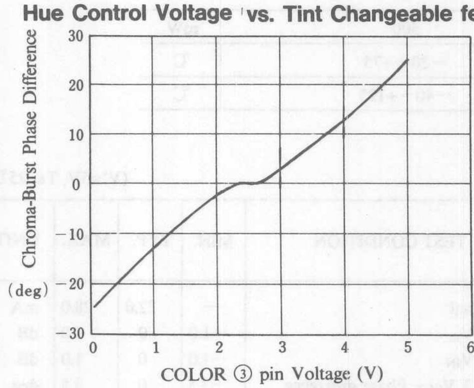
(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	SWITCH				TEST CONDITION	MIN.	TYP.	MAX.	UNIT
		S1	S2	S3	S4					
Operating Current	I_{CC}	2	2	2	2	No signal	—	22.0	28.0	mA
Voltage Gain 1	GC	2	2	3	2	V_{OUT}/V_{In}	−1.0	0	1.0	dB
Voltage Gain 2	GB	2	2	1	2	V_{OUT}/V_{IN}	−1.0	0	1.0	dB
Hue Offset	T1	2	2		2	S3=1/3 V_{OUT} Phase difference	−3.5	0	3.5	deg
Hue Changeable width 1	T2	2	3		2	S3=1/3V_{OUT} Phase difference	20	22	—	deg
Hue Changeable width 2	T3	2	1		2	S3=1/3 V_{OUT} Phase difference	—	−22	−20	deg
Tint Changeable width 1	GC	2	2		2	Gain (S3=3)−Gain (S3=1)	−0.6	0	0.6	dB
Tint Changeable width 2	GB	2	2		3	Gain (S3=3)−Gain (S3=1)	4.5	5.5	—	dB
Tint Changeable width 3	T1	2	2		1	Gain (S3=3)−Gain (S3=1)	—	—	−20	dB
Hue Offset Adjustment width 1	OSTH	3	2		2	S3=1/3 V_{OUT}	—	—	−3.5	deg
Hue Offset Adjustment width 2	OSTL	1	2		2	S3=1/3 V_{OUT}	3.5	—	—	deg
BGP Threashold Voltage 1	VTHH	2	2	3	2	Switch on level	2.2	—	5.0	V
BGP Threashold Voltage 2	VTHL	2	2	3	2	Switch off level	0	—	0.8	V
Secondary Distortion 1	HC	2	2	3	2	3.58MHz, 700mV_{P-P} Sine Wave	—	−37	−33	dB
Secondary Distortion 2	HB	2	2	1	2	3.58MHz, 700mV_{P-P} Sine Wave	—	−37	−33	dB

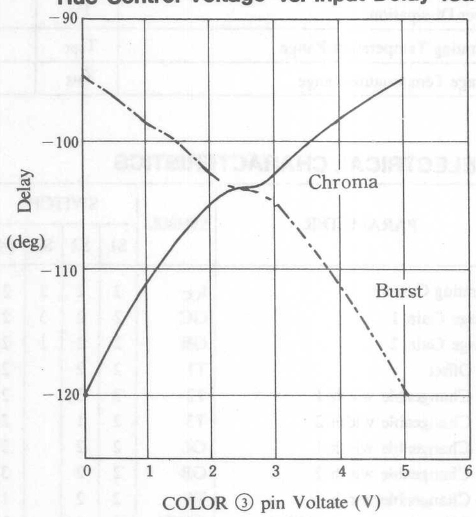
Note Unless otherwise specified, input signal is 3.58MHz and 300mV_{P-P} sine wave.

■ TYPICAL CHARACTERISTICS

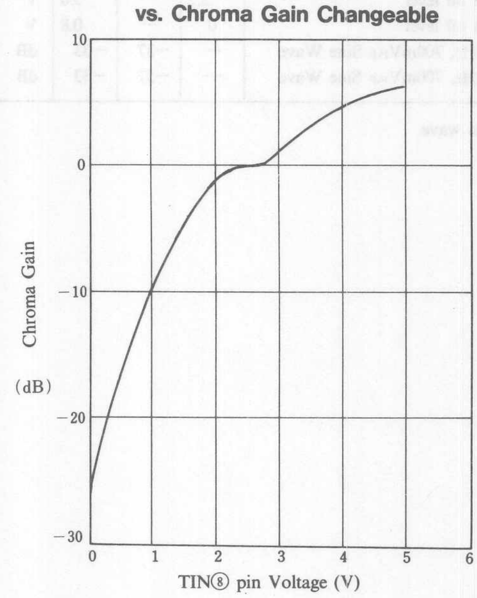
Hue Control Voltage vs. Tint Changeable feature



Hue Control Voltage vs. Input Delay feature



Color Control Voltage vs. Chroma Gain Changeable



VIDEO COLOR SUPERIMPOSER

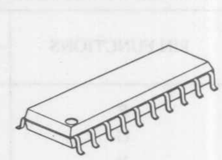
■ GENERAL DESCRIPTION

NJM2256 is the multi-functional color super-imposer IC for video base band (Y, R-Y, B-Y), Various type of Y, R-Y, B-Y output signals can be made by the digital controlled signals.

The signal control at the base band, made it possible on operation with less external parts, as well as for non adjustment on opertaion.

NJM2256 can be operated much higher switching speed comparing to NJM2247.

■ PACKAGE OUTLINE



NJM2256M

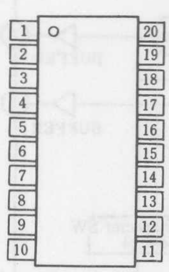
■ FEATURES

- 5 V Single Power Supply
- 8 Types Color Super-imposer
- Burst Flag Insert Function
- Y Inversion, C Inversion Function
- NTSC/PAL Matching
- Non Operational Adjustment
- Less External Parts
- Higher switching speed can be made comparing to NJM2247
- Package Outline DMP20
- Bipolar Technology

■ RECOMMENDED INPUT CONDITIONS

● Y Signal	$0.7V_{P-P}$
● R-Y Signal	$1.0V_{P-P}$
● B-Y Signal	$0.7^{V_{P-P}}$
● Control Voltage	
● Low Level	0~0.25V
● High Level	4.75~5V

■ PIN CONFIGURATION



NJM2256M

Pin Function

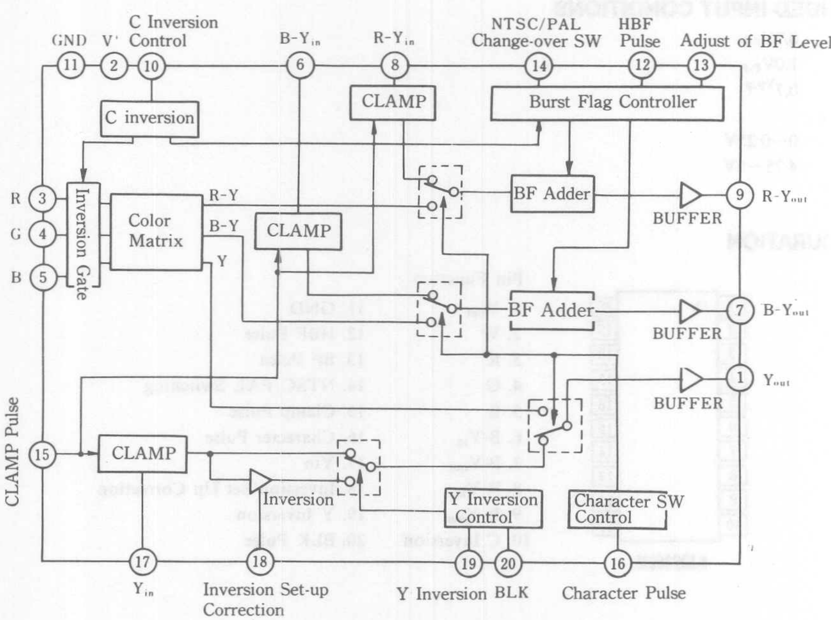
1. Y_{out}	11. GND
2. V^{+}	12. HBF Pulse
3. R	13. BF Pulse
4. G	14. NTSC/PAL Switching
5. B	15. Clamp Pulse
6. $B\text{-}Y_{in}$	16. Character Pulse
7. $B\text{-}Y_{out}$	17. Yin
8. $R\text{-}Y_{in}$	18. Inversion Set Up Correction
9. $R\text{-}Y_{out}$	19. Y Inversion
10. C Inversion	20. BLK Pulse

■ CONTROL PIN CHARACTERISTICS

(V⁺=5V)

PIN NO.	PIN FUNCTIONS	THRESHOLD LEVEL(V)		SINK/SOURCE CURRENT(μA)	
		LOW	HIGH	0V	5V
3 4 5	R G B	0.7	0.8	−500	500
3 4 5	(at C Inversion)	2.5	2.6	−100	100
10	C Inversion	3.5	4.5	−200	400
12	HBF Pulse	0.5	2.0	−2	1
14	NTSC/PAL	0.7	0.8	0	150
15	Clamp Pulse	2.5	2.8	−2	0
16	Character Pulse	0.5	0.9	−0.5	0
19	Y Inversion	0.4	0.8	−0.5	0
20	BLK Pulse	0.4	0.8	−0.5	0

■ BLOCK DIAGRAM



■ INFORMATIONS

Following four points are the outstanding function of the NJM2256. These functions are to go through three input (Y, R-Y, B-Y) signals control by ten control pins.

1. Color Superimpose
   DC level of each equivalent colors shall be supplied to Y, R-Y and B-Y inputs.
2. Burst Flag Insertion
   150 mV burst flag shall be added to R-Y, B-Y input signals.
   Burst flag is selected by the NTSC/PAL switch.
3. C Inversion
   The color phase of the picture shall be inverted for one hundred and eighty degrees. The color phase of the imposed character shall not be altered. This function shall be proceeded when inverting the burst flag, and at the same time, the imposed character level shall be inverted too.
4. Y Inversion
   It is the brightness level inversion. The imposed character color shall not be changed. This function shall be proceeded the switching Y signal output to the inverter side.

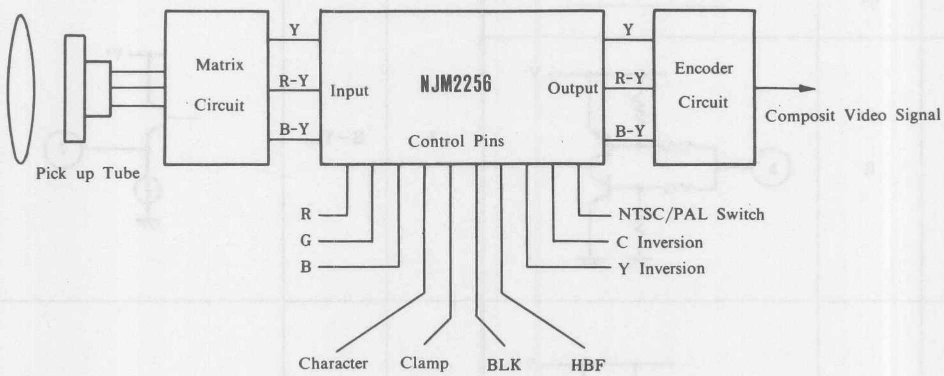
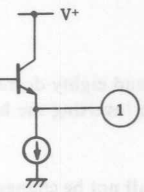
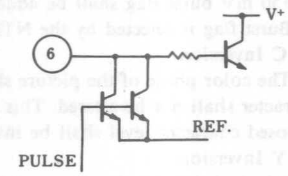
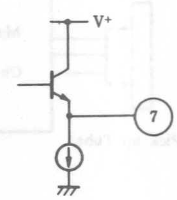
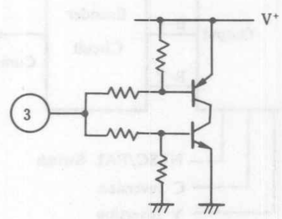
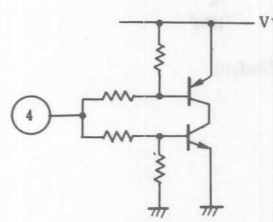
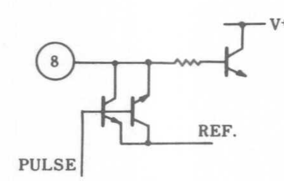
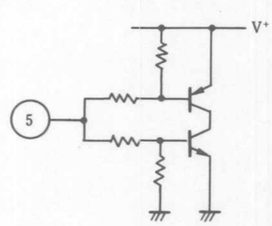
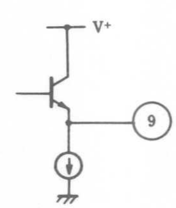
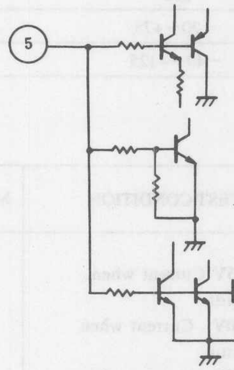
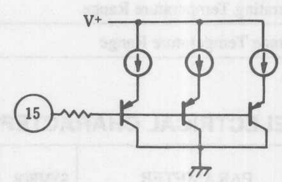
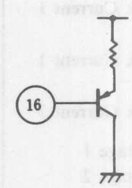
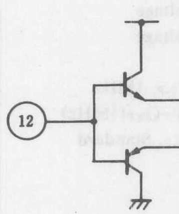
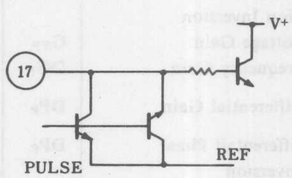
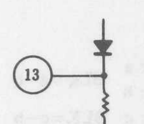
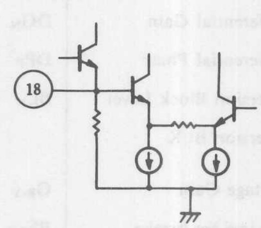
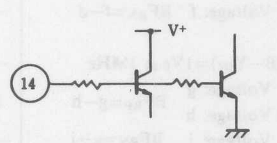
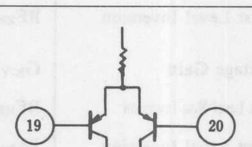


Fig. 1 Video Camera Application

■ EQUIVALENT CIRCUIT

PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT	PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	Y_{out}		6	$B-Y_{in}$	
2	V^+		7	$B-Y_{out}$	
3	R				
4	G		8	$R-Y_{in}$	
5	B		9	$R-Y_{out}$	

■ EQUIVALENT CIRCUIT

PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT	PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT
10	C Inversion		15	Clamp Pulse	
11	GND		16	Character Pulse	
12	HBF Pulse		17	Y_{in}	
13	BF Level		18	Inversion Set up Correction	
14	NTSC/PAL		19 20	Y Inversion BLK	

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Power Dissipation	P_D	350	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

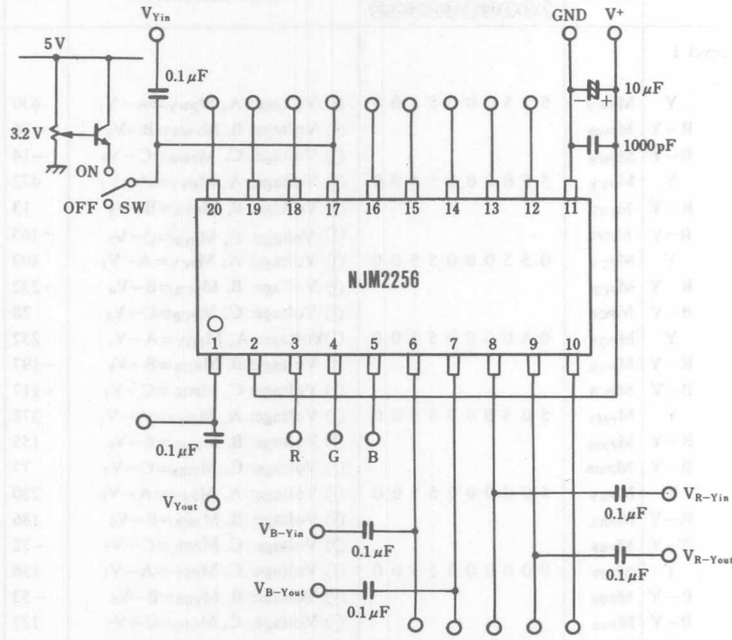
PARAMETER	SYMBOL	CONTROL PIN ③④⑤⑩⑫⑭⑮⑯⑲⑳	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	0 0 0 0 0 0 0 0 0 0		12	18.5	26	mA
Terminal Sink Current 1	I17	0 0 0 0 0 0 0 0 0 0	V⑰=2.5V Current when application	0		10	μA
Terminal Sink Current 1	I6	0 0 0 0 0 0 0 0 0 0	V⑥=3.0V Current when application	0		6	μA
Terminal Sink Current 3	I8	0 0 0 0 0 0 0 0 0 0	V⑧=3.0V Current when application	0		6	μA
Terminal Voltage 1	V_1	0 0 0 0 0 5 0 0 0 0	① Open Voltage	1.68		1.92	V
Terminal Voltage 2	V_7	0 0 0 0 0 5 0 0 0 0	⑦ Open Voltage	2.18		2.42	V
Terminal Voltage 3	V_9	0 0 0 0 0 5 0 0 0 0	⑨ Open Voltage	2.18		2.42	V
Terminal Voltage 4	V_{13}	0 0 0 0 0 5 0 0 0 0	⑬ Open Voltage	0.23		0.37	V
Terminal Voltage 5	V_{18}	0 0 0 0 0 5 0 0 0 0	⑱ Open Voltage	1.68		1.92	V
Y Non Inversion							
Voltage Gain	G_{YP}	0 0 0 0 0 0 0 0 0 0	$V(Y_{IN})=1V_{P\text{-}P}$, 1MHz	−0.5	0	0.5	dB
Frequency Gain	DG_P	0 0 0 0 0 0 0 0 0 0	$G_{YP}(6MHz)-G_{YP}(1MHz)$	−1	0	1	dB
Differential Gain	DP_P	0 0 0 0 0 0 0 0 0 0	$VY_{IN})=1V_{P\text{-}P}$, Standard Staircase	−3	0	3	%
differentail Phase	DP_P	0 0 0 0 0 0 0 0 0 0		−3	0	3	deg
Y Inversion							
Voltage Gain	G_{YN}	0 0 0 0 0 0 0 0 5 5	$V(Y_{IN})=0.6V_{P\text{-}P}$, 1MHz	−2.3	−1.3	0.3	dB
Frequency	G_{FYN}	0 0 0 0 0 0 0 0 5 5	$G_{YN}(6MHz)-G_{YN}(1MHz)$	−2	−0.1	1	dB
Differential Gain	DG_N	0 0 0 0 0 0 0 0 5 5	$V(Y_{IN})=0.5V_{P\text{-}P}$, Standard Staircase	−8		8	%
Differential Phase	DP_P	0 0 0 0 0 0 0 0 5 5		−3	0	3	deg
Inversion Block Level	BL_N	0 0 0 0 0 0 5 0 5 5 0 0 0 0 0 0 5 0 5 5	① Voltage: a ① Voltage: b $BL_N=a-b$	0.59	0.68	0.77	V
Inversion BLK		0 0 0 0 0 0 5 0 5 0	① Voltage: c BLK=c−b	−0.1	0	0.1	V
R-Y							
Voltage Gain	$G_{R\text{-}Y}$	0 0 0 0 0 0 5 0 0 0	$V(R-Y_{IN})=1V_{P\text{-}P}$, 1MHz	−0.5		0.5	dB
Burst Level Non Inversion	BF_{RP}	0 0 0 0 0 0 5 0 0 0 0 0 0 5 5 0 5 0 0 0	⑨ Voltage: d ⑨ Voltage: e $BF_{RP}=e-d$	135	150	165	mV
Burst Level Inversion	BF_{RN}	0 0 0 5 5 0 5 0 0 0	⑨ Voltage: f $BF_{RN}=f-d$	−165	−150	−135	mV
B-Y							
Voltage Gain	$G_{R\text{-}Y}$	0 0 0 0 0 0 5 0 0 0	$V(B-Y_{IN})=1V_{P\text{-}P}$, 1MHz	−0.5	0	0.5	dB
Burst Level Non Inversion	BF_{HP}	0 0 0 0 5 5 5 0 0 0 0 0 0 0 0 5 5 0 0 0	⑦ Voltage: g ⑦ Voltage: h $BF_{RP}=g-h$	135	150	165	mV
Burst Level Inversion	BF_{RN}	0 0 0 5 5 5 5 0 0 0	⑦ Voltage: i $BF_{RN}=g-i$	−165	−150	−135	mV
R-Y Switching Speed		X 0 0 0 0 0 5 5 0 0	X=1MHz 5V_{PP} Rectangular Wave			∗100	nS
B-Y Switching Speed		X 0 0 0 0 0 5 5 0 0	X=1MHz 5V_{PP} Rectangular Wave			∗100	nS

∗ Remark 1) ∗ Item indicates design assurance rating.

■ ELECTRICAL CHARACTERISTICS

PARAMETER		SYMBOL	CONTROL PIN ③④⑤⑩⑫⑭⑮⑯⑲⑳	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Character Output Level 1								
C inversion								
White	Y	M_{PWY}	5 5 5 0 0 0 5 5 0 0	① Voltage: A, $M_{PWY}=A-V_1$	630	700	770	mV
	R−Y	M_{PWR}		⑨ Voltage: B, $M_{PWR}=B-V_9$	−16	0	16	mV
	B−Y	M_{PWB}		⑦ Voltage: C, $M_{PWB}=C-V_7$	−14	0	14	mV
Yellow	Y	M_{PYY}	5 5 0 0 0 0 5 5 0 0	① Voltage: A, $M_{PYY}=A-V_1$	472	525	578	mV
	R−Y	M_{PYR}		⑨ Voltage: B, $M_{PYR}=B-V_9$	13	33	53	mV
	B−Y	M_{PYB}		⑦ Voltage: C, $M_{PYR}=C-V_7$	−165	−146	−127	mV
Cyanoge	Y	M_{PCY}	0 5 5 0 0 0 5 5 0 0	① Voltage: A, $M_{PCY}=A-V_1$	409	455	501	mV
	R−Y	M_{PCR}		⑨ Voltage: B, $M_{PCR}=B-V_9$	−232	−209	−186	mV
	B−Y	M_{PCB}		⑦ Voltage: C, $M_{PCB}=C-V_9$	28	50	72	mV
Green	Y	M_{PGY}	0 5 0 0 0 0 5 5 0 0	①Voltage: A, $M_{PGY}=A-V_1$	252	280	308	mV
	R−Y	M_{PGR}		⑨ Voltage: B, $M_{PGR}=B-V_9$	−197	−176	−155	mV
	B−Y	M_{PCB}		⑦ Voltage: C, $M_{PGB}=C-V_7$	−117	−97	−77	mV
Mazenta	Y	M_{PMY}	5 0 5 0 0 0 5 5 0 0	① Voltage: A, $M_{PMY}=A-V_1$	378	420	462	mV
	R−Y	M_{PMR}		⑦ Voltage: B, $M_{PMR}=B-V_9$	155	176	197	mV
	B−Y	M_{PMB}		⑦ Voltage: C, $M_{PMB}=C-V_7$	77	97	117	mV
Red	Y	M_{PRY}	5 0 0 0 0 0 5 5 0 0	① Voltage: A, $M_{PRY}=A-V_1$	220	245	270	mV
	R−Y	M_{PRR}		⑨ Voltage: B, $M_{PRR}=B-V_9$	186	209	232	mV
	B−Y	M_{PRB}		⑦ Voltage: C, $M_{PRB}=C-V_7$	−72	−50	−28	mV
Blue	Y	M_{PBY}	0 0 0 0 0 0 5 5 0 0	① Voltage: C, $M_{PBY}=A-V_1$	156	175	194	mV
	R−Y	M_{PBR}		⑨ Voltage: B, $M_{PBR}=B-V_9$	−53	−33	−13	mV
	B−Y	M_{PBB}		⑦ Voltage: C, $M_{PBB}=C-V_7$	127	146	165	mV
Black	Y	M_{PPY}	0 0 0 0 0 0 5 5 0 0	① Voltage: A, $M_{PPY}=A-V_1$	−20	0	20	mV
	R−Y	M_{PPR}		⑨ Voltage: B, $M_{PPR}=B-V_9$	−14	0	14	mV
	B−Y	M_{PPB}		⑦ Voltage: C, $M_{PPB}=C-V_7$	−12	0	12	mV
Character Output Level 2								
C Inversion								
White	Y	M_{NWY}	5 5 5 5 0 0 5 5 0 0	① Voltage: A, $M_{NWY}=A-V_1$	630	700	770	mV
	R−Y	M_{NWR}		⑨ Voltage: B, $M_{NWR}=B-V_9$	−16	0	16	mV
	B−Y	M_{NWB}		⑦ Voltage: C, $M_{NWB}=C-V_7$	−14	0	14	mV
Yellow	Y	M_{NYY}	5 5 0 5 0 0 5 5 0 0	① Voltage: A, $M_{NYY}=A-V_1$	472	525	578	mV
	R−Y	M_{NYR}		⑨ Voltage: B, $M_{NYR}=B-V_9$	−53	−33	−13	mV
	B−Y	M_{NYB}		⑦ Voltage: C, $M_{PYB}=C-V_7$	127	146	165	mV
Cyanoge	Y	M_{NCY}	0 5 5 5 0 0 5 5 0 0	① Voltage: A, $M_{NCY}=A-V_1$	409	455	501	mV
	R−Y	M_{NCR}		⑨ Voltage: B, $M_{NCR}=B-V_9$	186	209	232	mV
	B−Y	M_{NCB}		⑦ Voltage: C, $M_{NCB}=C-V_7$	−72	−50	−28	mV
Green	Y	M_{NGY}	0 5 0 5 0 0 5 5 0 0	① Voltage: A, $M_{NGY}=A-V_1$	252	280	308	mV
	R−Y	M_{NGR}		⑨ Voltage: B, $M_{NGR}=B-V_9$	155	176	197	mV
	B−Y	M_{NGB}		⑦ Voltage: C, $M_{NGB}=C-V_7$	77	97	117	mV
Mazenta	Y	M_{NMY}	5 0 5 5 0 0 5 5 0 0	⑨ Voltage: A, $M_{NMY}=A-V_1$	378	420	462	mV
	R−Y	M_{NMR}		⑨ Voltage: B, $M_{NMR}=B-V_9$	−197	−176	−155	mV
	B−Y	M_{NMB}		⑦ Voltage: C, $M_{NMB}=C-V_7$	−117	−97	−77	mV
Red	Y	M_{NRY}	5 0 0 5 0 0 5 5 0 0	① Voltage: A, $M_{NRY}=A-V_1$	220	245	270	mV
	R−Y	M_{NRR}		⑨ Voltage: B, $M_{NRR}=B-V_9$	−232	−209	−186	mV
	B−Y	M_{NRB}		⑦ Voltage: C, $M_{NRB}=C-V_7$	28	50	72	mV
Blue	Y	M_{NBY}	0 0 5 5 0 0 5 5 0 0	① Voltage: A, $M_{NBY}=A-V_1$	156	175	194	mV
	R−Y	M_{NBR}		⑨ Voltage: B, $M_{NBR}=B-V_9$	13	33	53	mV
	B−Y	M_{NBR}		⑦ Voltage: C, $M_{NBB}=C-V_7$	−165	−146	−127	mV
Black	Y	M_{NPY}	0 0 0 5 0 0 5 5 0 0	① Voltage: A, $M_{NPY}=A-V_1$	−20	0	20	mV
	R−Y	M_{NPR}		⑨ Voltage: B, $M_{NPR}=B-V_9$	−14	0	14	mV
	B−Y	M_{NPB}		⑦ Voltage: C, $M_{NPB}=C-V_7$	−12	0	12	mV

■ TEST CIRCUIT



■ APPLICATION NOTES

I/O Explanation

• Supply Voltage	V^+	5V	②
	GND		⑪
• Input Signals	Y	0.7 V_{P-P}	⑰
	R-Y	1.0 V_{P-P}	⑧
	B-Y	0.7 V_{P-P}	⑥
• Output Signals	Y	0.7 V_{P-P}	①
	R-Y	1.0 V_{P-P}	⑨
	B-Y	0.7 V_{P-P}	⑦

■ APPLICATION NOTES

I/O Explanation

- Control Pin Low=0V, HIGH=5V

R③, G④, B⑤ — Superimposed color adjustment

Clamp Pulse ⑮, Character Pulse ⑯, HBF Pulse ⑫, BLK Pulse ⑳ — Y, R-Y, B-Y signal process pulse input

C Inversion ⑩, Y Inversion ⑲ — Color difference, brightness inverting pin

NTS/PAL Switch ⑭

- Adjusting Pin (Normally open → non adjustment)

BF level ⑬ Burst flag insert level adjusting pin.
Inversion set up correction ⑱ Y inversion signal level adjusting pin.

1. Input Signal

Superimposed color level shall be determined by the following standard signal level.

Y 0.7V_{P-P}
R-Y 1.0V_{P-P}
B-Y 0.7V_{P-P}

The character output standard level on the specification shall be determined through calculation out of 75 % of superimposed color level.

(In order to avoide the clipping of the encoding signal, the character output level is determined to lower level)

- The character output level converting expression

The basic expression

$E_R - E_Y = 0.70E_R - 0.59E_G - 0.11E_B$
$E_B - E_Y = -0.30E_R - 0.59E_G + 0.89E_B$
$E_Y = 0.30E_R + 0.59E_G + 0.11E_B$

From standard level and practical input level, each color signal level imposed in R-Y, B-Y and Y signals are as in the following.

$V_{R-Y} = 0.75 \times 1[V_{P-P}] \times E_{R-Y}/1.4$
$= 0.375E_R - 0.316E_G - 0.059E_B$
$V_{B-Y} = 0.75 \times 0.7[V_{P-P}] \times E_{B-Y}/1.78$
$= -0.088E_R - 0.174E_G + 0.263E_B$
$V_Y = 0.75 \times 0.7[V_{P-P}] \times E_Y/1$
$= 0.158E_R + 0.310E_G + 0.058E_B$
(E_R, E_G, E_B は, LOW 0, HIGH 1)

2. Clamp Pulse

During the interval of blanking, input the pulse through clamp pulse pin ⑳ the blanking level (0 level) of input signal (Y, R-Y, B-Y) is to be fixed at the bias point within the IC.

Note) The pulse width of clamp pulse shall be set more than 3 μs. (see figure 2)

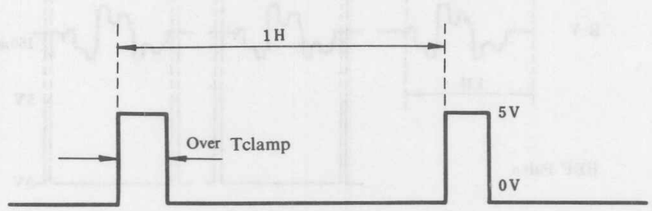


Fig. 2 Clamp Pulse Width

3. Character Color Adjustment

Superimposed color adjustment of the character can be determined in eight different colors, by choosing R, G, B input levels.

(LOW 0 V, HIGH 5 V)

R	G	B	COLOR
5	5	5	White
5	5	0	Yellow
0	5	5	Cyan
0	5	0	Green
5	0	5	Magenta
5	0	0	Red
0	0	5	blue
0	0	0	Black

Character Color Selecting Code

4. Character Insertion

Pulse informations from outside character generater shall be given input at the character pulse pin ⑯. During the period of pulse process, the selected color level shall be inserted into each Y, R-Y, B-Y.

5. Burst Flag Insertion

Inputting burst period pulse at the HBF pin ⑫, the burst flag (150mV) can be inserted in the B-Y, R-Y signals. At the same time, by putting NTSC/PAL switch ⑭, the burst flag can be altered to NTSC or PAL system.

	NTSC/PAL SWITCH⑭	
	LOW 0 V (PAL)	HIGH 5 V (NTSC)
R-Y Signal	+150 mV	non insertion
B-Y Signal	−150 mV	−150 mV

Burst Flag Inserting

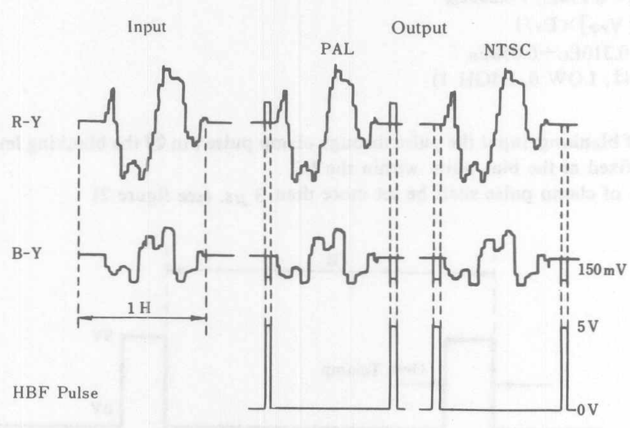


Fig.3 Burst Flag Inserting Example

6. C Inversion

The color phase of the picture shall be inverted for one hundred and eighty degrees setting C inversion pin ⑩. It is applied that the reference signal (burst flag) shall be inverted into one hundred and eighty degrees at the time of de-coding.

Superimposed character color do not change at the picture inversion.

	C INVERSION PIN ⑩	
	LOW 0 V	HIGH 5 V
Burst	Non Inversion	Inversion

C Inversion Form

7. Y Inversion

The brightness of the picture shall be inverted by setting Y inversion pin ⑲. It is that Y signal shall be inverted by the inverter, and then blanking period signal shall be adjusted to the black level with blanking pulse.

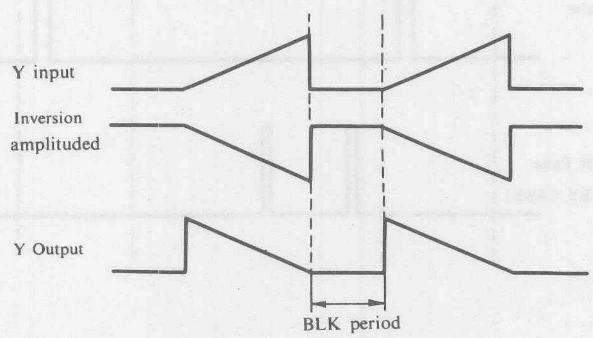


Figure 4. Y Inversion Output Example

	Y INVERSION PIN ⑲	
	LOW 0 V	HIGH 5 V
Y output	Non inversion	Inversion

Y Inversion Form

8. Adjusting pin

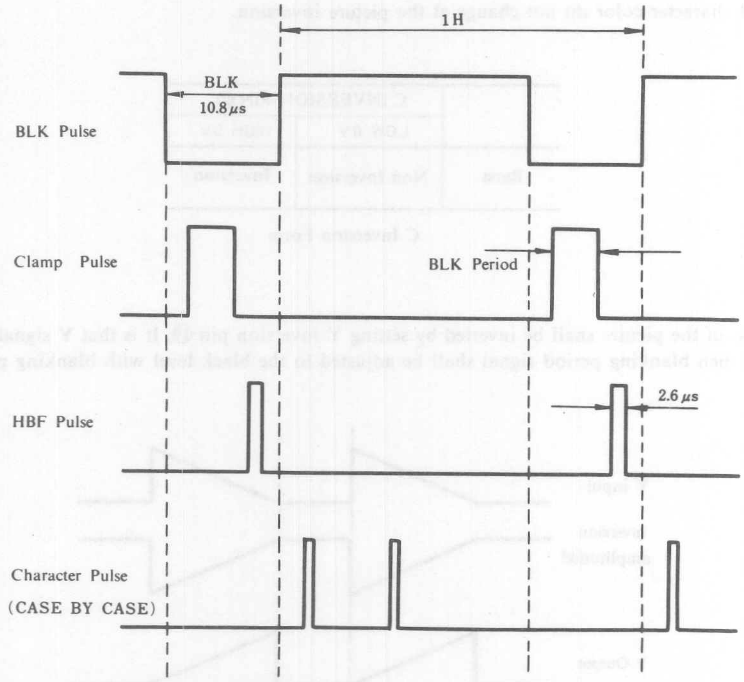
(1) BF Level Pin ⑬

It is the burst flag minor adjusting pin. The burst level shall be adjusted at the open voltage, 0.3V level adjustment. Therefore, the most recommended on operation with the open condition, as it has been controlled at 135 to 165 mV (burst level) on specification.

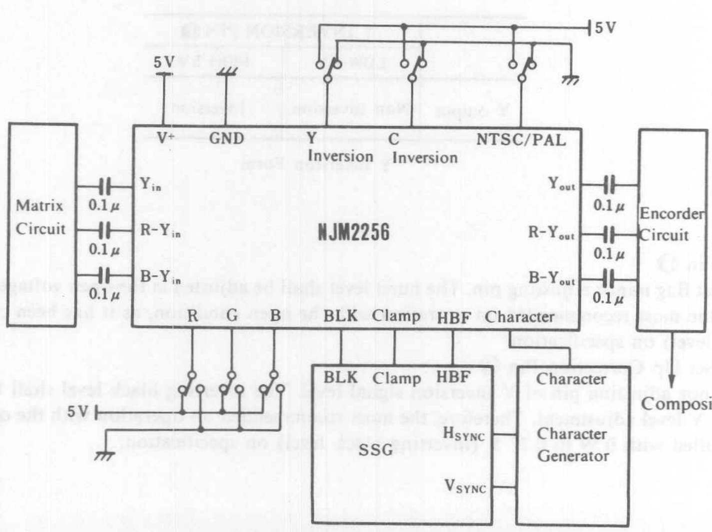
(2) Inversion Set Up Correction Pin ⑱

It is the minor adjusting pin of Y inversion signal level. The inverting black level shall be adjusted at the open voltage, 1.8 V level adjustment. Therefore, the most recommended on operation with the open condition, as it has been controlled with 0.59 to 0.77 V (inverting black level) on specification.

9. Pulse Timing
The pulse input timing should be proceeded as in the following.



■ **TYPICAL APPLICATION**



SYNCHRONOUS SEPARATOR WITH AFC

■ GENERAL DESCRIPTION

NJM2257 excutes Horizontal and Vertical synchronous signal separation, and odd/even field signal detection, from composit video signals.

Built-in 1/2 fH Killer Function circuit can make stabilization of the Horizontal signal oscillation output during the Vertical period.

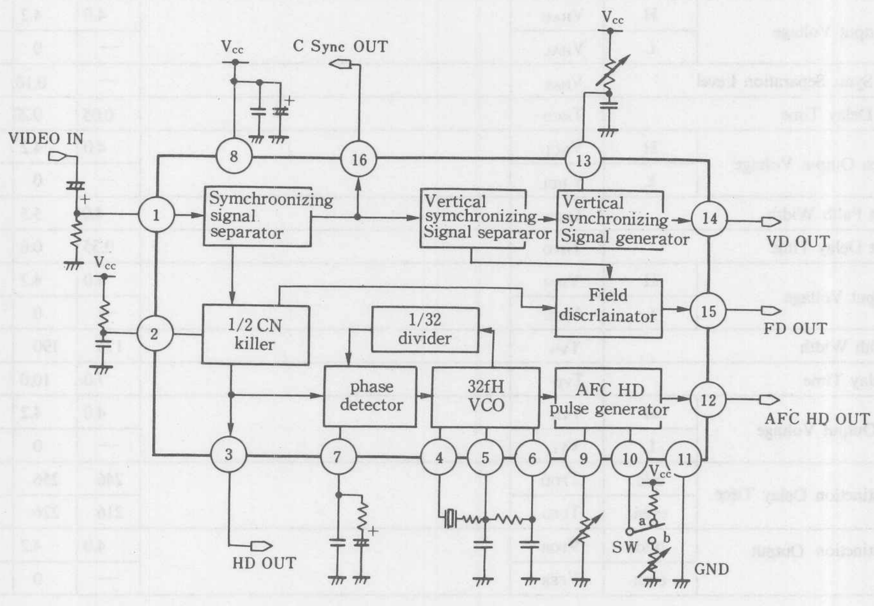
■ FEATURES

- Operating Voltage (+4.5～+5.3V)
- Internal AFC circuit (Horizontal sync. signal.)
- Internal 1/2fH Killer Function
- AFC output Pulse Delay time is Adjustable
- Vertical synchronous pulse width is Adjustable
- Internal Field Discrlainat Function
- Package Outline DIP16, DMP16
- Bipolar Technology

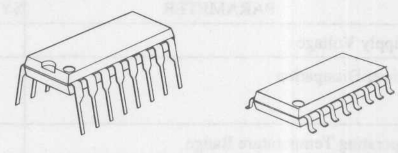
■ APPLICATION

- VTR, TV, AV components etc.

■ BLOCK DIAGRAM



■ PACKAGE OUTLINE



NJM2257D NJM2257M

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

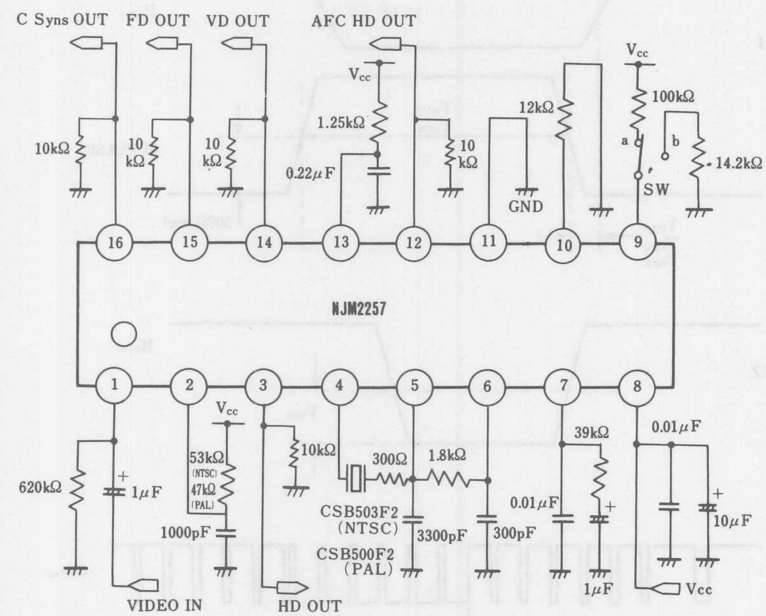
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+7	V
Power Dissipation	P_D	(DIP16) 500 (DMP16) 350	mW mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(Vcc=5V, Ta=25℃)

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiessent Current		I_Q		—	23.0	30.0	mA
AFC Free Run Frequency		f_{OH}		15.54	15.74	15.94	KHz
AFC HD pulse width		T_{AHW1}	SW=a	3.5	4.0	4.5	μS
		T_{AHW2}	SW=b	2.5	4.0	5.5	
AFC HD Delet Time		T_{AHD}		−1.0	0.5	2.0	μS
AFC Lock Range		Δf_{HL}		500	700	—	Hz
AFC Cap Charange		Δf_{HP}		400	600	—	Hz
AFC Output Voltage	H	V_{HAH}		4.0	4.2	—	V
	L	V_{HAL}		—	0	0.1	
Sync Sepa Sync. Separation Level		V_{HSR}		—	0.16	0.18	V
Sync Sepa Delay Time		T_{HCD}		0.05	0.20	0.35	μS
Sync Sepa Output Voltage	H	V_{HCH}		4.0	4.2	—	V
	L	V_{HCL}		—	0	0.1	
HD Output Palth Width		T_{HPW}		4.0	5.5	7.0	μS
HD Output Delay Time		T_{HPD}		0.35	0.6	0.8	μS
HD Output Voltage	H	V_{HfH}		4.0	4.2	—	V
	L	V_{HfL}		—	0	0.1	
V Sync Palth Width		T_{VW}		170	190	210	μS
V Sync Delay Time		T_{VD}		7.0	10.0	13.0	μS
V Sync Output Voltage	H	T_{VH}		4.0	4.2	—	V
	L	V_{VL}		—	0	0.1	
Field Distinction Delay Time	odd	T_{FOD}		246	256	266	μS
	even	T_{FED}		216	226	236	
Field Distinction Output Voltage	odd	V_{FOR}		4.0	4.2	—	V
	even	V_{FER}		—	0	0.1	

■ APPLICATION CIRCUIT



■ APPLICATION NOTES

It shows the characteristics by changing of the following resistor.

- The resistance between 9 Pin and GND
  High resistance——AFC HD pulse is wide
  Low resistance——AFC HD pulse is narrow
- The resistor between 9 Pin and V+
  At the resistor is 100Ω. AFC HD Delay adjustment is off, and AFC HD output width is 4μs (typ.)
- The resistor between 9 Pin and GND is fandamentally 14.2 kΩ, because the purpose of this resistor is pulse width adjusts 4μs
- The resistor between 10 Pin and GND
  High resistance——AFC HD Delay time gains
  Low resistance——AFC HD Delay time loses
- The resistor between 13 Pin and GND
  High resistance——Vsynk pulse is wide
  Low resistance——Vsynk pulse is narrow
- The resistor joind 2 Pin
  Please adjust the wide of following W is from 33 μs to 37 μs

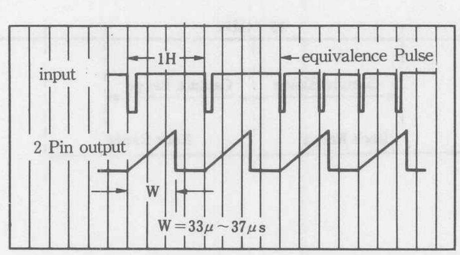
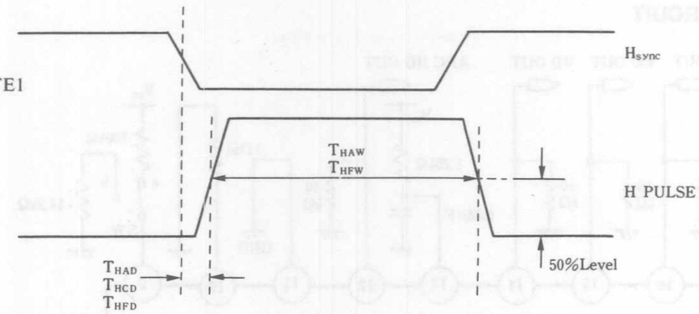
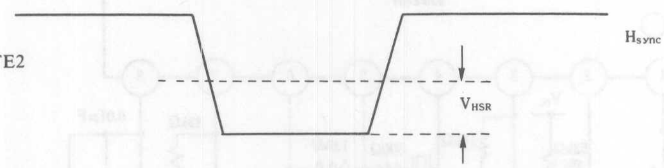


Fig 1 I/O PULSE

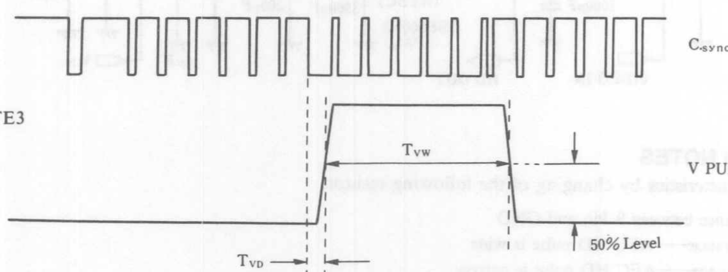
NOTE1



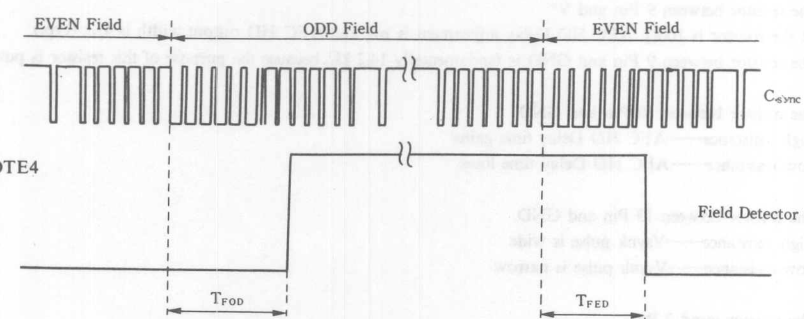
NOTE2



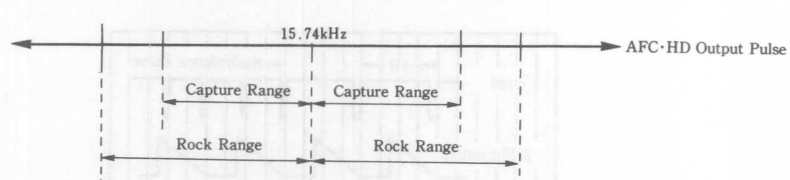
NOTE3



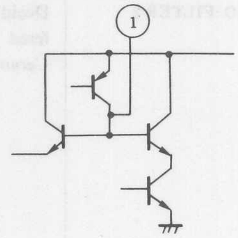
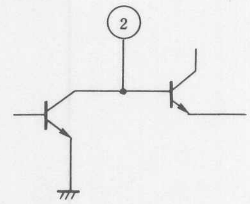
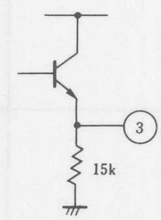
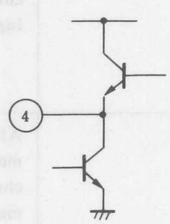
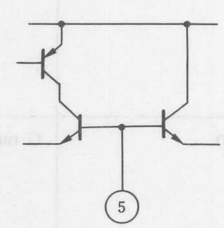
NOTE4



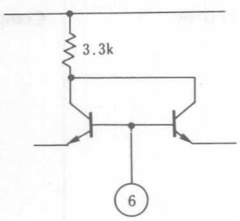
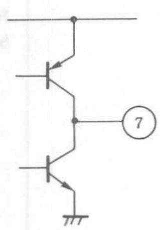
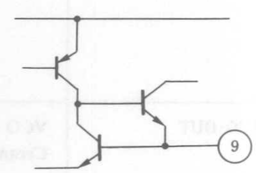
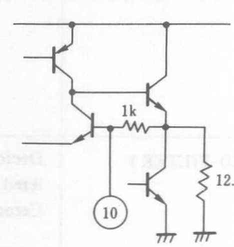
NOTE5



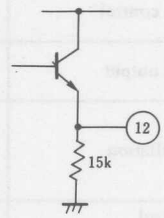
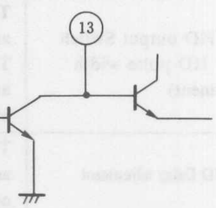
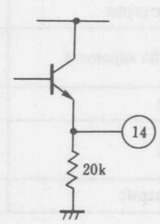
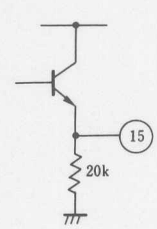
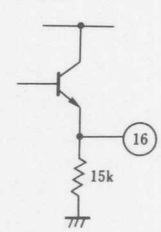
■ TERMINAL EXPLANATION

PIN NO.	PIN NAME	FUNCTION	INSIDE EQUINALENT CIRCUIT
1	VIDEO-IN	Composit Video Signal Input	
2	MM-HT	HD & FD puse are Controlled by setling mono multi	
3	HD-OUT	1/2 f_H Killer D Output	
4	VCO-OUT	VCO Output is to be given to Ceramic Oscillator	
5	VCO-FILTER 1	Decide the Volume to be transfered shall by decided of Ceramic Oscittator. (90°late)	

■ TERMINAL EXPLANATION

PIN NO.	PIN NAME	FUNCTION	INSIDE EQUINALENT CIRCUIT
6	VCO-FILTER 2	Decide the Volume to be transfered shall by decided of Ceramic Oscittator. (90°late)	
7	L.P.F	L.P.F. of AFC	
8	V+	Supply Voltage	
9	VR-1	AFC-HD Output Can be adjusted by putting resistor betwee 9~GND (9 to V_{CC}no adjustment). The pulse width cam be adjusted by making changeable of resister (Adjusting mode)	
10	VR-2	AFC-HD Output delay adjustment by putting 10 pin resister changeabl at 9 pin adjustment mode.	
11	GND	G raund	

■ **TERMINAL EXPLANATION**

PIN NO.	PIN NAME	FUNCTION	INSIDE EQUINALENT CIRCUIT
12	AFC, HD-OUT	AFC·HD Output	
13	MM-VT	Pulse Width of Vsync-OUT is adjusted by setting mono multi time constant.	
14	Vsync-OUT	Vertical Synchronous Signal Output.	
15	FD-OUT discrimination	Field Distiniction Signal Output.	
16	Csync-OUT	Synchronous Separation Output	

■ **PIN FUNCTION**

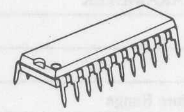
PIN NO	FUNCTION BLOCK	OPERATIONAL DESCRIPTION	NDTE
① Pin	Signal Input	Video Signal input	Sync tip clump
② Pin	HD pulse control	HD pulse and FD pulse control by time constant of CR	
③ Pin	HD pulse output	1/2 f_H killer HD pulse output	In a period of vertical synchronizing, a f_H is converted to f_H
④ Pin ⑤ Pin ⑥ Pin	AFC Oscillation	Oscillation of 503KHz by a ceramic oscillator, and divided by 32 to get down to 15.74KHz	
⑦ Pin	AFC control	Lag Lead filter for phase detection	
⑧ Pin	V_{CC}	V_{CC}	
⑨ Pin	AFC HD output Switch (AFC HD pulse width adjustment)	The case that R is connected between 9pin and V_{CC}···Fixed output The case that R is connected between 9pin and GND···Adjustable AFC HD Delay Mode	high Resistance → Wide pulse width Low Resistance → Narrow pulse widh
⑩ Pin	AFC HD Delay adjustment	The case that R is connected between 9pin and GND···Adjustable AFC HD Delay output	High REsistance → Low Resistance →
⑪ Pin	GND	GND	
⑫ Pin	AFC HD output	AFC HD pulse output	Positive polarity
⑬ Pin	VD pulse width adjustment	VD pulse widh control by time constant of CR	
⑭ Pin	VD output	Vertical synchronizing signal output	Positive polarity
⑮ Pin	FD output	Field discriminating signal output	odd field → High Output even field → Low Output
⑯ Pin	C Sync. output	Composite Sync Signal output	Positive polarity

VIDEO EQUALIZER

■ GENERAL DESCRIPTION

NJM2258 is the IC functioning the gain high pass correction, as well as for equalizing function of wave distortion correction, generated by bright signal of group delay feature like low band filter. It has internalizing REC line, one circuit, and then the playback line 2 circuit.

■ PACKAGE OUTLINE



NJM2258L

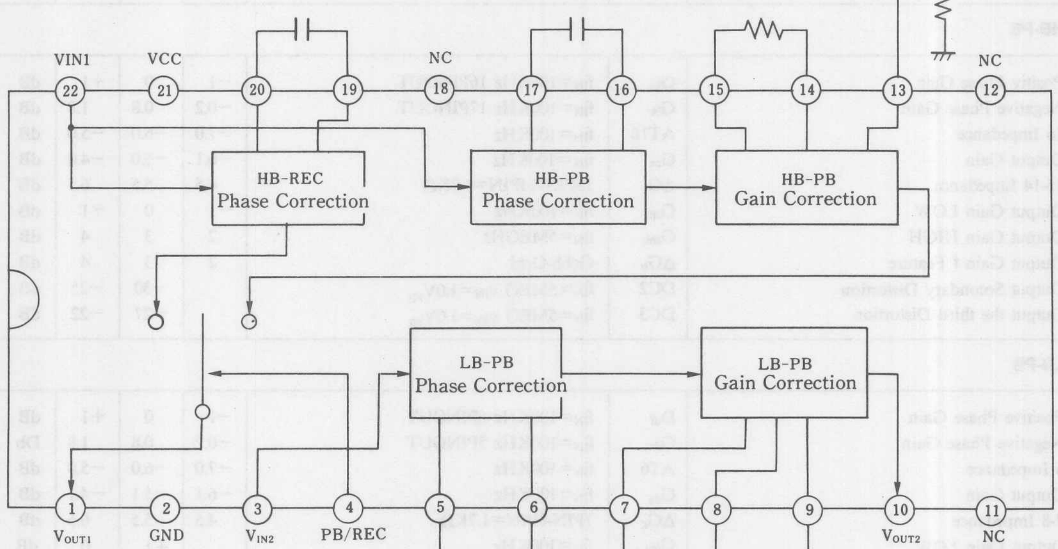
■ FEATURES

- 5V Spec, (Recmmended Operating Voltage Range)
- Wide Band Width, 10MHz
- REC/PLAYBCK Change over function attached
- Package Outline SDIP22
- Bipolar Technology

■ Application

- VCR (S-VHS compatible)
- Video Camera
- Laser Disc

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	7	V
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_p	No Signal		26	34	mA
HB-REC						
Phase Positive Gain	G_{af}	f_{IN}=100KHz 19PINOUT	−1	0	+1	dB
Phase Negative Gain	G_{ar}	f_{IN}=100KHz 20PINOUT	−6.4	−5.4	−4.4	dB
19pin Impedance	AT19	f_{IN}=100KHz	−7.0	−6.0	−5.0	dB
Output Gain LOW	G_{al}	f_{IN}=100kHz	−1	0	+1	dB
Output Gain HIGH	G_{ah}	f_{IN}=5MEGHz	−1	0	+1	dB
Output Gain f Feature	ΔG_a	Gah-Gal	−1	0	+1	dB
Output Secondary Distortion	DA2	f1IN=5MEG v_{IN}=1.0V_{pp}		−40	−30	dB
Output the third Distortion	DA3	f_{IN}5MEG v_{IN}=1.0V_{pp}		−36	−30	dB
HB-PB						
Positiv Phase Gain	G_{bf}	f_{IN}=100KHz 16PINOUT	−1	0	+1	dB
Negative Phase Gain	G_{br}	f_{IN}=100KHz 17PINOUT	−0.2	0.8	1.8	dB
16 Impedance	AT16	f_{IN}=100KHz	−7.0	−6.0	−5.0	dB
Output Gain	G_{ca}	f_{IN}=100KHz	−6.1	−5.0	−4.0	dB
15-14 Impedance	ΔG_c	15PIN-14PIN=1.7KΩ	4.5	5.5	6.5	dB
Output Gain LOW	G_{cbl}	f_{IN}=100KHz	−1	0	+1	dB
Output Gain HIGH	G_{cbh}	f_{IN}=5MEGHz	2	3	4	dB
Output Gain f Feature	ΔG_b	Gcbh-Gcbl	2	3	4	dB
Output Secondary Distortion	DC2	f_{IN}=5MEG v_{IN}=1.0V_{pp}		−30	−25	dB
Output the third Distortion	DC3	f_{IN}=5MEG v_{IN}=1.0V_{pp}		−27	−22	dB
LB-PB						
Positive Phase Gain	D_{df}	f_{IN}=100KHz 6PINOUT	−1	0	+1	dB
Negative Phase Gain	G_{dr}	f_{IN}=100KHz 5PINOUT	−0.2	0.8	1.8	Db
6 Impedance	AT6	f_{IN}=100KHz	−7.0	−6.0	−5.0	dB
Output Gain	G_{da}	f_{IN}=100KHz	−6.1	−5.1	−4.1	dB
7-8 Impedance	ΔG_d	7PIN-8PIN=1.7KΩ	4.5	5.5	6.5	dB
Output Gain LOW	G_{ebl}	f_{IN}=100KHz		+1	0	dB
Output Gain HIGH	G_{ebh}	f_{IN}=5MEGHz	−1	0	+1	dB
Output Gain f Feature	ΔG_e	Gebh-Gebl	−1	0	+1	dB
Output Secondary Distortion	DE2	f_{IN}=5MEG v_{IN}=1.0V_{pp}		−35	−28	dB
Output the third Distortion	DE3	f_{IN}=5MEG v_{IN}=1.0V_{pp}		−36	−30	dB

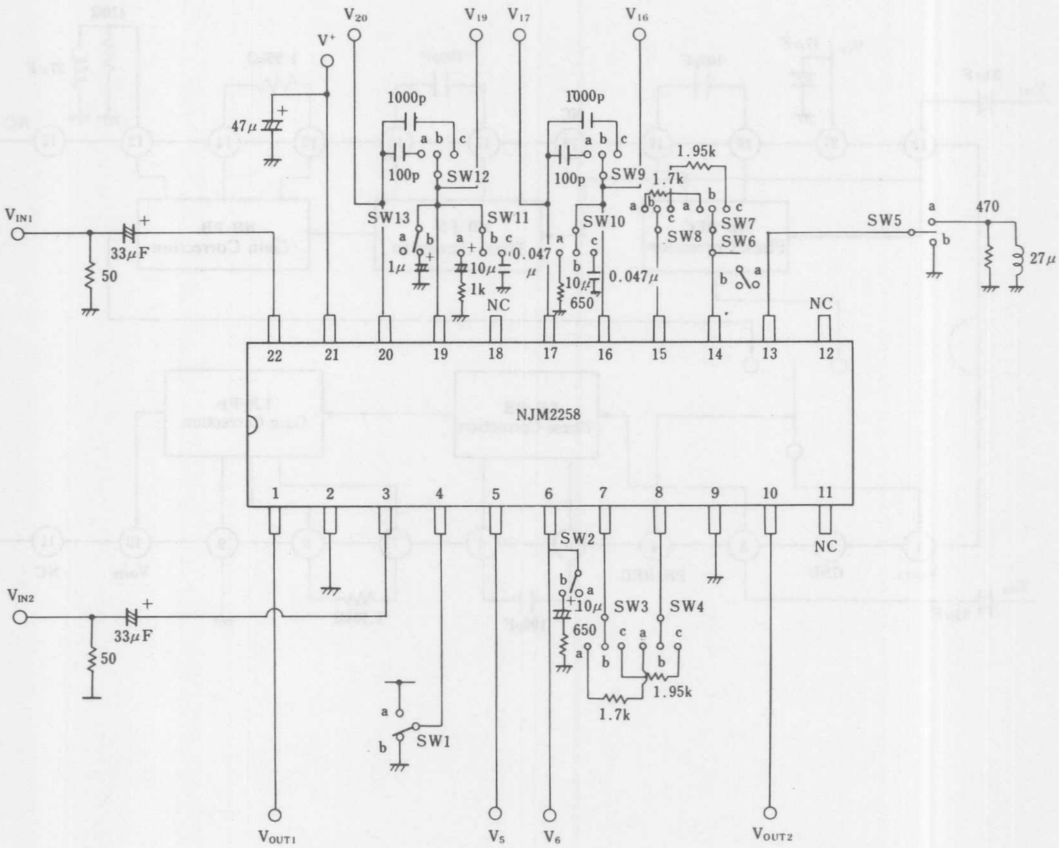
■ TERMINAL FUNCTION

PIN	PIN NAME	SYMBOL	FUNCTION
1	HB-REC/PB OUT	VOUT1	HB type (S-VHS) Correction Output Pin
2	GND	GND	Ground
3	LB-PB IN	VIN2	LB type, (VHS) play-back signal Input Pin
4	HB-REC/PB Change over	PB REC	HB type, Change-over output of REC signal or Play-back signal High makes play-back signal output, and low makes REC signal output.
5	LB-PB Phase Correction Pin 1	LPC1	Connecting Capacitor between Pin 5~6, which helps to give feature of correcting the group delay.
6	LB-PB Phase Correction Pin 2	LPC2	Connecting Capacitor between Pin 5~6, which helps to give feature of correcting the group delay.
7	LB-PB Gain Correction Pin 1	LGC1	Setting up Gain by eonnecting resistor between Pin 7~8.
8	LB-PB Gain Correction Pin 2	LGC2	Setting up Gain by eonnecting resistor between Pin 7~8.
9	LB-PB Gain Correction Pin 3	LP	Connecting L-C parallel resonance between pin 9~GND, helps to give High band keeping, and if not required of keeping connect to GND.
10	LB-PB OUT	VOUT2	LB type Output pin
11	N.C		N.C pin
12	N.C		N.C pin
13	LB-PB Gain Correction Pin 3	HP	Connecting L-C parallel resonance between pin 13~GND, helps to give High band keeping, and if not required of keeping connect to GND.
14	LB-PB Gain Correction Pin 2	HPG1	Setting up Gain by eonnecting resistor between Pin 14~15.
15	LB-PB Gain Correction Pin 1	HPG2	Setting up Gain by eonnecting resistor between Pin 14~15.
16	LB-PB Phase Correction Pin 2	HPC1	Connecting Capacitor between Pin 16~17, which helps to give feature of correcting the group delay.
17	LB-PB Phase Correction Pin 1	HPC2	Connecting Capacitor between Pin 16~17, which helps give feature of correcting the group delay.
18	N.C		N.C pin
19	LB-PB Phase Correction Pin 2	HRC1	Connecting Capacitor between Pin 19~20, which helps to give feature of correcting the group delay.
20	LB-PB Phase Correction Pin 1	HRC2	Connecting Capacitor between Pin 19~20, which helps to give feature of correcting the group delay.
21	V^+	V_{CC}	Voltage Source.
22	HB-REC/PB IN		HB type Input pin.

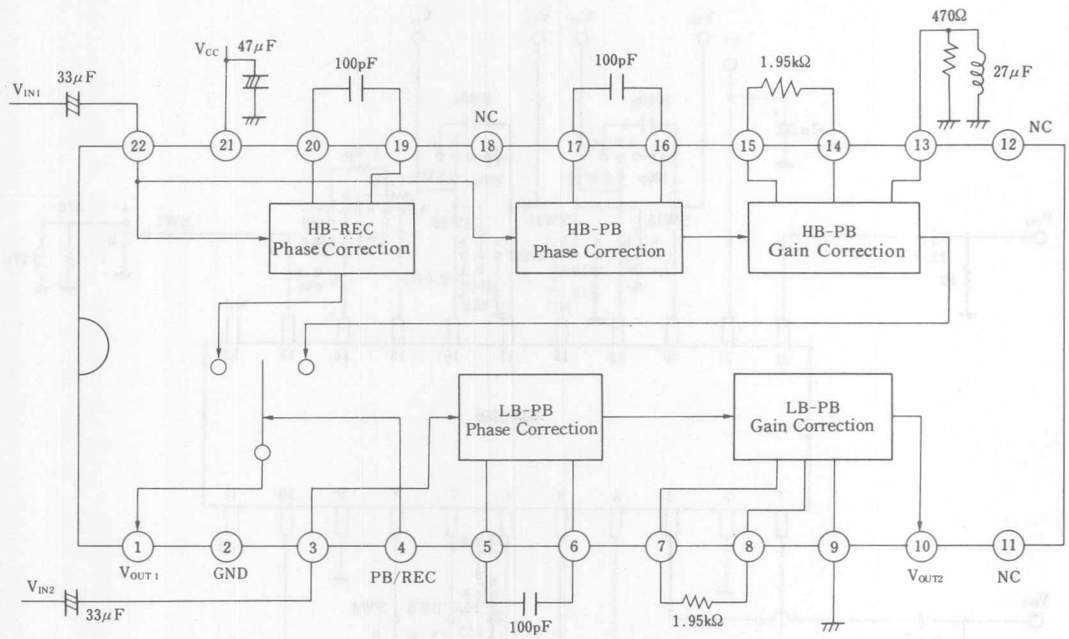
■ TEST CONDITION

PARAMETER	SW－CONDITION													TEST PIN	TEST CONDITION
	1	2	3	4	5	6	7	8	9	10	11	12	13		
I_P	a	a	b	b	b	a	b	b	b	b	b	b	a		
GAf	b													V19	f=100kHz, V=0.5V_{PP}
GAr													b	V20	f=100kHz, V=0.5V_{PP}
AT19											a		a	V19	f=100kHz, V=0.5V_{PP}
Gal											b	a		VOUT1	f=100kHz, V=0.5V_{PP}
Gah											b	a		VOUT1	f=5MHz, V=0.5V_{PP}
DA2												c		VOUT1	f=5MHz, V=1.0V_{PP}
DA3												c		VOUT1	f=5MHz, V=1.0V_{PP}
Gbf														V16	f=100kHz, V=0.5V_{PP}
Gbr														V17	f=100kHz, V=0.5V_{PP}
AT16										a				V16	f=100kHz, V=0.5V_{PP}
Gca	a								a	b				VOUT1	f=100kHz, V=0.5V_{PP}
ΔGca							a	a						VOUT1	f=100kHz, V=0.5V_{PP}
Gcbl					a		c	c						VOUT1	f=100kHz, V=0.5V_{PP}
Gcbh					a		c	c						VOUT1	f=5MHz, V=0.5V_{PP}
DC2					b		c	c	c					VOUT1	f=5MHz, V=1.0V_{PP}
DC3					b		c	c	c					VOUT1	f=5MHz, V=1.0V_{PP}
Gdf	a										b	a		V6	f=100kHz, V=0.5V_{PP}
Gdr														V5	f=100kHz, V=0.5V_{PP}
AT6		b												V6	f=100kHz, V=0.5V_{PP}
Gda		a												VOUT2	f=100kHz, V=0.5V_{PP}
ΔGd			a	a										VOUT2	f=100kHz, V=0.5V_{PP}
Gebl			c	c										VOUT2	f=100kHz, V=0.5V_{PP}
Gebh			c	c										VOUT2	f=5MHz, V=0.5V_{PP}
DE2			c	c										VOUT2	f=5MHz, V=1.0V_{PP}
DE3			c	c										VOUT2	f=5MHz, V=1.0V_{PP}

■ TEST CIRCUIT



■ APPLICATION CIRCUIT



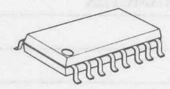
2-INPUT VIDEO SUPERIMPOSER

■ GENERAL DESCRIPTION

NJM 2262 is a 2input video superimposer, inculuding video switch circuit that consist of four Y signal circuit and one C signal circuit.

Its impose voltage is set up white level and black level but You can fix its impose voltage.

■ PACKAGE OUTLINE



NJM2262M

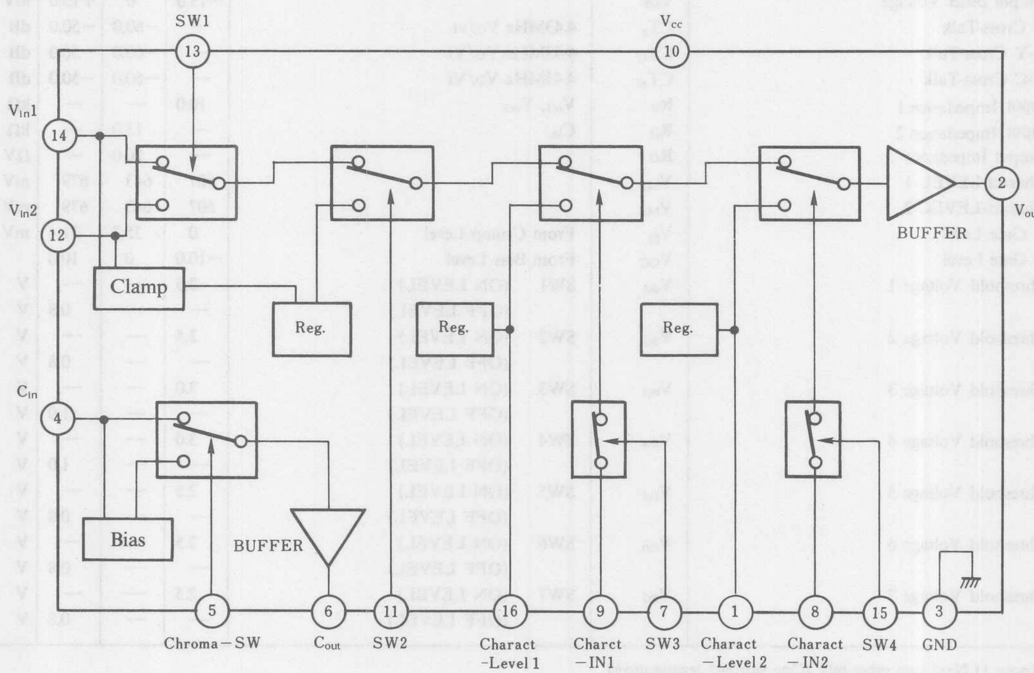
■ FEATURES

- Operating Voltage (4.5V～5.5V)
- Low Operating Current : 5V movement (I_{CC}=8mA)
- Internal Video SW
- Internal Clamp circuit and Bias circuit
- Impose voltage is step up white level and black level but you can fix is impose voltage.
- Package Outline DMP16
- Bipolar Technology

■ APPLICATION

- VTR Camera, VTR, TV etc.

■ BLOCK DIAGRAM



NJM2262M

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+7	V
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, V_{in}=1V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	No signal	—	8.0	12.0	mA
Y Voltage Gain	G_{vy}	1MHz, $1V_{p-p}$ Sine Wave	−0.7	−0.2	+0.3	dB
C Voltage Gain	G_{vc}	1MHz, $1V_{p-p}$ Sine Wave	−0.8	−0.3	+0.2	dB
Y Frequency Characteristics	G_{fy}	Vo(7MHz)/Vo(1MHz)	−1.0	0	+1.0	dB
C Frequency Characteristics	G_{fc}	Vo(7MHz)/Vo(1MHz)	−1.0	0	+1.0	dB
Differential Gain	DG	Stea Step	—	—	3.0	%
Differential Phase	DP	Stea Step	—	—	3.0	deg
Output offset Voltage	Vos		−15.0	0	+15.0	mV
Y Cross-Talk	CT_y	4.43MHz Vo/vi	—	−60.0	−50.0	dB
C-Y Cross-Talk	CT_{cy}	4.43MHz Vo/Vi	—	−60.0	−50.0	dB
Y-C Cross-Talk	CT_{yc}	4.43MHz Vo/Vi	—	−60.0	−50.0	dB
Input Impedance 1	R_{i1}	V_{in1}, V_{in2}	10.0	—	—	kΩ
Input Impedance 2	R_{i2}	C_{in}	—	15.0	—	kΩ
Output Impedance	Ro		—	20.0	—	ΩV
Charact-LEVEL 1	V_{M1}		607	643	679	mV
Charact-LEVEL 2	V_{M2}		607	643	679	mV
Y Gate Level	V_{gy}	From Crump Level	0	35.7	71.4	mV
C Gate Level	V_{GC}	From Bias Level	−10.0	0	10.0	
Threshold Voltage 1	V_{th1}	SW1 (ON LEVEL)	2.5	—	—	V
		(OFF LEVEL)	—	—	0.8	V
Threshold Voltage 2	V_{th2}	SW2 (ON LEVEL)	2.5	—	—	V
		(OFF LEVEL)	—	—	0.8	V
Threshold Voltage 3	V_{th3}	SW3 (ON LEVEL)	3.0	—	—	V
		(OFF LEVEL)	—	—	1.0	V
Threshold Voltage 4	V_{th4}	SW4 (ON LEVEL)	3.0	—	—	V
		(OFF LEVEL)	—	—	1.0	V
Threshold Voltage 5	V_{th5}	SW5 (ON LEVEL)	2.5	—	—	V
		(OFF LEVEL)	—	—	0.8	V
Threshold Voltage 6	V_{th6}	SW6 (ON LEVEL)	2.5	—	—	V
		(OFF LEVEL)	—	—	0.8	V
Threshold Voltage 7	V_{th7}	SW7 (ON LEVEL)	2.5	—	—	V
		(OFF LEVEL)	—	—	0.8	V

(note 1) Next two cross-talk (One side 0Ω termination)
① $V_{in1} \rightarrow V_{in2}$ ② $V_{in2} \rightarrow V_{in1}$

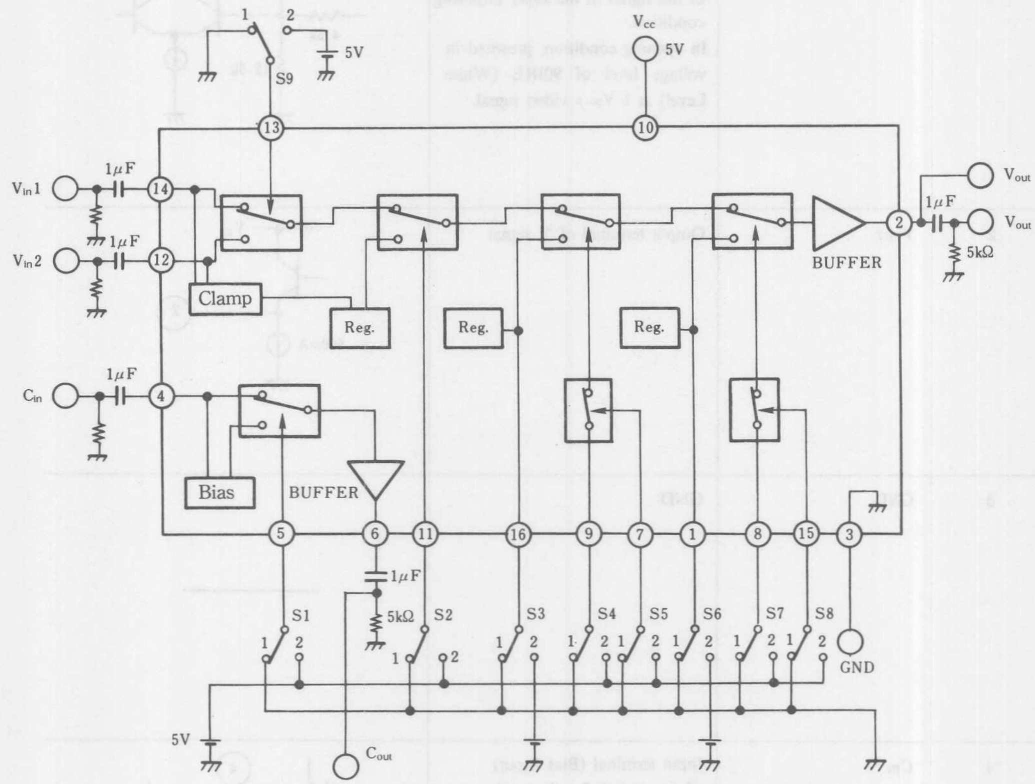
(note 2) Next two cross-talk (One side 0Ω termination)
① $C_{in} \rightarrow V_{in1}$ ② $C_{in} \rightarrow V_{in2}$

(note 3) Next two cross-talk (One side 0Ω termination)
① $V_{in1} \rightarrow C_{in}$ ② $V_{in2} \rightarrow C_{in}$

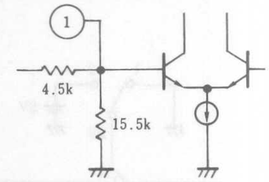
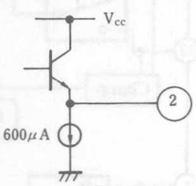
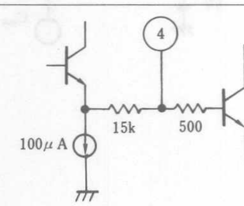
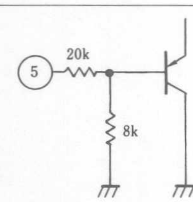
(note 4) White Level

(note 5) Black Level

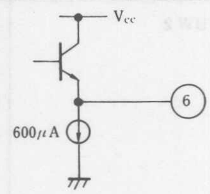
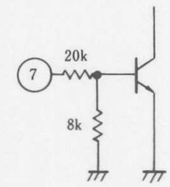
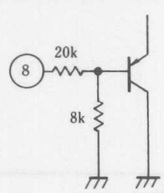
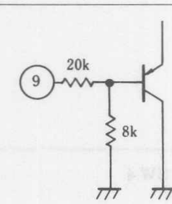
■ TEST CIRCUIT



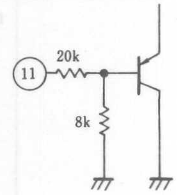
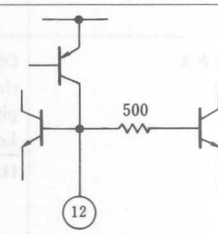
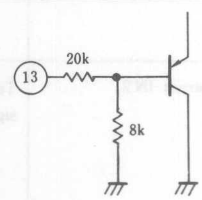
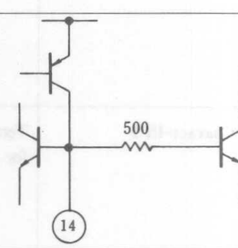
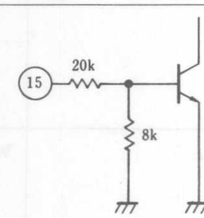
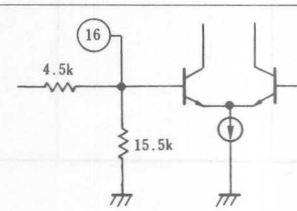
■ TERMINAL FUNCTION

PIN NO.	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	Charact-Level 2	Input terminal of the DC Voltage or the signal in the super imposing condition. In opening condition, presetted in voltage level of 90IRE (White Level) at 1 V_{P-P} video signal.	
2	V_{OUT}	Output terminal of Y signal	
3	GND	GND	
4	C_{IN}	Input terminal (Bias Input) of gate switch for C signal.	
5	Chroma-SW	Control Terminal of C-SW. L_O | Signal Output H_i | Bias Voltage Output	

■ TERMINAL FUNCTION

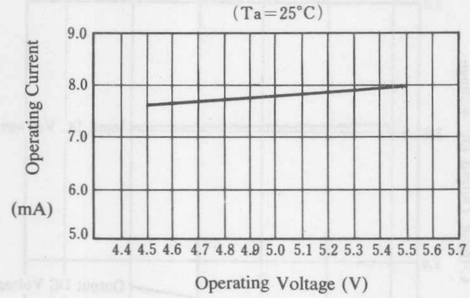
PIN NO	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
6	C_{OUT}	Output terminal of C-SW.	
7	SW 3	ON/OFF control terminal of character signal inputted from 9 pin L_O | Charactor Signal Through H_i | Charactor Signal OFF	
8	Charact-IN 2	Terminal to input character signal for super impose.	
9	Charact-IN 1	Terminal to input character signal for super impose.	
10	Vcc	$V_{cc}=5V$	

■ TERMINAL FUNCTION

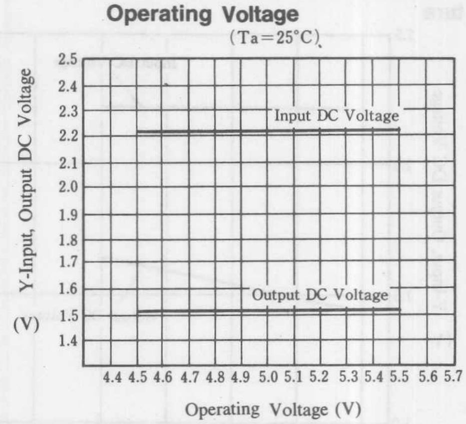
PIN NO.	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
11	SW 2	Terminal to input charactor signal for super impose. Voltage for impose is presetted internally, at the voltage level 5IRE (Black Level)with 1V_{P-P} video signal.	
12	V_{in} 2	Input terminal of Y signal(1$V_{P\text{-}P}$). Clamp circuit is internalized and clamp voltage is about 2.15V. (Oscillation might occur when higher impedance source. So, please control source impedance under 3.5Ω.)	
13	SW 1	Contorol terminal for input signal switch of Y signal. | | Output | | Lo | V_{in} 1 | | Hi | V_{in} 2 |	
14	V_{in} 1	Input terminal of Y signal (1$V_{P\text{-}P}$). Clamp circuit is internalized and clamp voltage is about 2.15V. (Oscillation migh occire when higher impedance source. So, please contorol source impedance under 3.5kΩ.)	
15	SW 4	ON/OFF control terminal of charactor signal inputted from 8 pin. Lo | Charactor Through Hi | Charactor Signal OFF	
16	Charact-Level 1		

■ TYPICAL CHARACTERISTICS

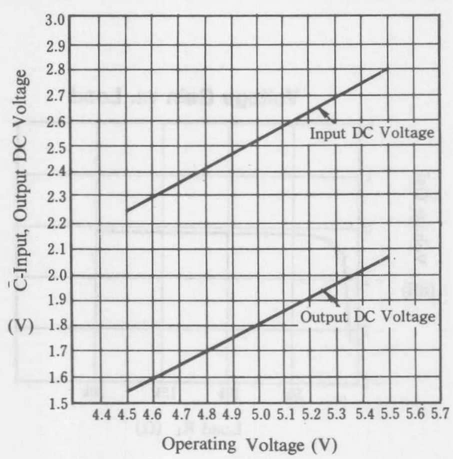
Operating Current vs. Operating Voltage



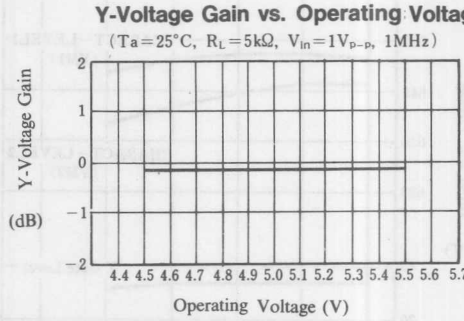
Y-Input, Output DC Voltage vs. Operating Voltage



C-Input, Output DC Voltage vs. Operating Voltage

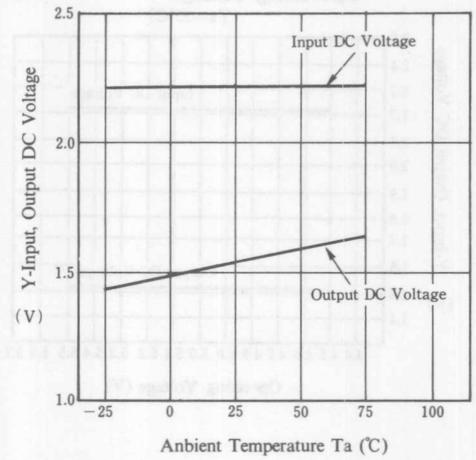


Y-Voltage Gain vs. Operating Voltage

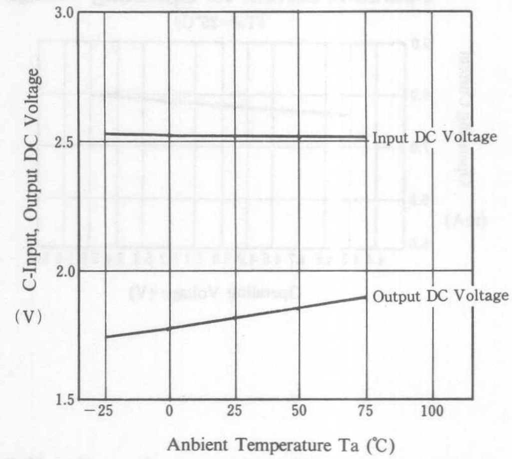


■ TYPICAL CHARACTERISTICS

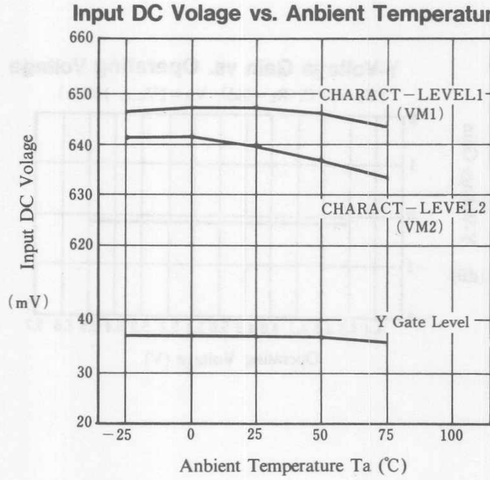
Y-Input, Output DC Voltage vs. Anbient Temperature



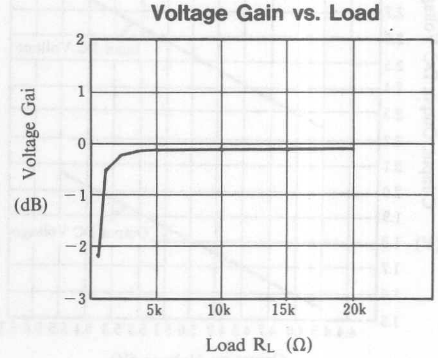
C-Input, Output DC Voltage vs. Anbient Temperature



Input DC Volage vs. Anbient Temperature



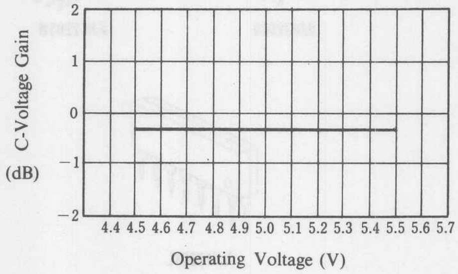
Voltage Gain vs. Load



■ TYPICAL CHARACTERISTICS

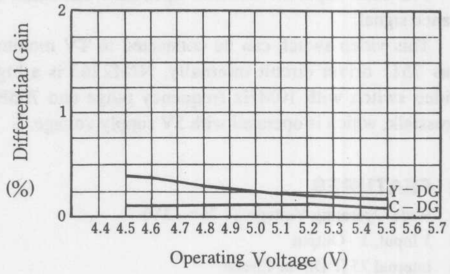
C-Voltage Gain vs. Operating Voltage

(Ta=25°C, R_L=5kΩ, V_{in}=1V_{P-P}, 1MHz)



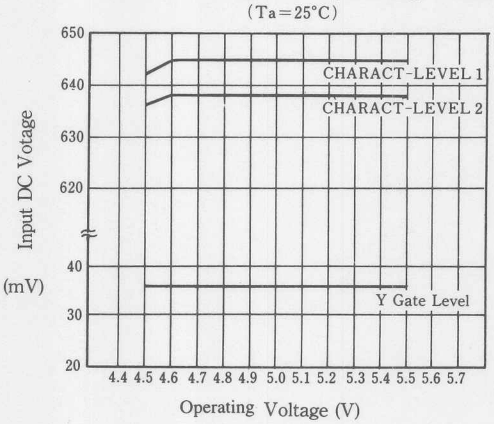
Differential Gain vs. Operating Voltage

(Ta=25°C, V_{IN}=1V_{P-P} Nomal Stea Case Pulse R_L=5kΩ)



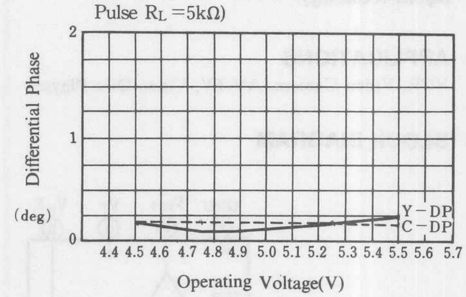
Input DC Votage vs. Operating Voltage

(Ta=25°C)

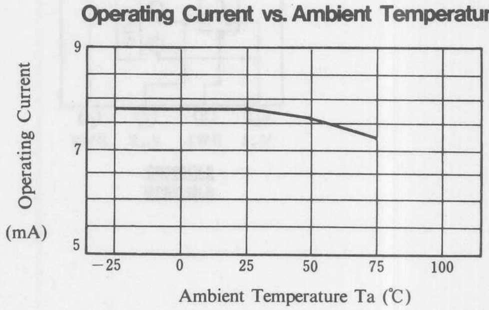


Differential Phase vs. Operating Voltage

(Ta=25℃, VIN=1V_{P-P} Normal Stea Case Pulse R_L=5kΩ)



Operating Current vs. Ambient Temperature



3-INPUT VIDEO SUPER IMPOSER WITH 75Ω DRIVER

■ GENERAL DESCRIPTION

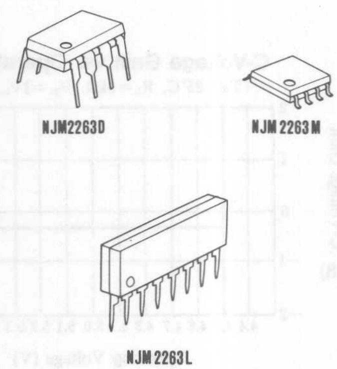
NJM2263 is 3-input, 1-output video switch with 75Ω driver circuit.

Two input are provided with sink chip clamp function, which adjust the DC level of video sighal.

The other input of transistor open base can make control of luminance signal.

This video switch can be connected to TV monitor directly, as it has 75Ω driver circuit internally. NJM2263 is a high performance video switch with 10MHz frequency range and 70dB (at 4.43MHz) crosstalk, which is operated with 5V supply voltage.

■ PACKAGE OUTLINE



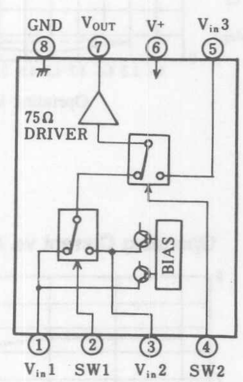
■ FEATURES

- Wide Operating Voltage (4.75～13V)
- 3 Input, 1 - Output
- Internal 75Ω Driver Circuit
- Internal Sink Chip Clamp Function ($V_{IN}1$, $V_{IN}2$)
- Internal luminance Signal Control Function ($V_{IN}3$)
- Crosstalk 70dB(at 4.43MHz)
- Wide Operating Frequency Range 10MHz($2V_{P-P}$ input)
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

■ APPLICATIONS

- VCR, Video Camera, AV-TV, Video Disc Player.

■ BLOCK DIAGRAM



NJM2263D
NJM2263M

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DIP8) 500 (DMP8) 300 (SIP8) 800	mW mW mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25±2℃)

PARAMETERS	SYMBOLS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage	V^+		4.75	—	13.0	V
Operating Current	I_{CC}	S1=S2=S3=S4=S5=2	—	16.5	23.0	mA
Voltage Gain	G_V	V_{in}=2.0V_{P-P}, 100kHz V_o/V_i	−0.8	−0.3	+0.2	dB
Frequency Characteristics	G_f	V_{in}=2.0V_{P-P}, V_o(10MHz)/V_o(100kHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_{in}=2.0V_{P-P}, Staircase, R_L=150Ω	—	0.3	—	%
Differential Phase	DP	V_{in}=2.0V_{P-P}, Staircase, R_L=150Ω	—	0.3	—	deg
Output Offset Voltage	V_{OS}	S1=S2=S3=2, S4=2 → 1	−30	0	+30	mV
Crosstalk	CT	V_i=2.0V_{P-P}, 4.43MHz V_o/V_i V_{in}3 Biased (note 2)		−70		dB
Switch change Voltage	V_{CH}	Switch High Level Voltage	2.4	—		
	V_{CL}	Switch Low Level Voltage	—	—	0.8	V

Note 1) Unless otherwise specified, tested with the following conditions.
a) S1=1 S2=S3=S4=S5=2 b) S2=S4=1, S1=S3=S5=2 c) S3=S5=1, S1=S2=1, S4=1 or 2

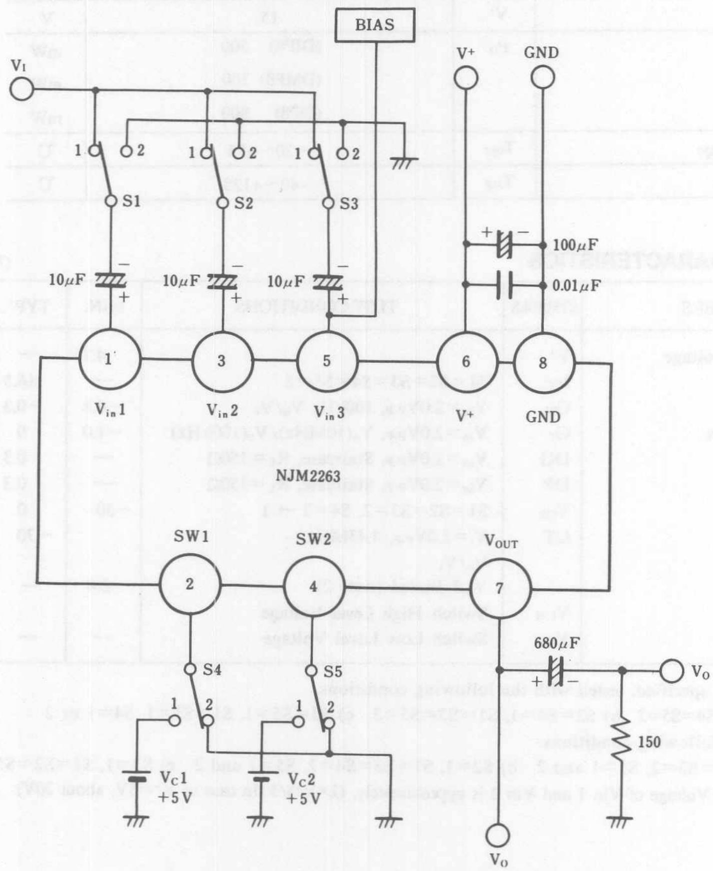
Note 2) Tested with the following conditions.
a) S1=S4=1, S2=S3=2, S5=1 and 2 b) S2=1, S1=S3=S4=2, S5=1 and 2 c) S3=1, S1=S2=S5=2, S4=1 and 2

Note 3) The Clamp Input Voltage of Vin 1 and Vin 2 is approximately, $(2\times V^+)/5$.(In case of V^+=5V, about 20V)

■ SWITCH CONTROL SIGNAL-OUTPUT SIGNAL

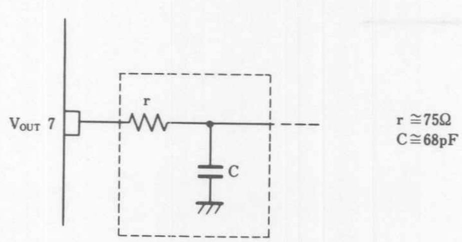
SW1	SW2	OUTPUT SIGNAL
L	L	$V_{in}1$
H	L	$V_{in}2$
L/H	H	$V_{in}3$

■ TEST CIRCUIT

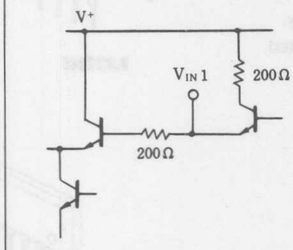
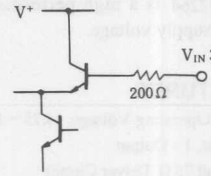
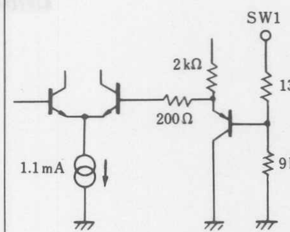
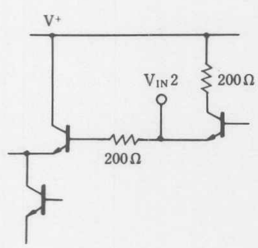
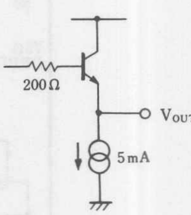
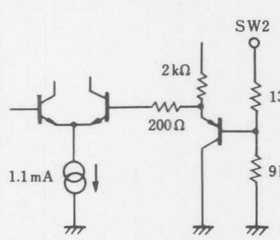


■ APPLICATION

Oscillation Prevention on light loading conditions
Recommended under circuit



■ EQUIVALENT CIRCUIT

PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT	PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	V_{IN} 1		5	V_{IN} 3	
2	SW 1		6	V⁺	
3	V_{IN} 2		7	V_{OUT}	
4	SW 2		8	GND	

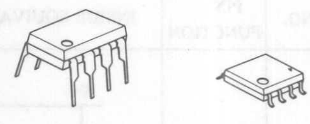
3-INPUT VIDEO SUPER IMPOSER WITH 75Ω DRIVER

■ GENERAL DESCRIPTION

NJM2264 is 3-input, 1-output video switch with 75 Ω driver circuit. One input is provided with sink chip clamp function, which adjusts the DC level of video sighal. The other two inputs of transistor open base can make control of luminance signal. This video switch can be connected to TV monitor directly, as it has 75 Ω driver circuit internally.

NJM2264 is a high performance video switch which is operated with 5V supply voltage.

■ PACKAGE OUTLINE



NJM2264D NJM2264M

NJM2264L

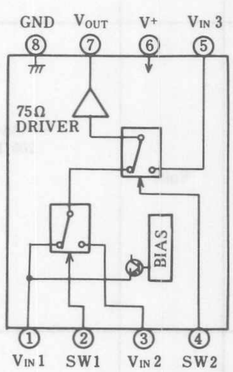
■ FEATURES

- Wide Operating Voltage (4.75 ~ 13V)
- 3 Input, 1 - Output
- Internal 75 Ω Driver Circuit
- Internal Sink Chip Clamp Function ($V_{IN}1$)
- Internal Luminance Signal Control Function ($V_{IN}2$, $V_{IN}3$)
- Crosstalk 70dB(at 4.43MHz)
- Wide Operating Frequency Range 10MHz($2V_{P-P}$ input)
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

■ APPLICATIONS

- VCR, Video Camera, AV-TV, Video Disc Player.

■ BLOCK DIAGRAM



NJM2264D
NJM2264M

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(SIP8) 800	mW
Operating Temperature Range	T_{opr}	−20∼+75	℃
Storage Temperature Range	T_{stg}	−40∼+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25°C±2°C)

PARAMETERS	SYMBOLS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage	V^+		4.75	—	13.0	V
Operating Current	I_{CC}	S1=S2=S3=S4=S5=2	—	16.5	23.0	mA
Voltage Gain	G_V	V_{IN}=2.0V_{P-P}, 100kHz, V_O/V_I	−0.8	−0.3	+0.2	dB
Frequency Characteristics	G_f	V_{IN}=2.0V_{P-P}, V_O(10MHz)/V_O(100kHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_{IN}=2.0V_{P-P} Staircase, R_L=150Ω	—	0.3	—	%
Differential Phase	DP	V_{IN}=2.0V_{P-P} Staircase, R_L=150Ω	—	0.3	—	deg
Crosstalk	CT	V_I=2.0V_{P-P}, 4.43MHz V_O/V_1 $V_{IN}2$ $V_{IN}3$ Biased (Note 2)	—	−70	—	dB
Switch Change Voltage	V_{CH}	Switch High Level Voltage	2.4	—	—	V
	V_{CL}	Switch Low Level Voltage	—	—	0.8	V

Note 1) Unless otherwise specified, tested with the following conditions.
a) S1=1, S2=S3=S4=S5=2 b) S2=S4=1, S1=S3=S5=2 c) S3=S5=1, S1=S2=1, S4=1 and 2

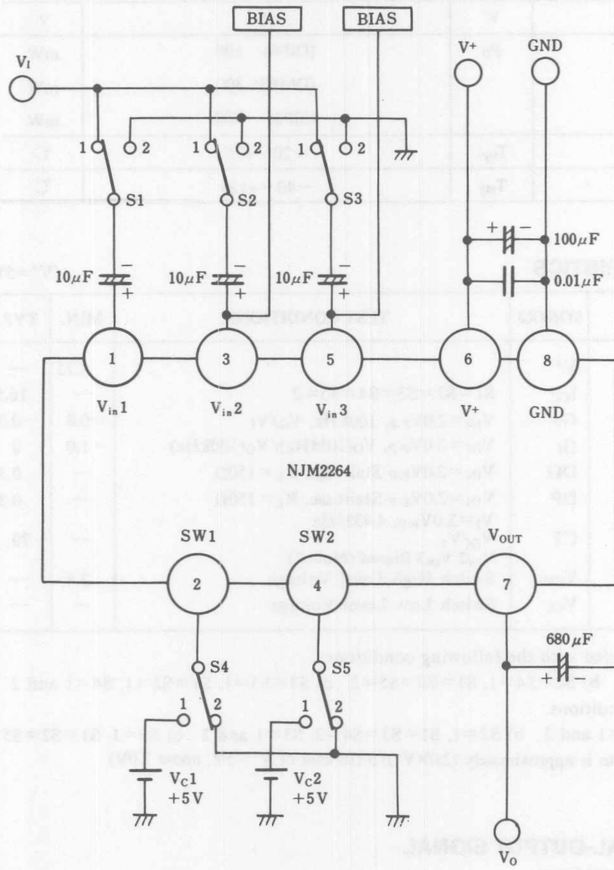
Note 2) Tested with the following conditions.
a) S1=S4=1, S2=S3=2, S5=1 and 2 b) S2=1, S1=S3=S4=2, S5=1 and 2 c) S3=1, S1=S2=S5=2, S4=1 and 2

Note 3) The Clamp Input Voltage of Vin is approximately (2.0×V^+)/5 (In case of V^+=5V, about 2.0V)

■ SWITCH CONTROL SIGNAL-OUTPUT SIGNAL

SW 1	SW 2	OUTPUT SIGNAL
L	L	V_{IN} 1
H	L	V_{IN} 2
L/H	H	V_{IN} 3

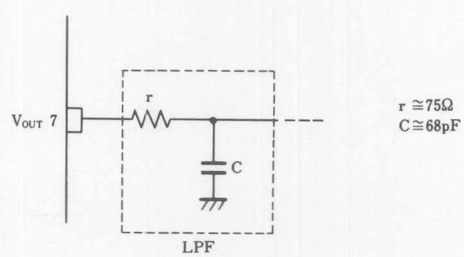
■ TEST CIRCUIT



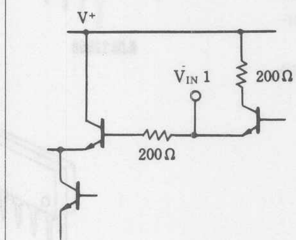
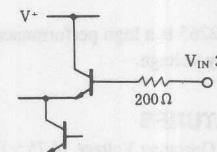
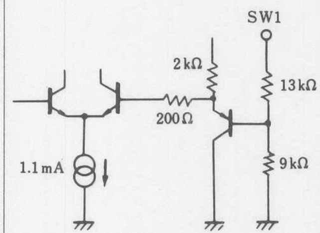
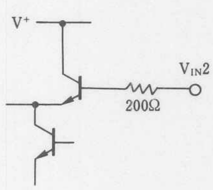
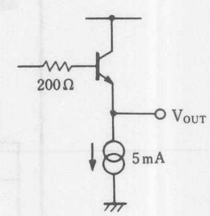
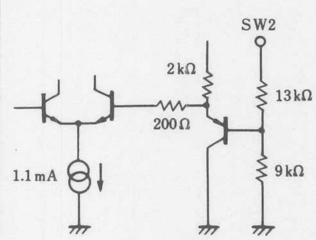
■ APPLICATION

Oscillation Prevention on light loading conditions

Recommended under circuit



■ EQUIVALENT CIRCUIT

PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT	PIN NO.	PIN FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	V_{IN} 1		5	V_{IN} 3	
2	SW 1		6	V^+	
3	V_{IN} 2		7	V_{OUT}	
4	SW 2		8	GND	

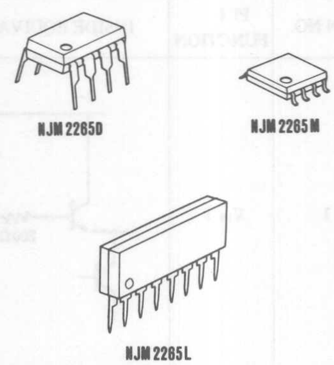
3-INPUT VIDEO SUPER IMPOSER WITH 6dB AMPLIFIER

■ GENERAL DESCRIPTION

NJM2265 is 3-input, 1-output video switch with 6dB amplifier. Two inputs are provided with sink chip clamp function which adjust the DC level of video sighal. The other input of transistor open base can make control of luminance signal. This video switch can be connected to TV monitor directly, as it has 6dB amplifier circuit internally.

NJM2265 is a high performance video switch which is operated with 5V supply voltage.

■ PACKAGE OUTLINE



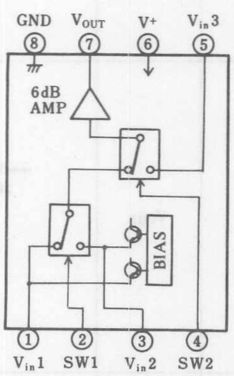
■ FEATURES

- Wide Operating Voltage (4.75~13V)
- 3 Input, 1 - Output
- Internal 6 dB Amplifier Circuit
- Internal Sink Chip Clamp Function ($V_{IN}1$, $V_{IN}2$)
- Internal Luminance Signal Control Function ($V_{IN}3$)
- Crosstalk 65dB(at 4.43MHz)
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

■ APPLICATIONS

- VCR, Video Camera, AV-TV, Video Disc Player.

■ BLOCK DIAGRAM



NJM2265D
NJM2265M

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(SIP8) 800	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25±2℃)

PARAMETERS	SYMBOLS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage	V^+		4.75	—	13.0	V
Operating Current	I_{CC}	S=1=S2=S3=S4=S5=2	—	15	21.0	mA
Voltage Gain	G_V	V_{in}=1.0V_{P-P}, 1MHz, V_O/V_I	5.7	6.2	6.7	dB
Frequency Characteristics	G_f	V_{in}=1.0V_{P-P}, V_O(5MHz)/V_O(1MHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_{in}=1.0V_{P-P}, Staircase, R_L=1kΩ	—	0.2	—	%
Differential Phase	DP	V_{in}=1.0V_{P-P}, Staircase, R_L=1kΩ	—	0.1	—	deg
Output Offset Voltage	V_{OS}	S1=S2=S3=2, S4=2→1 V_{in}=1.0V_{P-P}, 4.43MHz	−60	0	+60	mV
Crosstalk	CT	V_O/V_I Vin3 Biased (note 2)	—	−65	—	dB
Switch Change Voltage	V_{CH}	Switch High Level Voltage	2.4	—	—	V
Switch High Level Voltage	V_{CL}	Switch Low Level Voltage	—	—	0.8	V

Note 1 Unless otherwise specified, tested with the following conditions.
a) S1=1, S2=S3=S4=S5=2 b) S2=S4=1, S1=S3=S5=2 c) S3=S5=1, S1=S2=1, S4=1 or 2

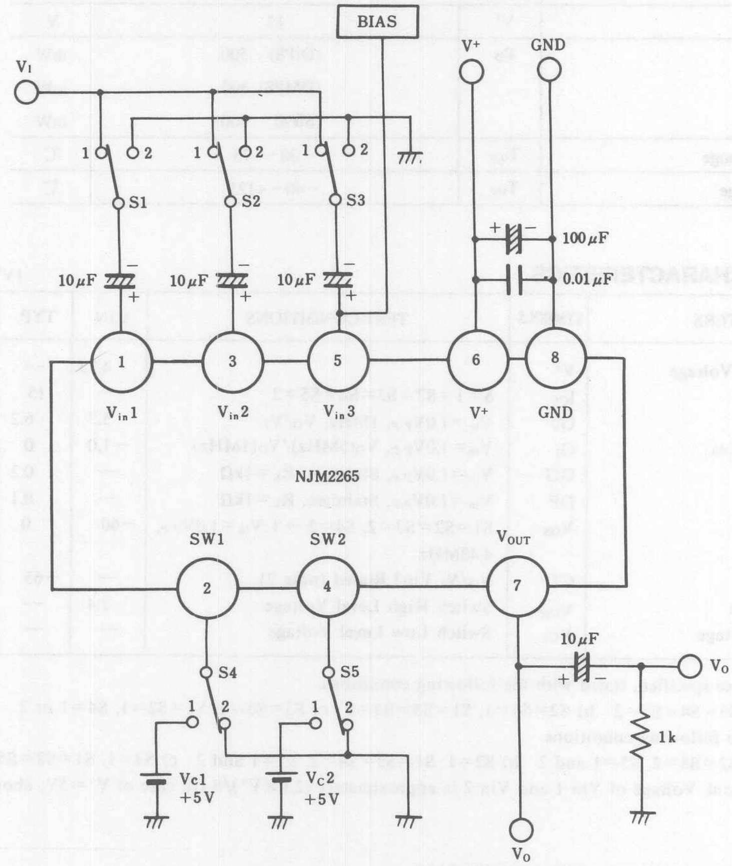
Note 2 Tested with the following conditions.
a) S1=S4=1, S2=S3=2, S5=1 and 2 b) S2=1, S1=S3=S4=2, S5=1 and 2 c) S3=1, S1=S2=S5=2, S4=1 and 2

Note 3 The Clamp Input Voltage of Vin 1 and Vin 2 is approximately (2.1×V^+)/5 (In case of V^+=5V, about 2.1V)

■ SWITCH CONTROL SIGNAL-OUTPUT SIGNAL

SW1	SW2	OUTPUT SIGNAL
L	L	V_{in}1
H	L	V_{in}2
L/H	H	V_{in}3

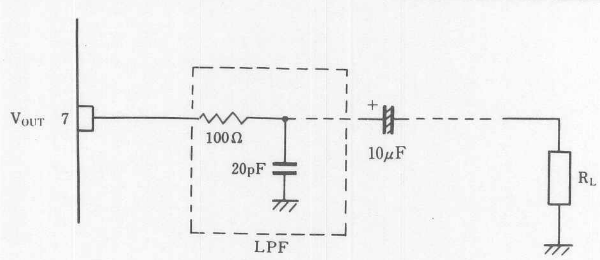
■ TEST CIRCUIT



■ APPLICATION

Oscillation Prevention

It is much effective to insert LPF (Cutoff Frequency 70MHz) under light loading conditions (R_L 》 1kΩ)

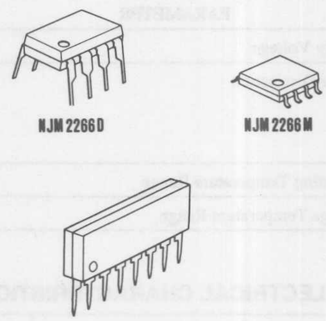


3-INPUT VIDEO SUPER IMPOSER WITH 6dB AMPLIFIER

■ GENERAL DESCRIPTION

NJM2266 is 3-input, 1-output video switch with 6dB amplifier. One input is provided with sink chip clamp function, which adjust the DC level of video sighal. The other two inputs of transistor open base can make control of luminance signal. This video switch can be connected to TV monitor directly, as it has 6dB amplifier circuit internally. NJM2266 is a high performance video switch with is operated 4.75V supply voltage.

■ PACKAGE OUTLINE



NJM2266D NJM2266M

NJM2266L

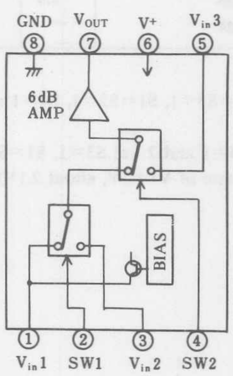
■ FEATURES

- Wide Operating Voltage (4.75~13V)
- 3 Input, 1 - Output
- Internal 6 dB Amplifier Circuit
- Internal Sink Chip Clamp Function ($V_{IN}1$)
- Internal Luminance Signal Control Function ($V_{IN}2$, $V_{IN}3$)
- Crosstalk 65dB(at 4.43MHz)
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

■ APPLICATIONS

- VCR, Video Camera, AV-TV, Video Disc Player.

■ BLOCK DIAGRAM



NJM2266D
NJM2266M

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	(DIP8) 500 (DMP8) 300 (SIP8) 800	mW mW mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25±2℃)

PARAMETERS	SYMBOLS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage	V^+		4.75		13.0	V
Operating Current	I_{CC}	S1=S2=S3=S4=S5=2	—	15	21.0	mA
Voltage Gain	G_V	V_{in}=1.0V_{P-P}, 1MHz, V_o/V_i	5.7	6.2	6.7	dB
Frequency Characteristics	G_f	V_{in}=1.0V_{P-P}, V_o(5MHz)/V_o(1MHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_{in}=1.0V_{P-P}, Staircase, R_L=1kΩ	—	0.2	—	%
Differential Phase	DP	V_{in}=1.0V_{P-P}, Staircase, R_L=1kΩ	—	0.1	—	deg
Crosstalk	CT	V_o/V_i V_{in}2, V_{in}3−Biased (Note 2)	—	−65	—	dB
Switch Change Voltage	V_{CH}	Switch High Level Voltage	2.4	—	—	V
	V_{CL}	Switch Low Level Voltage	—	—	0.8	V

Note 1) Unless otherwise specified, tested with the following conditions.
a) S1=1, S2=S3=S4=S5=2 b) S2=S4=1, S1=S3=S5=2 c) S3=S5=1, S1=S2=1, S4=1 and 2

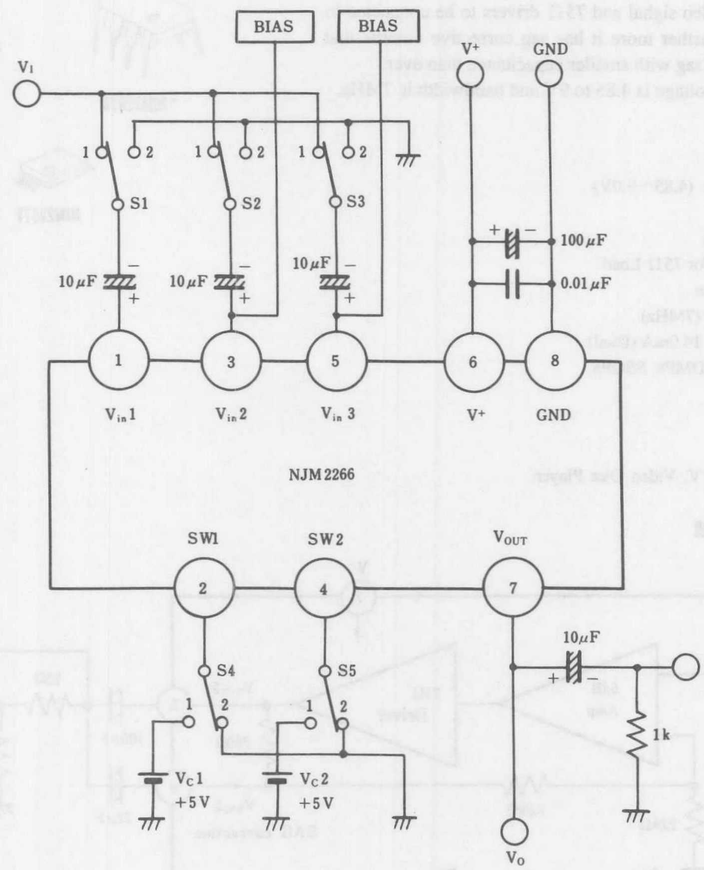
Note 2) Tested with the following conditions.
a) S1=S4=1, S2=S3=2, S5=1 and 2 b) S2=1, S1=S3=S4=2, S5=1 and 2 c) S3=1, S1=S2=S5=2, S4=1 and 2

Note 3) The clamp Input voltage of Vin1 is approximately (2.1×V^+)/5 (In case of V^+=5V, about 2.1V)

■ SWITCH CONTROL SIGNAL-OUTPUT SIGNAL

SW1	SW2	OUTPUT SIGNAL
L	L	$V_{in}1$
H	L	$V_{in}2$
L/H	H	$V_{in}3$

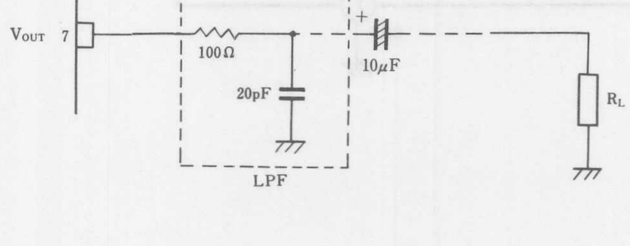
■ **TEST CIRCUIT**



■ **APPLICATION**

Oscillation Prevention

It is much effective to insert LPF(Cutoff Frequency 70 MHz) under light loading conditions ($R_L \gg 1k\Omega$)

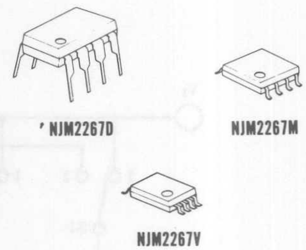


■ GENERAL DESCRIPTION

NJM2267 is a dual video 6dB amplifier with 75Ω drivers for S-VHS VCRs, HI-BAND VCRs, etc..Each channel has clamp function that fixes DC level of video sighal and 75Ω drivers to be connected to TV monitors directly. Further more it has sag corrective circuits that prevent the generation of sag with smaller capacitance than ever.

Its operating supply voltage is 4.85 to 9V and bandwidth is 7MHz.

■ PACKAGE OUTLINE



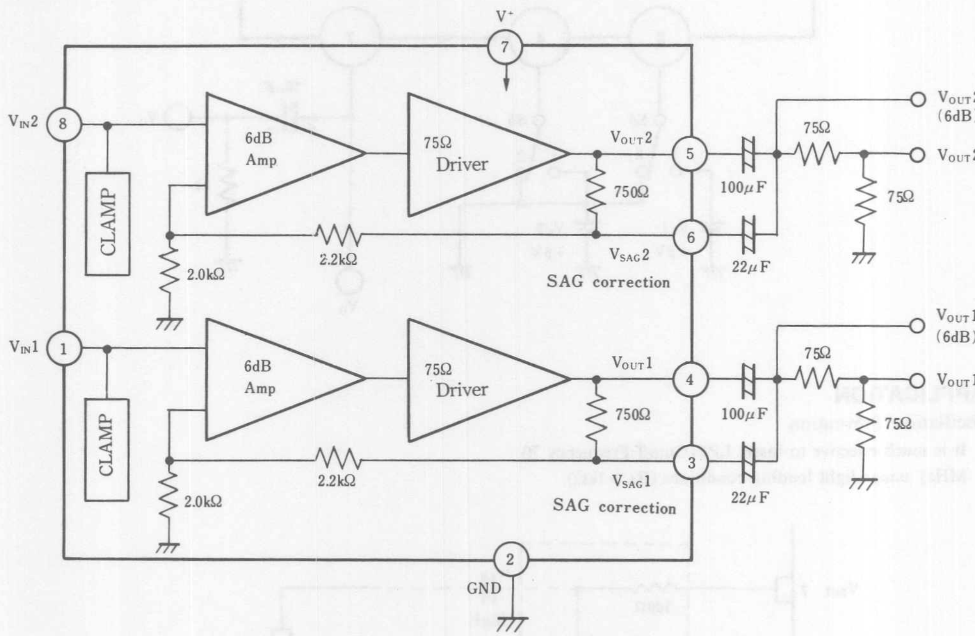
■ FEATURES

- Wide Operating Voltage (4.85～9.0V)
- Dual Channel
- Internal Clamp Function
- Internal Driver Circuit For 75Ω Load
- SAG Corrective Function
- Wide Frequency Range (7MHz)
- Low Operating Current 14.0mA (Dual)
- Package Outline DIP8, DMP8, SSOP8
- Bipolar Technology

■ APPLICATIONS

- VCR, Video Camera, TV, Video Disc Player

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	10	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(SSOP8) 250	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

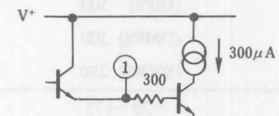
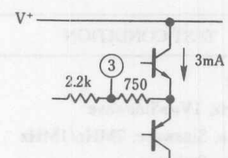
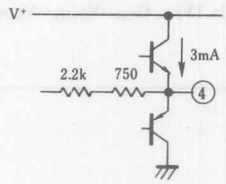
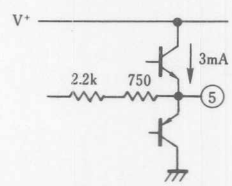
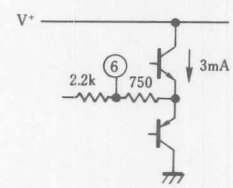
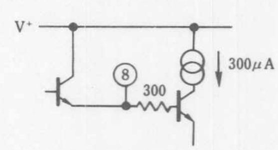
■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25±2℃)

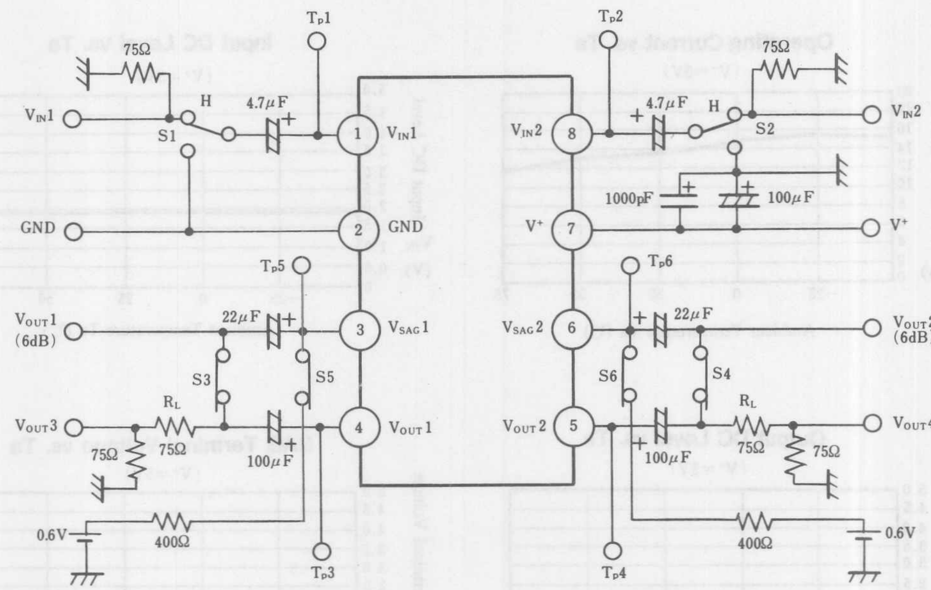
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	No Signal	—	14.0	18.2	mA
Voltage Gain	G_V	V_{IN}=1MHz, $1V_{P-P}$Sinewave	5.7	6.2	6.7	dB
Frequency Characteristic	G_f	$V_{IN}=1V_{P-P}$, Sinewave, 7MHz/1MHz	—	—	±1.0	dB
Differentail Gain *	DG	$V_{IN}=1V_{P-P}$, Staircase	—	1.0	3.0	%
Differentail Phase *	DP	$V_{IN}=1V_{P-P}$, Staircase	—	1.0	3.0	deg
Crosstalk	CT	V_{IN}=4.43MHz, $1V_{P-P}$, Sinewave	—	−70	—	dB
Gain Offset	G_{CH}	V_{IN}=1MHz, $1V_{P-P}$, $G_{CH}=V_{OUT1}-V_{OUT2}$	—	—	±0.5	dB
Input Clamp Voltage	V_{CL}		1.79	1.91	2.03	V
SAG Terminal Gain	G_{SAG}		35	45	—	dB

■ TERMINAL FUNCTION

(V⁺=5.0V, Ta=25℃)

PIN No.	PIN NAME	SYMBOL	EQUIVALENT CIRCUIT	FUNCTIONS
1	Input Clamp Terminal	V_{IN1}		Input terminal of $1V_{P-P}$ composite signal or Y signal. Clamp level is 1.9V
2	GND	GND		Ground
3	SAG correction	V_{SAG1}		SAG caused by a coupling capacitor of the output can be prevented by connecting this tarminal with the output terminal through an external capacitor.(see block diagram) When SAG correcting function is not necessary, this terminal must be connected with pin "4" directly.
4	Video Output1	V_{OUT1}		Output terminal that can drive 75Ω line.
5	Video Output2	V_{OUT2}		Output terminal that can drive 75Ω line.
6	SAG correction	V_{SAG2}		SAG caused by a coupling capacitor of the output can be prevented by connecting this terminal with the output terminal though an external capacitor.(see block diagram) When SAG correcting function is not necessary, this terminal must be connected with pin "5" directly.
7	V⁺	V⁺		Supply Voltage
8	Input Clamp Terminal	V_{IN2}		Input terminal of $1V_{P-P}$ composite signal or Y signal. Clamp level is 1.9V.

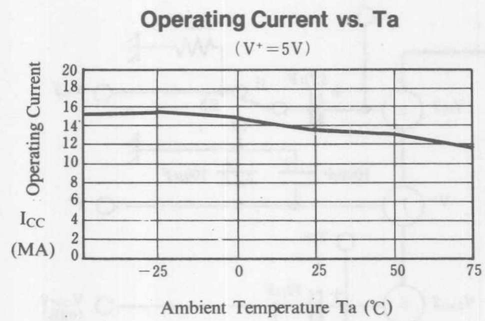
■ TEST CIRCUIT

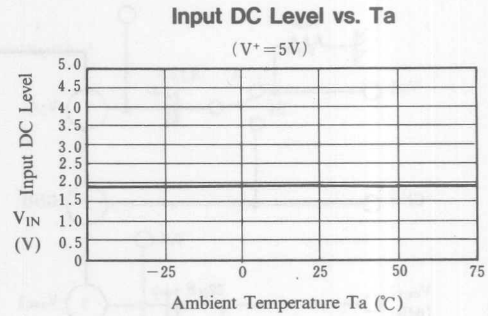


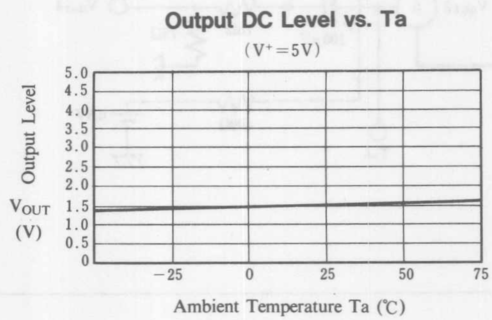
■ TEST METHODES

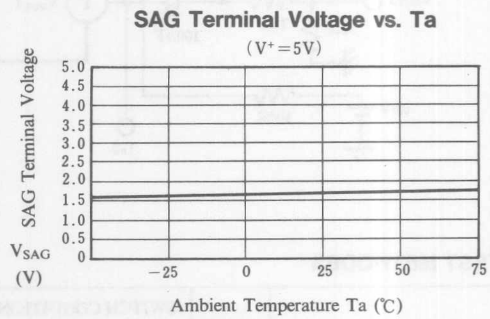
PARAMETER	SYMBOL	SWITCH CONDITIONS						CONDITIONS
		S1	S2	S3	S4	S5	S6	
Supply Voltage	I_{CC}	H	H					7PIN Sink Current
Voltage Gain	G_V	H	H	ON	ON			V_{OUT1}/V_{IN1}, V_{OUT2}/V_{IN2} at $V_{IN1}(V_{IN2})$=1MHz, $1V_{P-P}$, Sinewave
Frequency Characteristic	G_f	H	H	ON	ON			G_{V1M}; Voltage Gain at $V_{IN1}(V_{IN2})$=1MHz, $1V_{P-P}$ G_{V10M}; Voltage Gain at $V_{IN1}(V_{IN2})$=10MHz, $1V_{P-P}$ $G_f = G_{V10M} - G_{V1M}$
Differential Gain	DG	H	H	ON	ON			Measuring V_{OUT3} at V_{IN1}=Staircase Signal
Differential Phase	DP	H	H	ON	ON			Measuring V_{OUT3} at V_{IN1}=Staircase Signal
Crosstalk	CT	H	L	ON	ON			V_{OUT2}/V_{OUT1} at V_{IN1}=4.43MHz, $1V_{P-P}$, Sinewave V_{OUT1}/VIN2 at V_{IN2}=4.43MHz, $1V_{P-P}$, Sinewave
Gain Offset	G_{CH}	H	H	ON	ON			$G_{V1}=V_{OUT1}/V_{IN1}$, $G_{V2}=V_{OUT2}/V_{IN2}$ $G_{CH}=G_{V1}-G_{V2}$
Input Clamp Voltage	V_{CL}	H	H					Measuring at TP1(TP2)

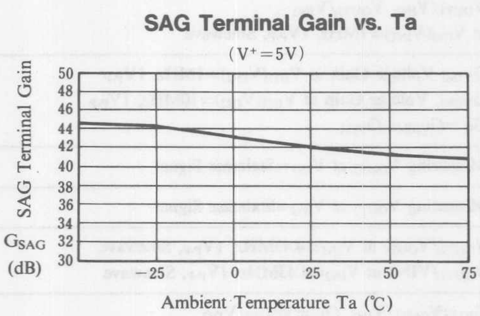
■ TYPICAL CHARACTERISTICS

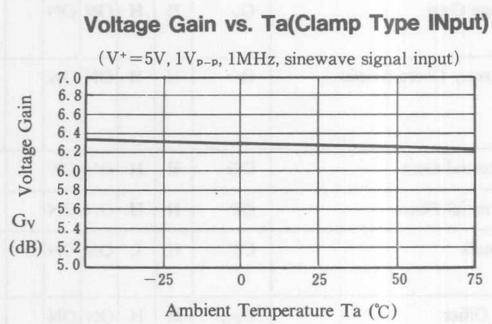








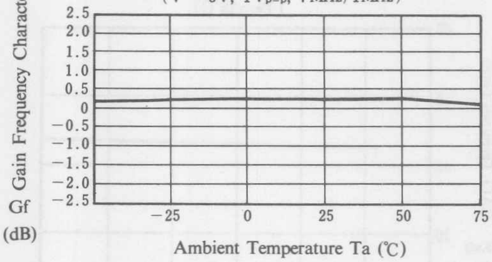




■ TYPICAL CHARACTERISTICS

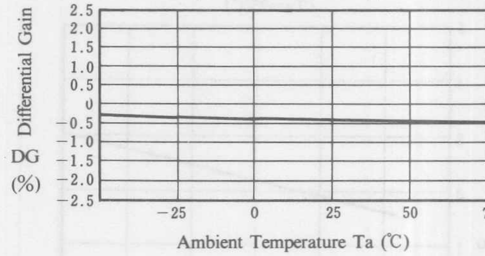
Gain Frequency Characteristics vs. Ta(Clamp Type Input)

($V^+=5V$, $1V_{P-P}$, 7MHz/1MHz)



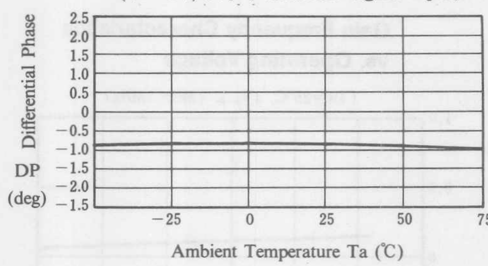
Differential Gain vs. Ta

($V^+=5V$, $1V_{P-P}$ staircase signal input)



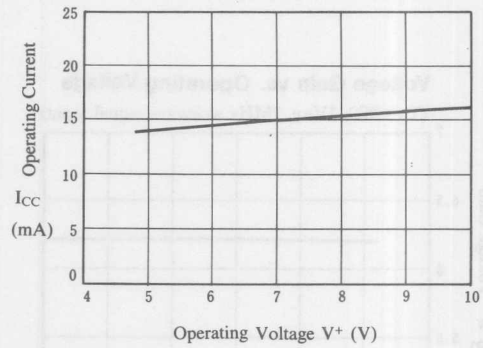
Differential Phase vs. Ta

($V^+=5V$, $1V_{P-P}$ staircase signal input)



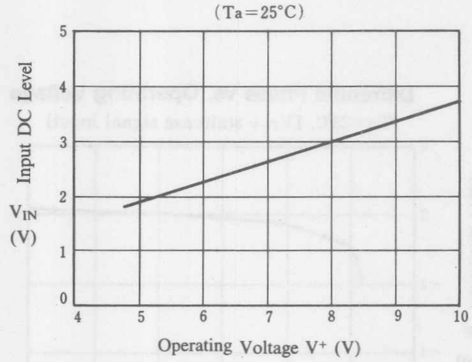
Operating Current vs. Operating Voltage

(Ta=25°C)



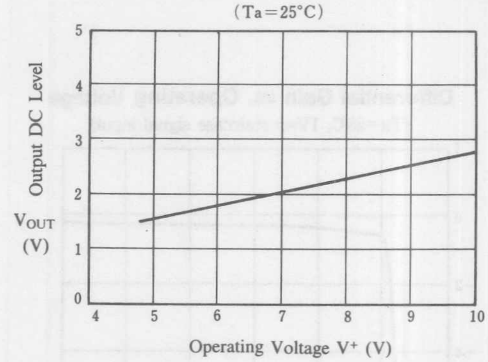
Input DC Level vs. Operating Voltage

(Ta=25°C)



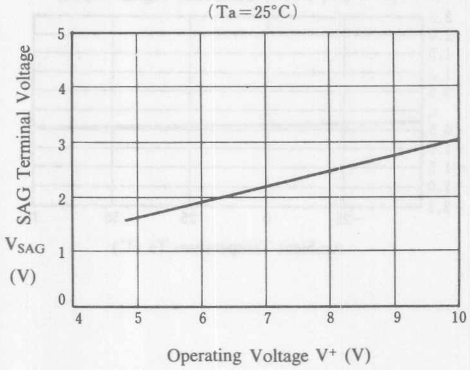
Output DC Level Vs. Operating Voltage

(Ta=25°C)

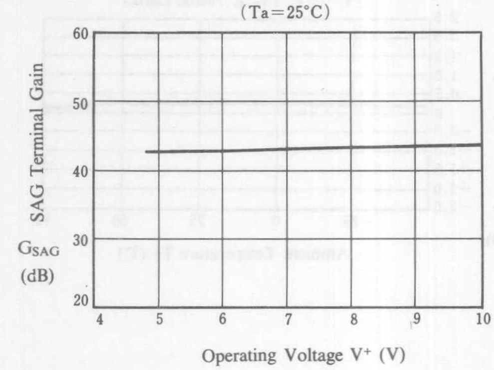


■ TYPICAL CHARACTERISTICS

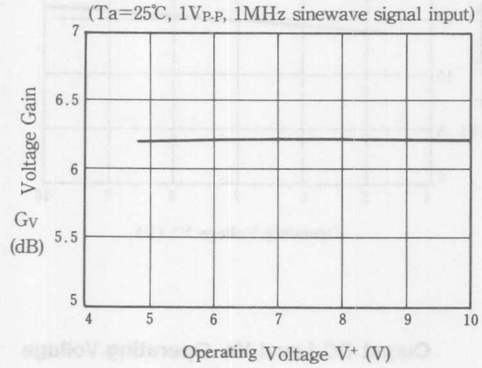
SAG Terminal Voltage vs. Operating Voltage
(Ta=25°C)



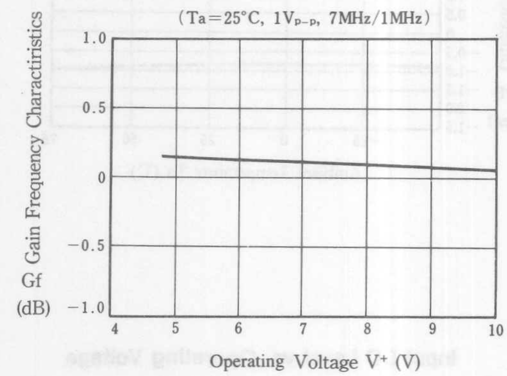
SAG Terminal Gain vs. Operating Voltage
(Ta=25°C)



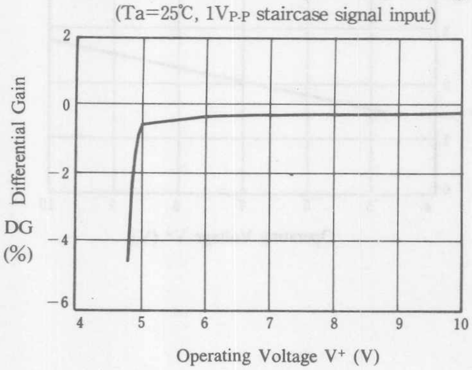
Voltage Gain vs. Operating Voltage
(Ta=25°C, $1V_{P\text{-}P}$, 1MHz sinewave signal input)



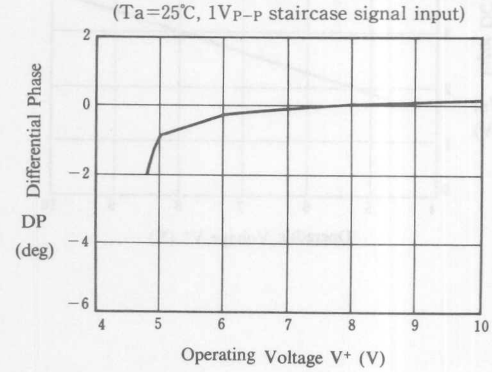
Gain Frequency Characteristics vs. Operating Voltage
(Ta=25°C, $1V_{P\text{-}P}$, 7MHz/1MHz)



Differential Gain vs. Operating Voltage
(Ta=25°C, $1V_{P\text{-}P}$ staircase signal input)



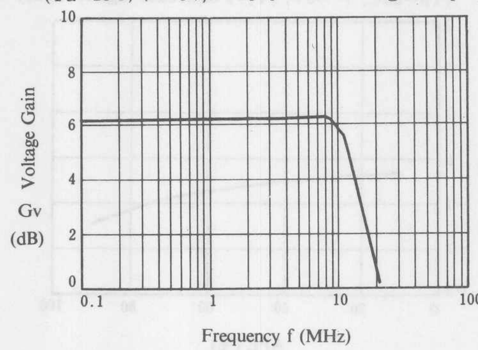
Diffrential Phase vs. Operating Voltage
(Ta=25°C, $1V_{P\text{-}P}$ staircase signal input)



■ TYPICAL CHARACTERISTICS

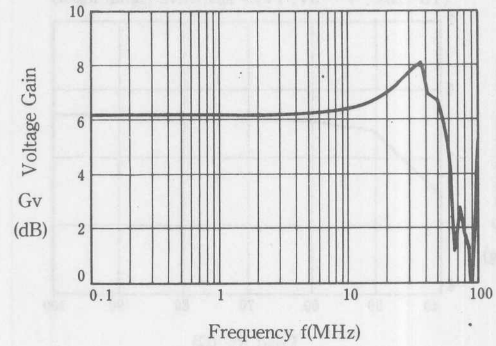
Voltage Gain vs. Frequency

(Ta=25℃, V+=5V, V1VP-P sinewave signal input)



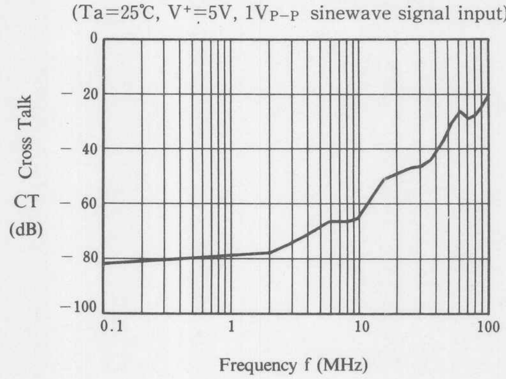
Small Signal Voltage Gain vs. Frequency

(Ta=25℃, V+=5VP-P, 25VP-P sinewave signal input)



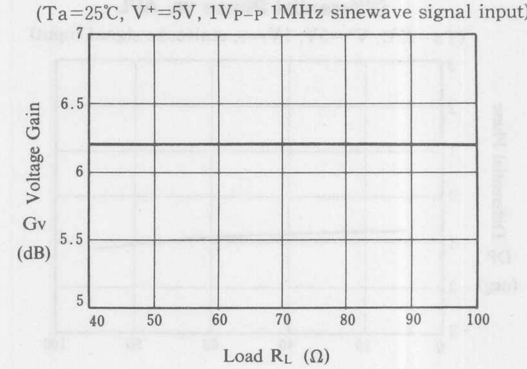
Cross Talk vs. Frequency

(Ta=25℃, V+=5V, 1VP-P sinewave signal input)



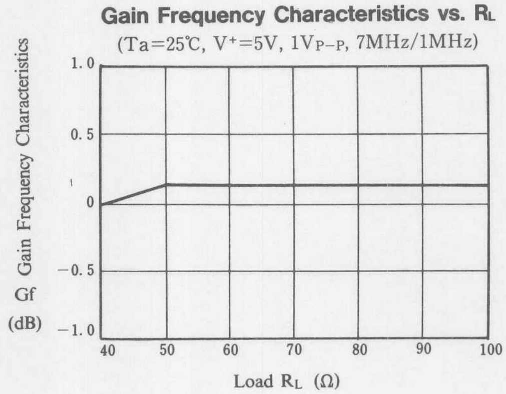
Voltage Gain vs. RL

(Ta=25℃, V+=5V, 1VP-P 1MHz sinewave signal input)



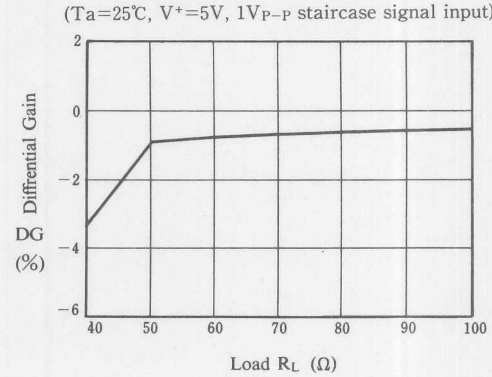
Gain Frequency Characteristics vs. RL

(Ta=25℃, V+=5V, 1VP-P, 7MHz/1MHz)



Differential Gain vs. RL

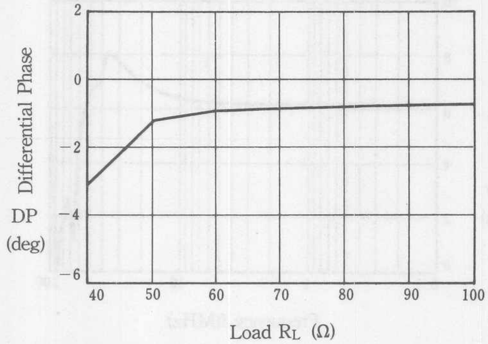
(Ta=25℃, V+=5V, 1VP-P staircase signal input)



■ **TYPICAL CHARACTERISTICS**

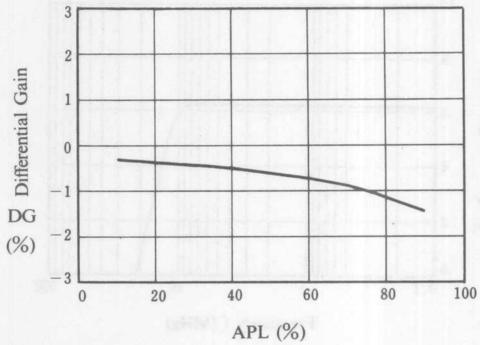
Differential Phase vs. R_L

($Ta=25°C$, $V^+=5V$, $1V_{P-P}$ sinewave signal input)



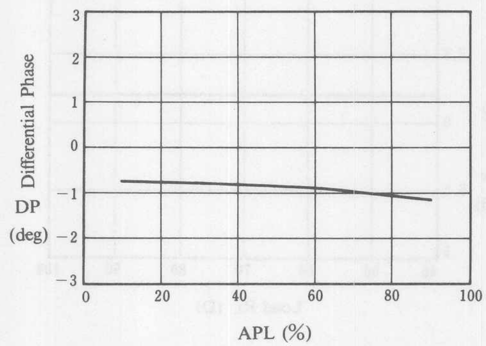
Differential Gain vs. APL

($Ta=25°C$, $V^+=5V$, $1V_{P-P}$ staircase signal input)



Differential Phase vs. APL

($Ta=25°C$, $V^+=5V$, $1V_{P-P}$, staircase signal input)



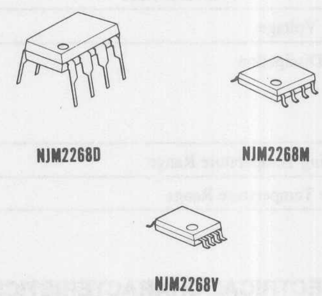
DUAL VIDEO 6dB AMPLIFIER WITH 75Ω DRIVER

■ GENERAL DESCRIPTION

NJM2268 is a dual video 6dB amplifier with 75Ω drivers for S-VHS VCRs, HI-BAND VCRs, etc..One channel has clamp function that fixes DC level of video sighal and another one is bias type. Furthermore it has 75Ω drivers to be connected to TV monitors directly and sag corrective circuits that prevent the generation of sag with smaller capacitance than ever.

Its operating supply voltage is 4.85 to 9V and bandwidth is 7MHz.

■ PACKAGE OUTLINE



■ FEATURES

- Wide Operating Voltage (4.85～9.0V)
- Dual Channel (Clamp Type, Bias Type)
- Internal Driver Circuit For 75Ω Load
- SAG Corrective Function
- Wide Frequency Range 7MHz
- Low Operating Current 14.0mA (Dual)
- Package Outline DIP8, DMP8, SSOP8
- Bipolar Technology

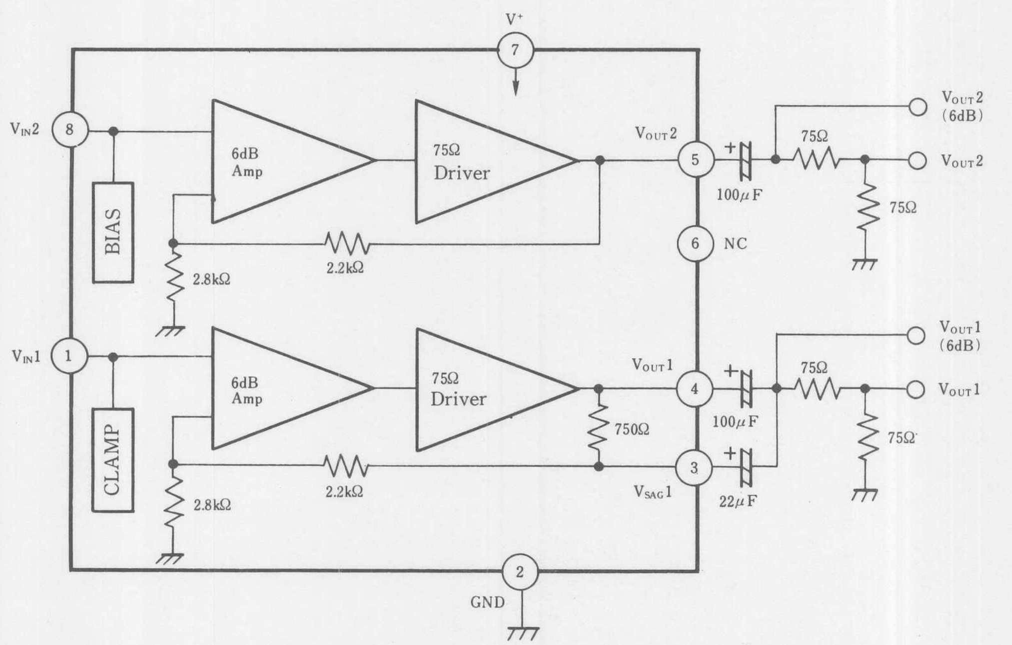
■ RECOMMENDED OPERATING CONDITION

- Supply Voltage V^+ 4.85~9.0V

■ APPLICATIONS

- VCR, Video Camera, TV, Video Disc Player

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	10	V
Power Dissipation	P_D	(DIP8) 500 (DMP8) 300 (SSOP8) 250	mW mW mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

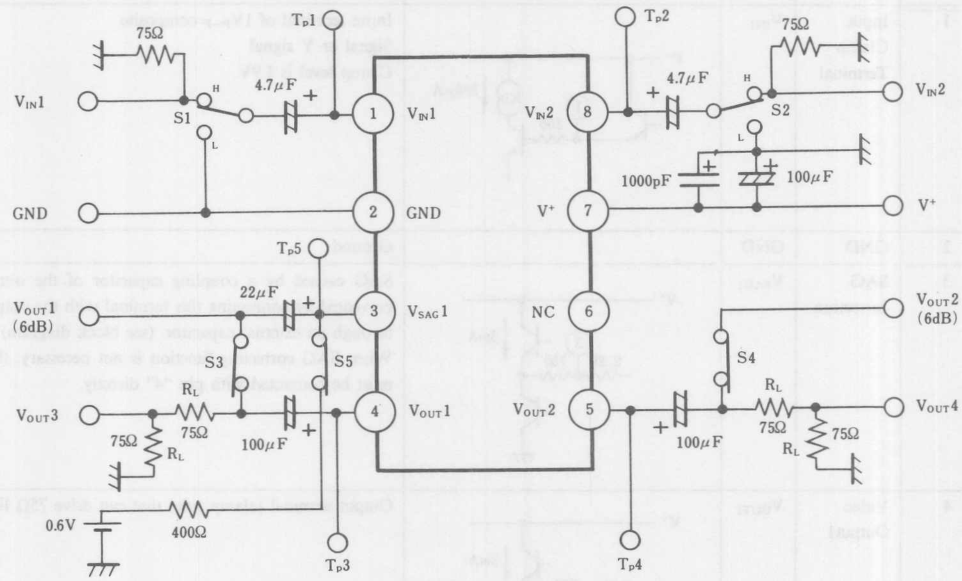
■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	No Signal	—	14.0	18.2	mA
Voltage Gain	G_V	V_{IN}=1MHz, $1V_{P-P}$Sinewave	5.7	6.2	6.7	dB
Frequency Characteristic	G_f	V_{IN}=$1V_{P-P}$, Sinewave, 7MHz/1MHz	—	—	±1.0	dB
Differentail Gain *	DG	V_{IN}=$1V_{P-P}$, Staircase	—	1.0	3.0	%
Differentail Phase *	DP	V_{IN}=$1V_{P-P}$, Staircase	—	1.0	3.0	deg
Crosstalk	CT	V_{IN}=4.43MHz, $1V_{P-P}$, Sinewave	—	−70		dB
Gain Offset	G_{CH}	V_{IN}=1MHz, $1V_{P-P}$, $G_{CH}=V_{OUT1}-V_{OUT2}$	—	—	±0.5	dB
Input Clamp Voltage	V_{CL}		1.79	1.91	2.03	V
Input Bias Voltage	V_{Bt}		2.56	2.84	3.12	V
SAG Terminal Gain	G_{SAG}		35	45	—	dB

NOTE: "*" is applied to clamp type input side only/

■ TEST CIRCUIT

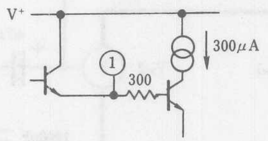
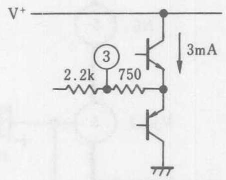
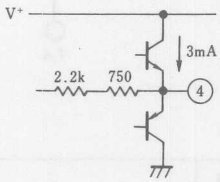
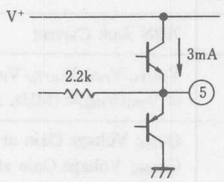
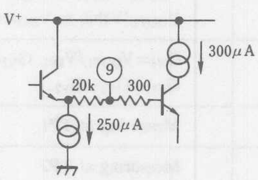


■ TEST METHODES

PARAMETER	SYMBOL	SWITCH CONDITIONS						CONDITIONS
		S1	S2	S3	S4	S5	S6	
Supply Voltage	$I_{CC}H$	H	H					7PIN Sink Current
Voltage Gain	G_V	H	H	ON	ON			V_{OUT1}/V_{IN1}, V_{OUT2}/V_{IN2} at $V_{IN1}(V_{IN2})$=1MHz, $1V_{P-P}$, Sinewave
Frequency Characteristic	G_f	H	H	ON	ON			G_{V1M}; Voltage Gain at $V_{IN1}(V_{IN2})$=1MHz, $1V_{P-P}$ G_{V10M}; Voltage Gain at $V_{IN1}(V_{IN2})$=10MHz, $1V_{P-P}$ $G_f = G_{V10M} - G_{V1M}$
Differential Gain	DG	H	H	ON	ON			Measuring V_{OUT3} at V_{IN1}=Staircase Signal
Differential Phase	DP	H	H	ON	ON			Measuring V_{OUT3} at V_{IN1}=Staircase Signal
Crosstalk	CT	H	L	ON	ON			V_{OUT2}/V_{OUT1} at V_{IN1}=4.43MHz, $1V_{P-P}$, Sinewave V_{OUT1}/VIN2 at V_{IN2}=4.43MHz, $1V_{P-P}$, Sinewave
Gain Offset	G_{CH}	H	H	ON	ON			$G_{V1}=V_{OUT1}/V_{IN1}$, $G_{V2}=V_{OUT2}/V_{IN2}$ $G_{CH}=G_{V1}-G_{V2}$
Input Clamp Voltage	V_{CL}	H	H					Measuring at TP1
Input Bias Voltage	V_{Bt}	H	H					Measuring at TP2
SAG Terminal Gain	G_{SAG}	H H	H H			 ON	 ON	TP3 Voltage; V_{O1A}, TP5 Voltage; V_{SO1A} TP3 Voltage; V_{O1B}, TP5 Voltage; V_{SO1B} G_{SAG}=20log $\{(V_{O1B}-V_{O1A})/(V_{SO1A}-V_{SO1B}\}$

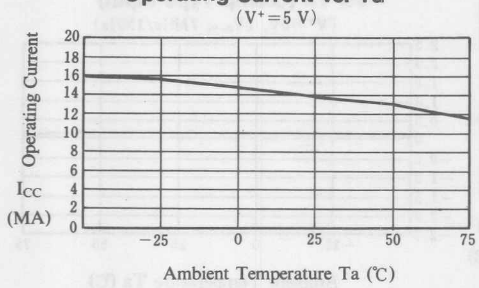
■ TERMINAL FUNCTION

(V^+=5.0V, Ta=25℃)

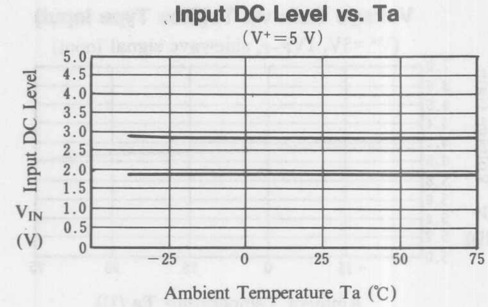
PIN No.	PIN NAME	SYMBOL	EQUIVALENT CIRCUIT	FUNCTIONS
1	Input Clamp Terminal	V_{IN1}		Input terminal of $1V_{P-P}$ composite Signal or Y signal Clamp level is 1.9V
2	GND	GND		Ground
3	SAG correction	V_{SAG1}		SAG caused by a coupling capacitor of the output can be prevented by connecting this tarminal with the output terminal through an external capacitor. (see block diagram) When SAG correcting function is not necessary, this terminal must be connected with pin "4" directly.
4	Video Output1	V_{OUT1}		Output terminal (clamp side) that can drive 75Ω line.
5	Video Output2	V_{OUT2}		Output terminal (bias side) that can drive 75Ω line.
6	No Connection	NC		
7	V^+	V^+		Supply Voltage
8	Input Clamp Terminal	V_{IN2}		Input terminal of $1V_{P-P}$ coler signal. Bias level is 2.8V.

■ TYPICAL CHARACTERISTICS

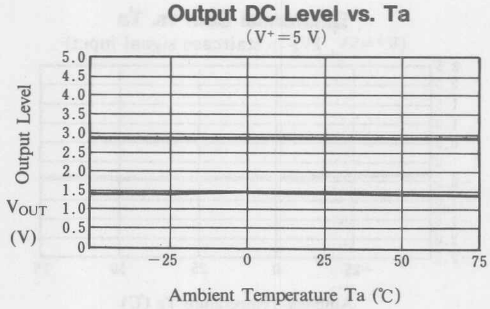
Operating Current vs. Ta



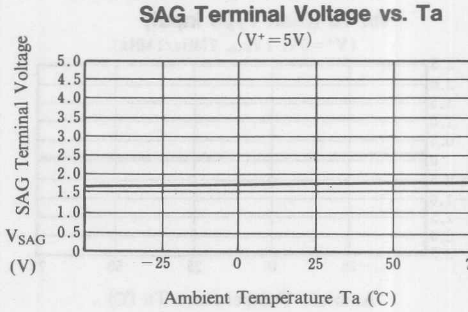
Input DC Level vs. Ta



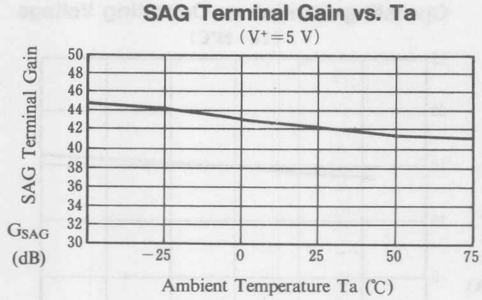
Output DC Level vs. Ta



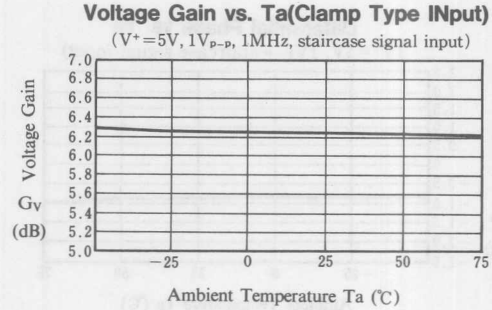
SAG Terminal Voltage vs. Ta



SAG Terminal Gain vs. Ta

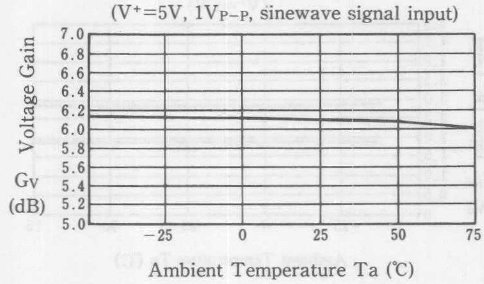


Voltage Gain vs. Ta(Clamp Type INput)

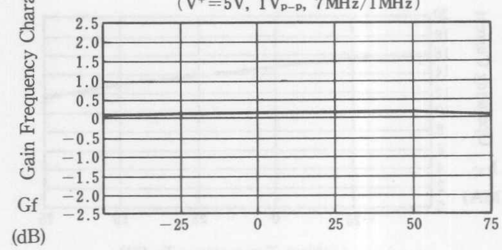


■ TYPICAL CHARACTERISTICS

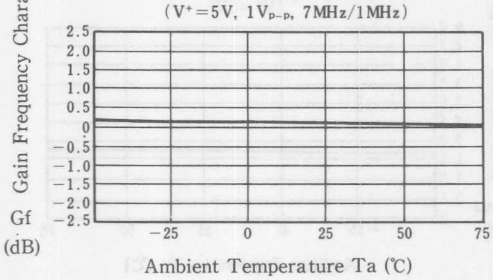
Voltage Gain vs. Ta(Bias Type Input)
(V^+=5V, 1V_{P-P}, sinewave signal input)



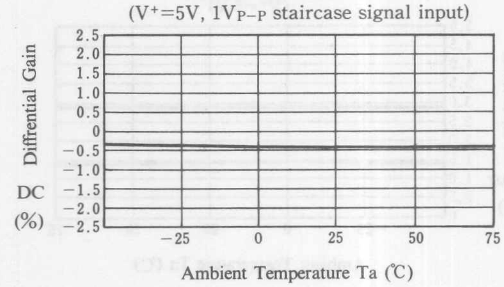
Gain Frequency Characteristics vs. Ta (Clamp Type Input)
(V^+=5V, 1V_{P-P}, 7MHz/1MHz)



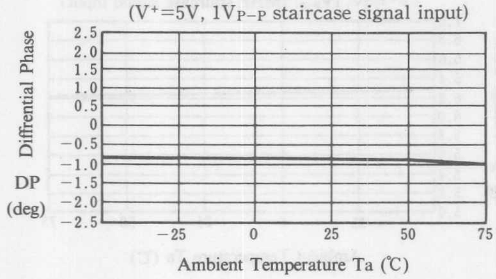
Gain Frequency Characteristics vs. Ta (Bias Type Input)
(V^+=5V, 1V_{P-P}, 7MHz/1MHz)



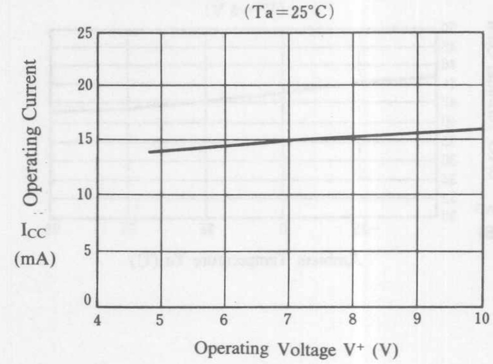
Differential Gain vs. Ta
(V^+=5V, 1V_{P-P} staircase signal input)



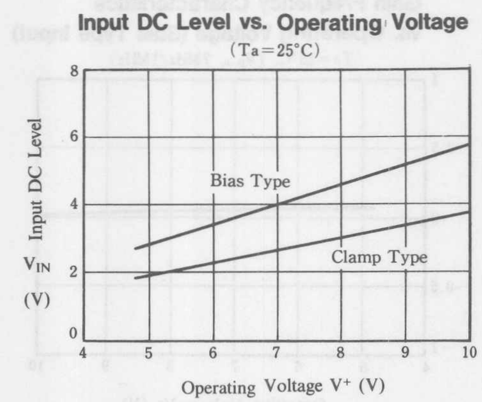
Differential Phase vs. Ta
(V^+=5V, 1V_{P-P} staircase signal input)

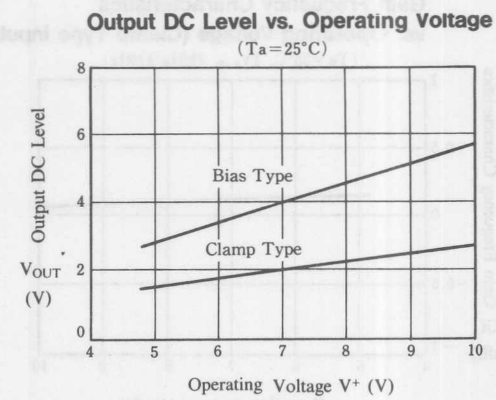


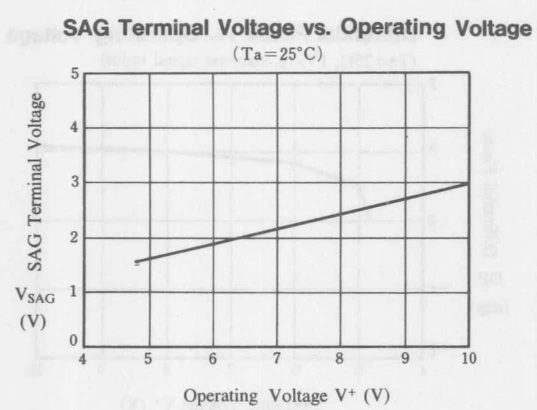
Operating Current vs. Operating Voltage
(Ta=25°C)

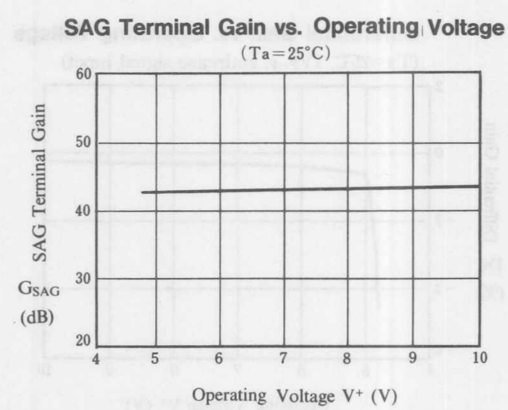


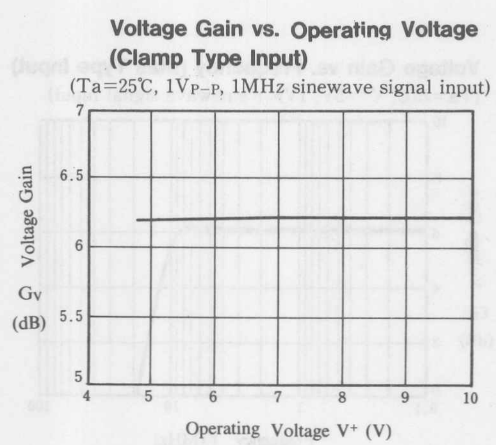
■ TYPICAL CHARACTERISTICS

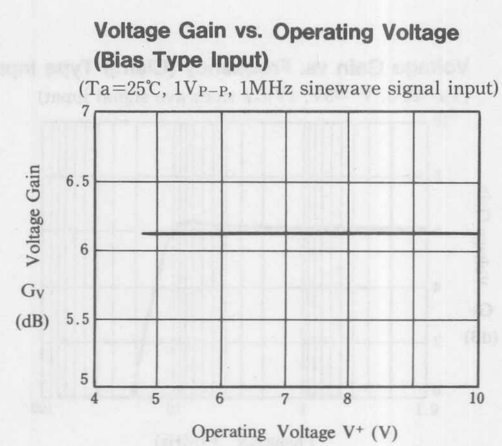








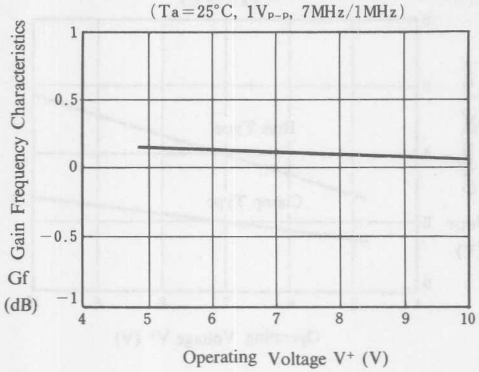




■ TYPICAL CHARACTERISTICS

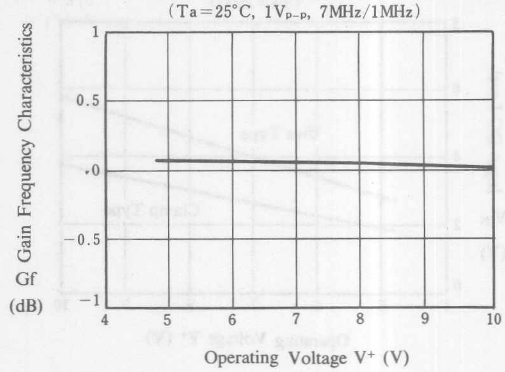
Gain Frequency Characteristics vs. Operating Voltage (Clamp Type Input)

(Ta=25°C, $1V_{P-P}$, 7MHz/1MHz)



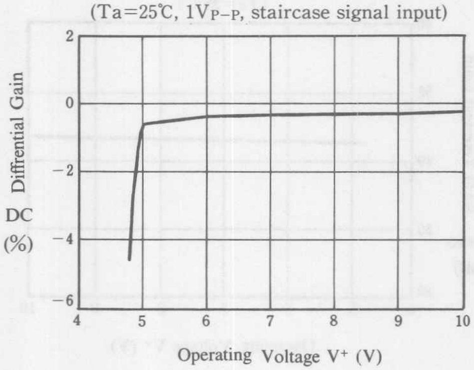
Gain Frequency Characteristics vs. Operating Voltage (Bias Type Input)

(Ta=25°C, $1V_{P-P}$, 7MHz/1MHz)



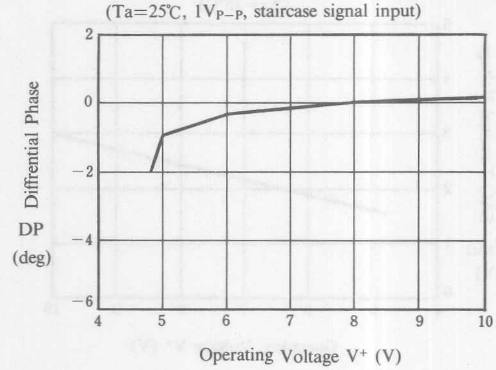
Differential Gain vs. Operating Voltage

(Ta=25℃, $1V_{P-P}$, staircase signal input)



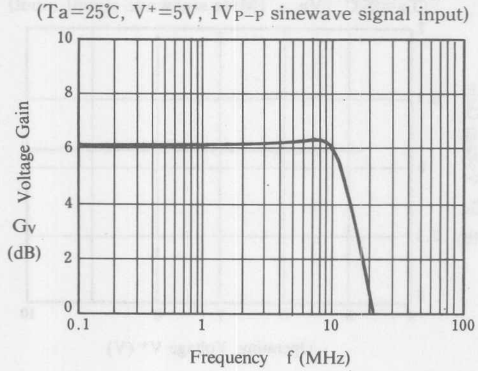
Diffrential Phase vs. Operating Voltage

(Ta=25℃, $1V_{P-P}$, staircase signal input)



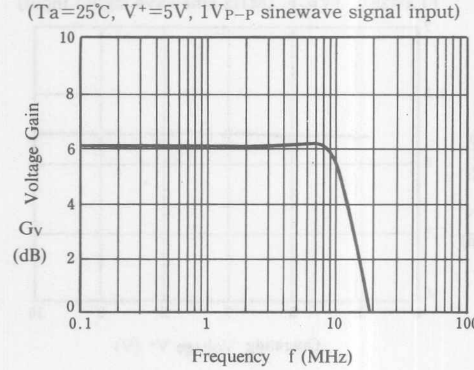
Voltage Gain vs. Frequency (Clamp Type Input)

(Ta=25℃, V^+=5V, $1V_{P-P}$ sinewave signal input)



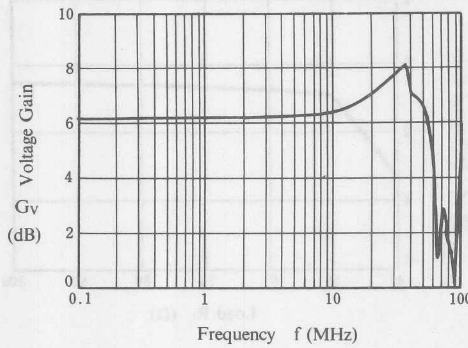
Voltage Gain vs. Frequency (Bias Type Input)

(Ta=25℃, V^+=5V, $1V_{P-P}$ sinewave signal input)

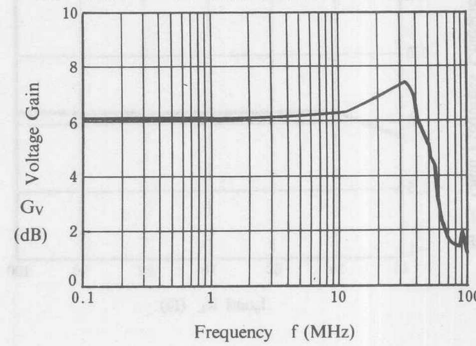


■ TYPICAL CHARACTERISTICS

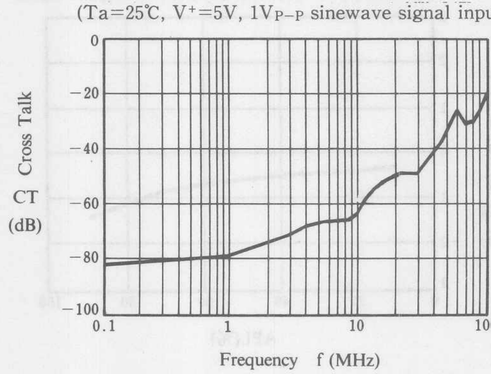
Small Signal Voltage Gain vs. Frequency (Clamp Type Input)
(Ta=25℃, V^{+}=5V_{P-P}, 25mV_{P-P} sinewave signal input)



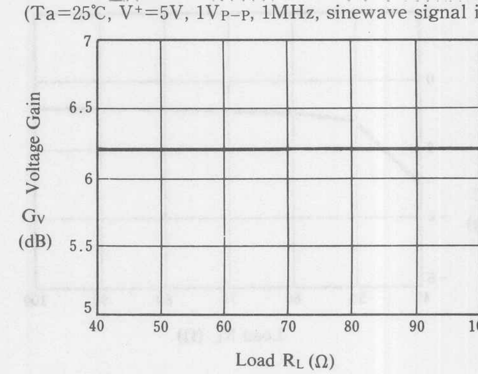
Small Signal Voltage Gain vs. Frequency (Bias Type Input)
(Ta=25℃, V^{+}=5V, 25mV_{P-P}, sinewave signal input)



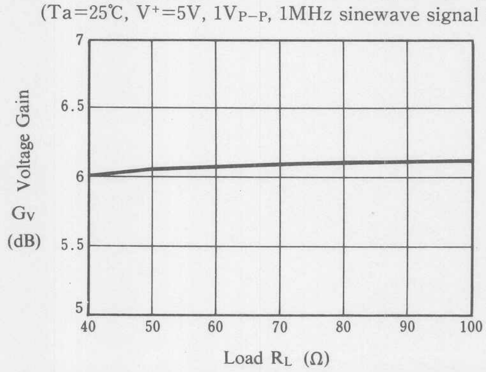
Cross Talk vs. Frequency
(Ta=25℃, V^{+}=5V, 1V_{P-P} sinewave signal input)



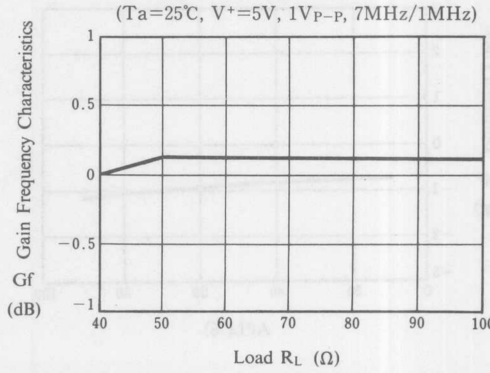
Voltage Gain vs. R_L (Clamp Type Input)
(Ta=25℃, V^{+}=5V, 1V_{P-P}, 1MHz, sinewave signal input)



Voltage Gain vs. R_L (Bias Type Input)
(Ta=25℃, V^{+}=5V, 1V_{P-P}, 1MHz sinewave signal input)

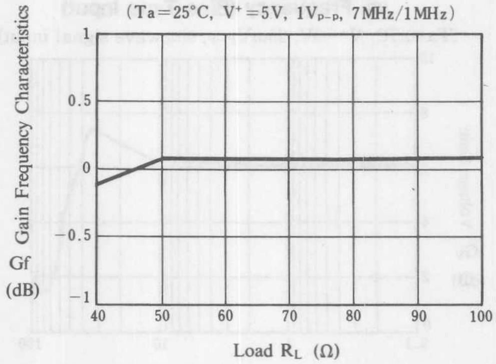


Gain Frequency Characteristics vs. R_L (Clamp Type Input)
(Ta=25℃, V^{+}=5V, 1V_{P-P}, 7MHz/1MHz)

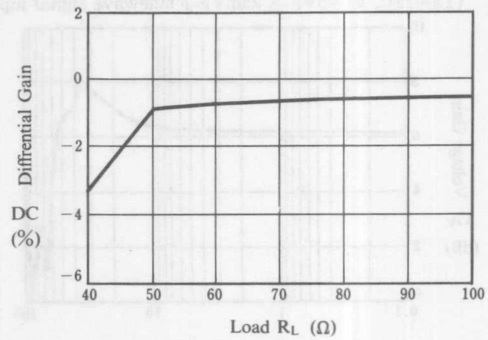


■ TYPICAL CHARACTERISTICS

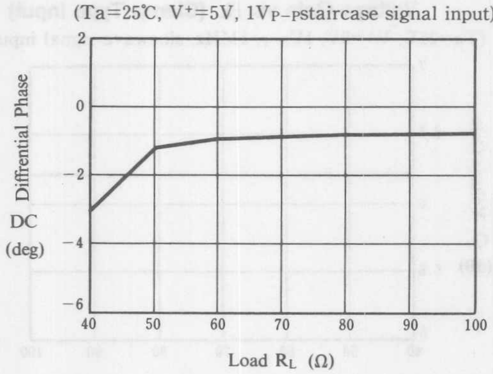
Gain Frequency Characteristics vs. R_L (Bias Type Input)
($Ta=25°C$, $V^+=5V$, $1V_{P-P}$, 7MHz/1MHz)



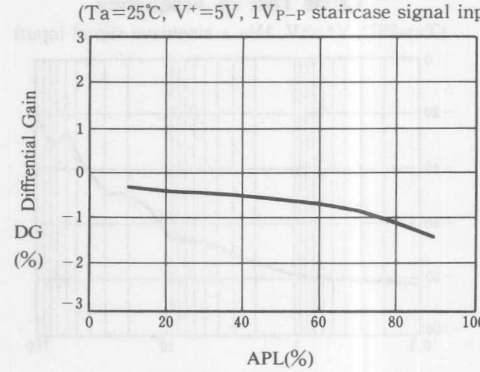
Differential Gain vs. R_L
($Ta=25°C$, $V^+=5V$, $1V_{P-P}$ staircase signal input)



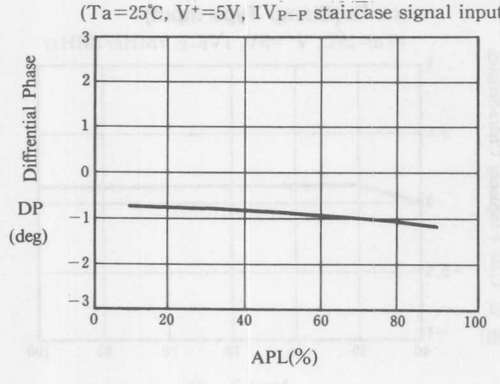
Differential Phase vs. R_L
($Ta=25°C$, $V^+=5V$, $1V_{P-P}$staircase signal input)



Differential Gain vs. APL
($Ta=25°C$, $V^+=5V$, $1V_{P-P}$ staircase signal input)



Differential Phase vs. APL
($Ta=25°C$, $V^+=5V$, $1V_{P-P}$ staircase signal input)

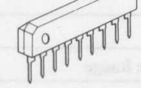


3-INPUT 1MUTE VIDEO SWITCH

■ GENERAL DESCRIPTION

NJM2273 is a switching IC for switching over from one audio or video input signal to another. Internalizing the mute function which can be operated by 3 inputs. It is a higher performance video switch, with the operating supply voltage 4.75 to 13V, frequency bandwidth 7MHz, crosstalk 75dB (at 4.43MHz).

■ PACKAGE OUTLINE



NJM2273S

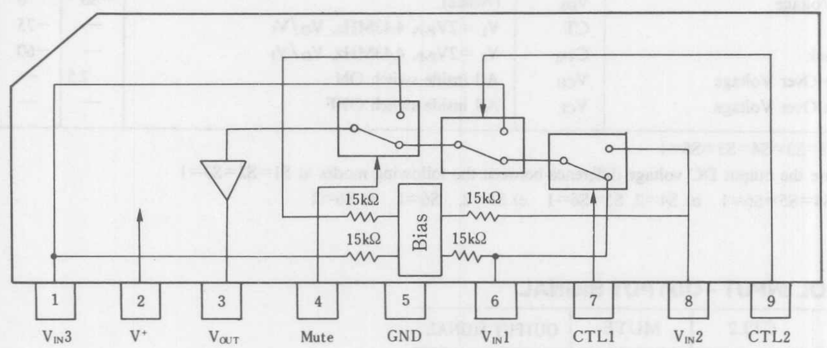
■ FEATURES

- 3 Input, 1 - Output
- Internalizing Mute Function
- Wide Operating Voltage (4.75～13.0V)
- Crosstalk 75 dB(at 4.43MHz)
- Wide Bandwidth Frequency 7MHz(2V_{P-P} Input)
- Package Outline SIP9
- Bipolar Technology

■ APPLICATIONS

- VCR, Video Camera, AV-TV, Video Disk Player.

■ BLOCK DIAGRAM



NJM2273S

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	14	V
Power Dissipation	P_D	(SIP9) 500	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	I_{CC1}	V^+=5V (Note1)	4.5	6.5	8.5	mA
Operating Current (2)	I_{CC2}	V^+=9V (Note1)	5.8	8.3	10.8	mA
Voltage Gain	G_V	V_I =100kHz, $2V_{P-P}$, V_O/V_I	−0.7	−0.2	+0.3	dB
Frequency Gain (1)	G_{F1}	V_I =$2V_{P-P}$, V_O(7MHz)/V_O(100kHz)	−1.0	0	+1.0	dB
Frequency Gain (2)	G_{F2}	V_I =$1V_{P-P}$, V_O(10MHz)/V_O(100kHz)		0		dB
Differential Gain	DG	V_I =$2V_{P-P}$, Standard Staircase Signal	—	0.3	—	%
Differential Phasa	DP	V_I =$2V_{P-P}$, Standard Staircase Signal	—	0.3	—	deg
Output offset Voltage	V_{OS}	(Note2)	−30	0	+30	mV
Crosstalk	CT	V_I =$2V_{P-P}$, 4.43MHz, V_O/V_I	—	−75	—	dB
Muting Crosstalk	C_{TM}	V_I =$2V_{P-P}$, 4.43MHz, V_O/V_I	—	−60	—	dB
Switch Change Over Voltage	V_{CH}	All inside switch ON	2.5	—	—	V
Switch Change Over Voltage	V_{CL}	All inside switch OFF	—	—	1.0	V

(Note1) S1=S2=S3=S4=S5=S6=1

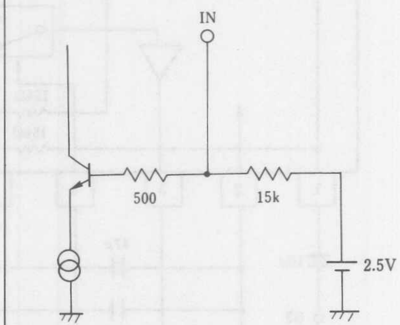
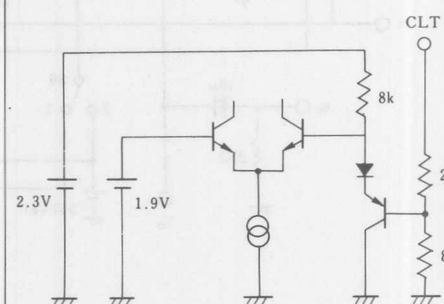
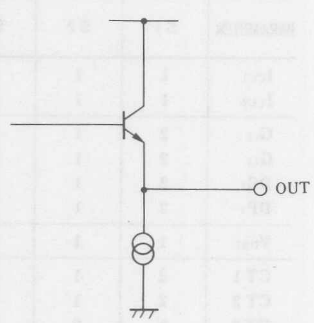
(Note2) Measure the output DC voltage difference between the following modes at S1=S2=S3=1

a) S4=S5=S6=1 b) S4=2, S5=S6=1 c) S5=2, S6=1 d) S6=2

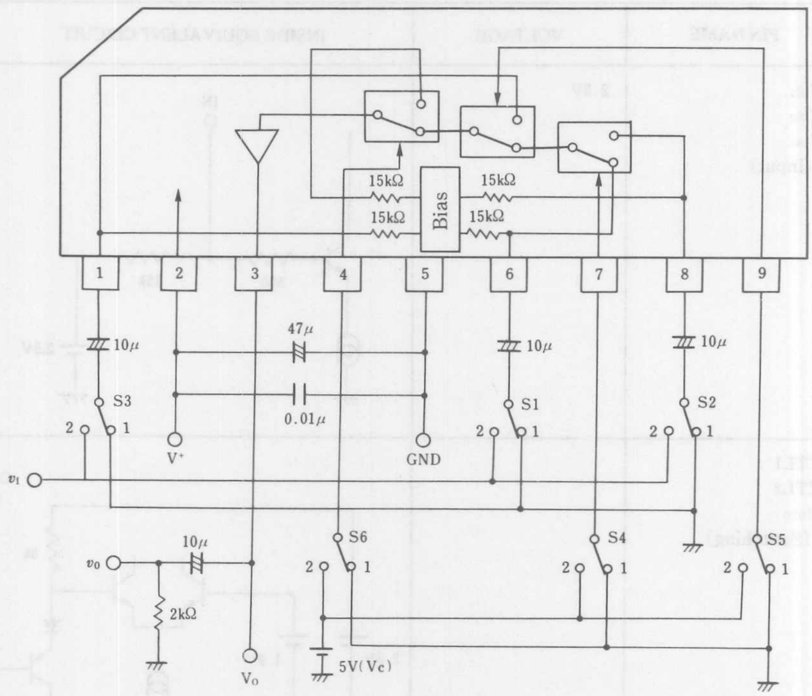
■ CONTROL INPUT - OUTPUT SIGNAL

CTL1	CTL2	MUTE	OUTPUT SIGNAL
L	L	L	$V_{IN}1$
H	L	L	$V_{IN}2$
L/H	H	L	$V_{IN}3$
L/H	L/H	H	Inside DC

■ TERMINAL EXPLANATION

PIN NO.	PIN NAME	VOLTAGE	INSIDE EQUIVALENT CIRCUIT
6 8 1	V_{IN1} V_{IN2} V_{IN3} 〔Input〕	2.5V	
7 9 4	CTL1 CTL2 Mute 〔Switching〕		
3	V_{OUT} 〔Output〕	1.8V	
2	V^{+}	5 V	
5	GND		

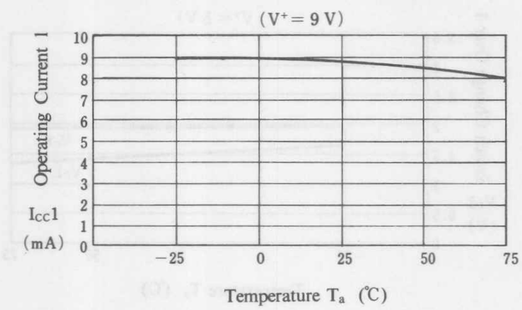
■ TEST CIRCUIT



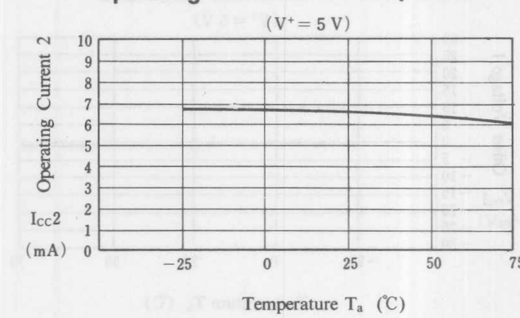
PARAMETER	S 1	S 2	S 3	S 4	S 5	S 6	TEST PART
I_{CC1}	1	1	1	1	1	1	V^+
I_{CC2}	1	1	1	1	1	1	
G_{v1}	2	1	1	1	1	1	v_0
G_{f1}	2	1	1	1	1	1	
DG_1	2	1	1	1	1	1	
DP_1	2	1	1	1	1	1	
V_{OS1}	1	1	1	2	1	1	V_O
CT 1	2	1	1	2	1	1	v_0
CT 2	2	1	1	1	2	1	
CT 3	1	2	1	1	1	1	
CT 4	1	2	1	2	2	1	
CT 5	1	1	2	1/2	1	1	
CT_{M1}	2	1	1	1	1	2	v_0
CT_{M2}	1	2	1	2	1	2	
CT_{M3}	1	1	2	1/2	2	2	
V_{OS1}	1	1	1	2	1	1	V_O
V_{C1}	2	1	1	V_C	1	1	V_C
THD	2	1	1	1	1	1	v_0

■ TYPICAL CHARACTERISTICS

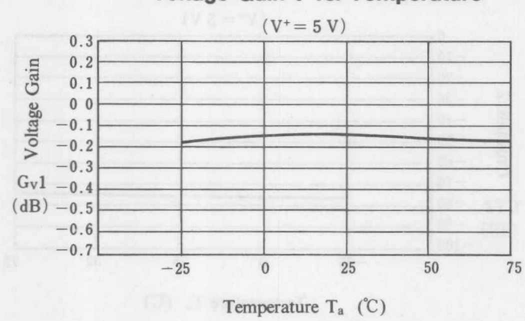
Operating Current 1 vs. Temperature



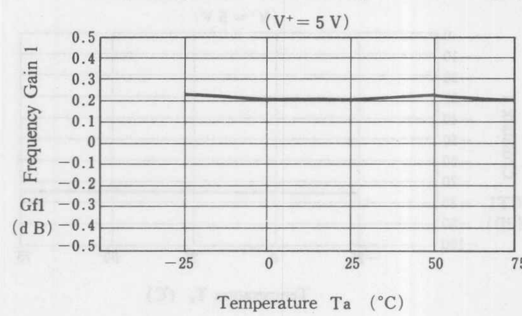
Operating Current 2 vs. Temperature



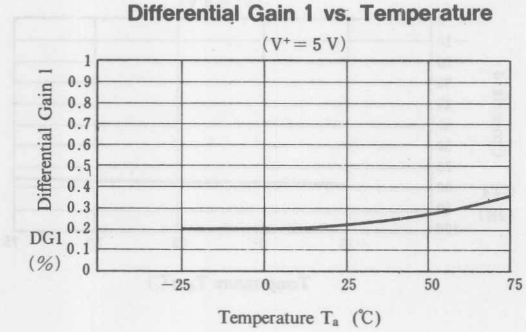
Voltage Gain 1 vs. Temperature



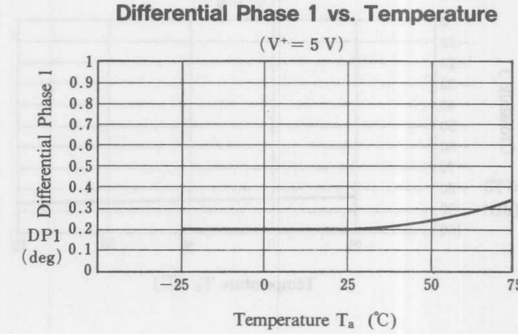
Frequency Gain 1 vs. Temperature Ta (℃)



Differential Gain 1 vs. Temperature

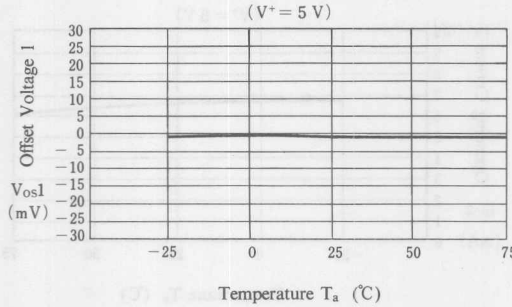


Differential Phase 1 vs. Temperature

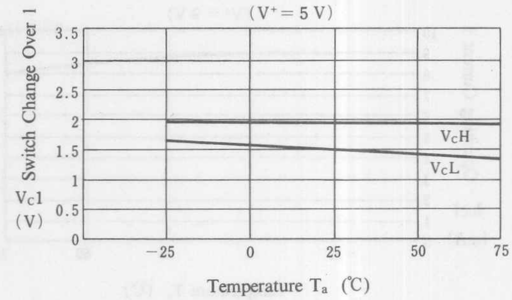


■ TYPICAL CHARACTERISTICS

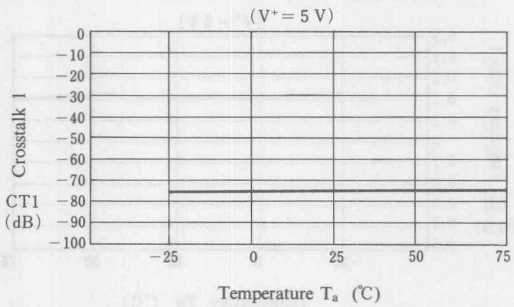
Offset Voltage 1 vs. Temperature



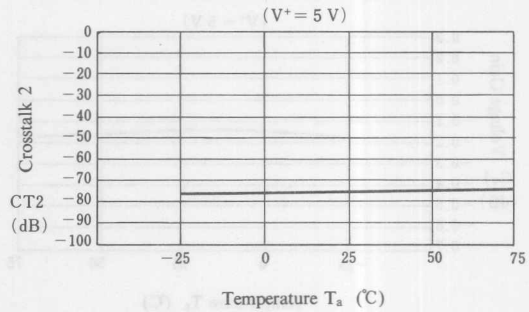
Switch Change Over 1 vs. Temperature



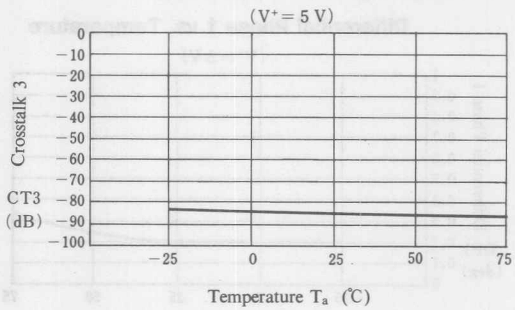
Crosstalk 1 vs. Temperature



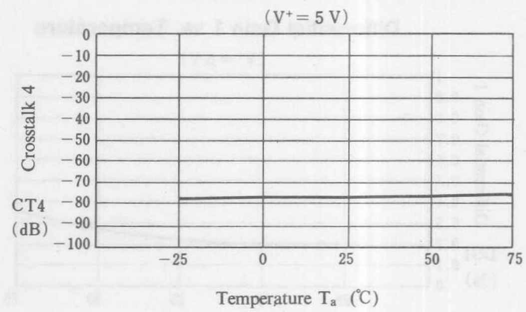
Crosstalk 2 vs. Temperature



Crosstalk 3 vs. Temperature



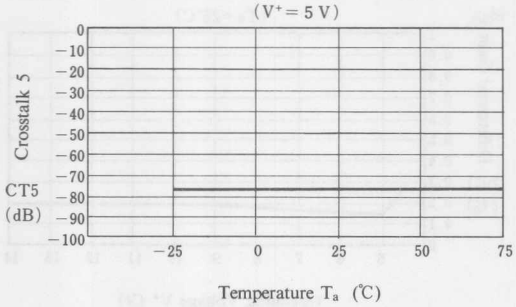
Crosstalk 4 vs. Temperature



■ TYPICAL CHARACTERISTICS

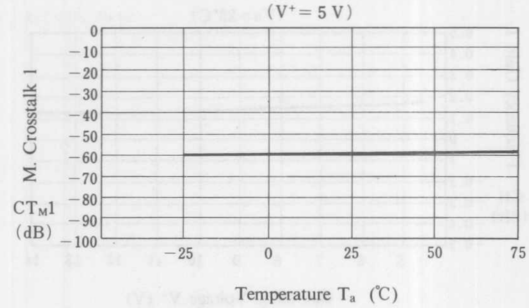
Crosstalk 5 vs. Temperature

($V^+ = 5$ V)



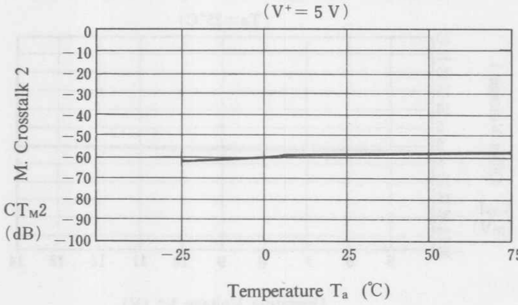
M. Crosstalk 1 vs. Temperature

($V^+ = 5$ V)



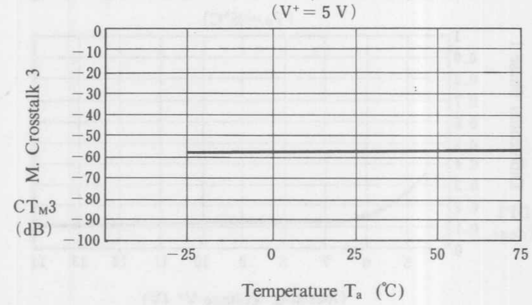
M. Crosstalk 2 vs. Temperature

($V^+ = 5$ V)



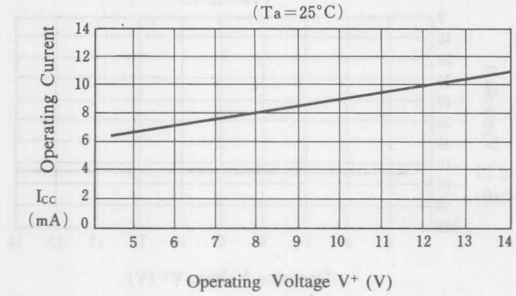
M. Crosstalk 3 vs. Temperature

($V^+ = 5$ V)



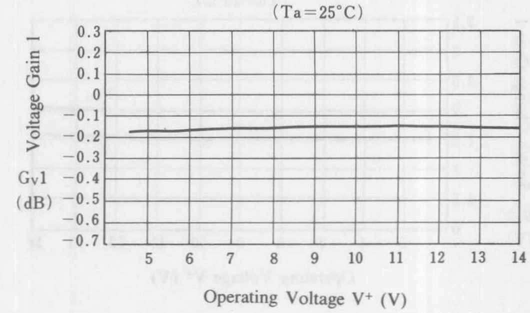
Operating Current vs. Operating Voltage

(Ta=25°C)



Voltage Gain 1 vs. Operating Voltage

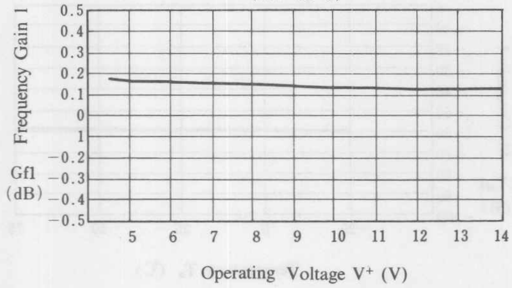
(Ta=25°C)



■ TYPICAL CHARACTERISTICS

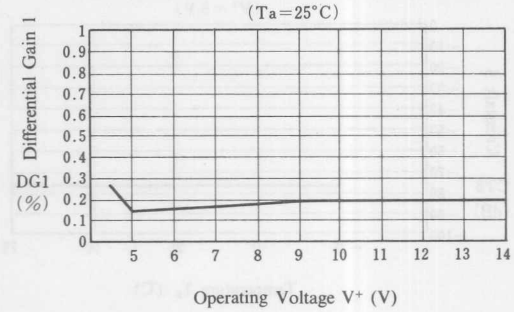
Frequency Gain 1 vs. Operating Voltage

(Ta=25°C)



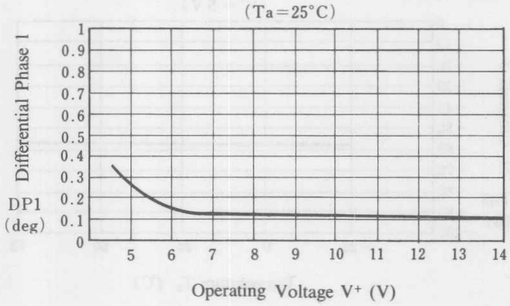
Differential Gain 1 vs. Operating Voltage

(Ta=25°C)



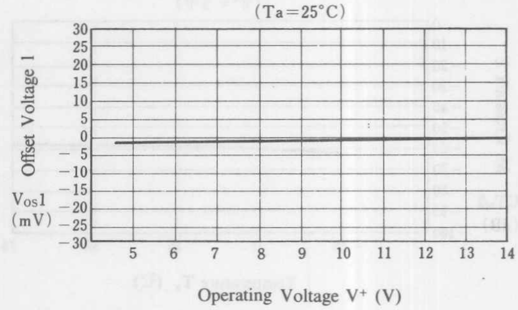
Differential Phase 1 vs. Operating Voltage

(Ta=25°C)



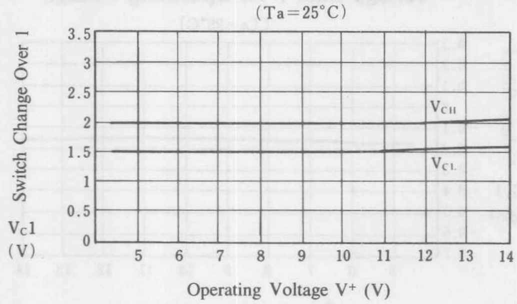
Offset Voltage 1 vs. Operating Voltage

(Ta=25°C)



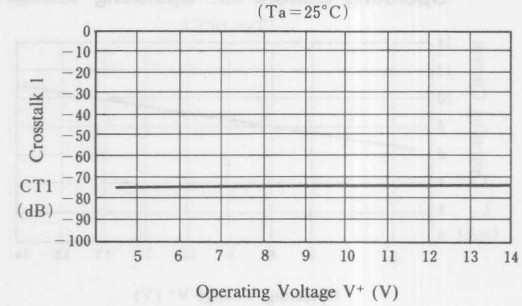
Switch Change Over 1 vs. Operating Voltage

(Ta=25°C)



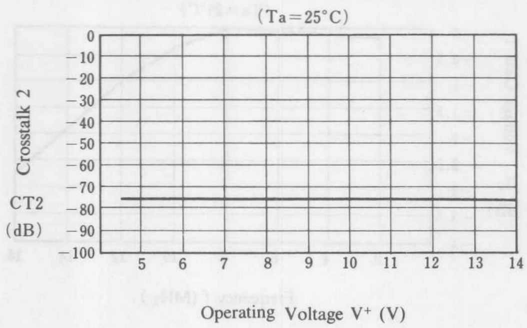
Crosstalk 1 vs. Operating Voltage

(Ta=25°C)

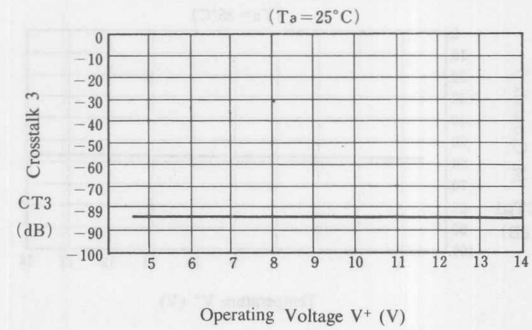


■ TYPICAL CHARACTERISTICS

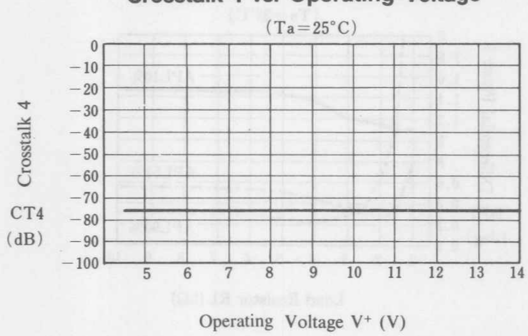
Crosstalk 2 vs. Operating Voltage



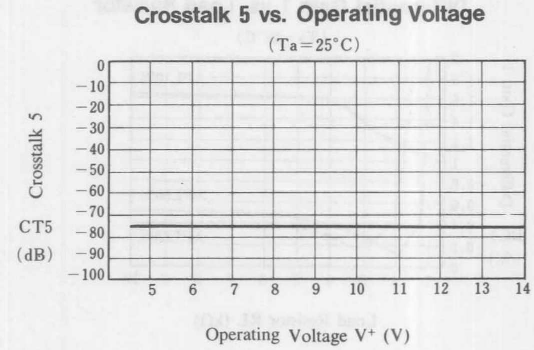
Crosstalk 3 vs. Operating Voltage



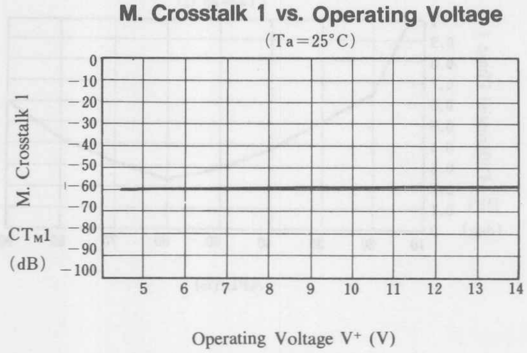
Crosstalk 4 vs. Operating Voltage



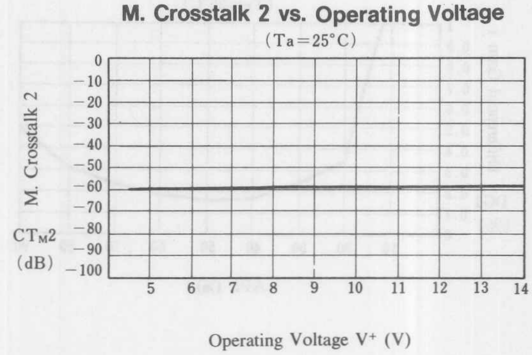
Crosstalk 5 vs. Operating Voltage



M. Crosstalk 1 vs. Operating Voltage

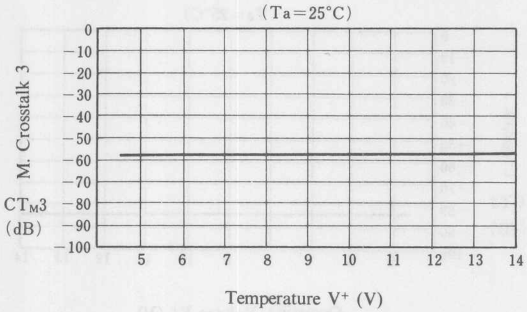


M. Crosstalk 2 vs. Operating Voltage

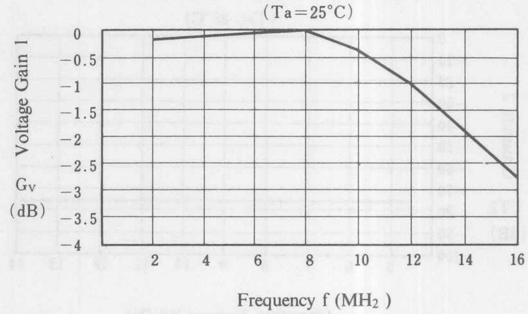


■ TYPICAL CHARACTERISTICS

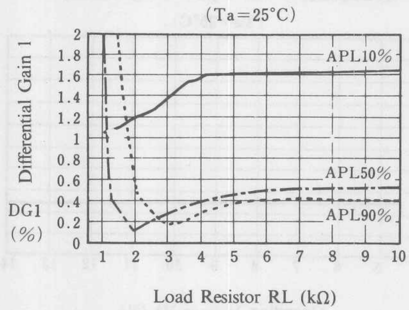
M. Crosstalk 3 vs. Temperature



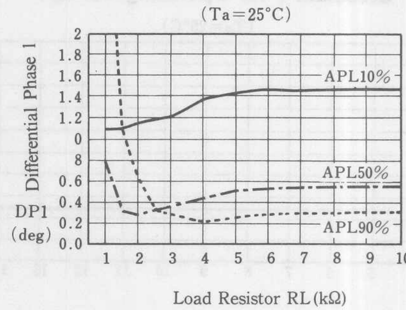
Voltage Gain 1 vs. Frequency



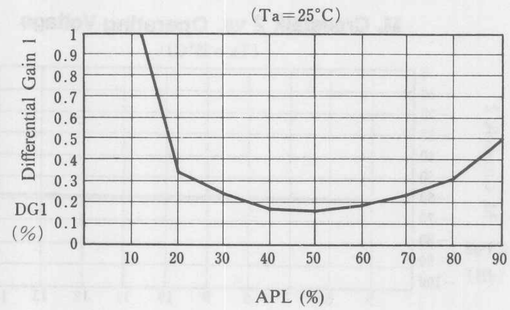
Differential Gain 1 vs. Load Resistor



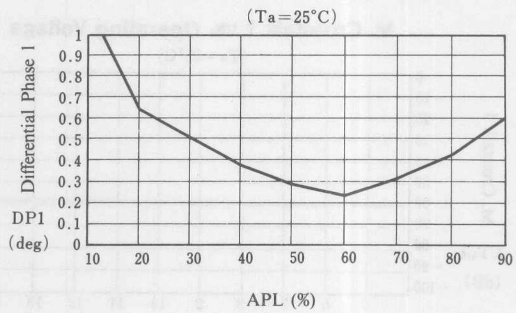
Differential Phase 1 vs. APL



Differential Gain 1 vs. APL

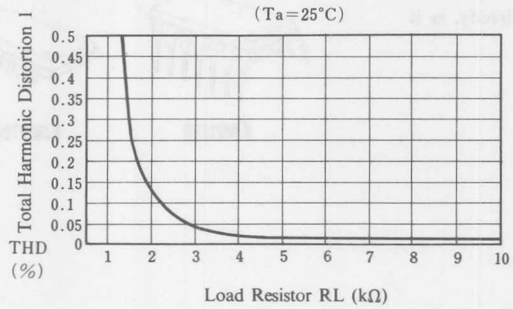


Differential Phase 1 vs. APL



■ TYPICAL CHARACTERISTICS

Total Harmonic Distortion 1 vs. Load Resistor



3-INPUT 2-OUTPUT VIDEO SWITCH FOR AV-SET

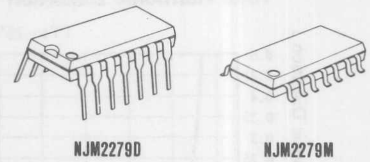
■ GENERAL DESCRIPTION

NJM2279 is 3-input, 2-output video switch with 75Ω driver circuit.

This video switch can be connected to TV monitor directly, as it has 6dB amplifier and 75Ω drivers circuit internally.

The NJM2279 has the mute function.

■ PACKAGE OUTLINE



NJM2279D NJM2279M

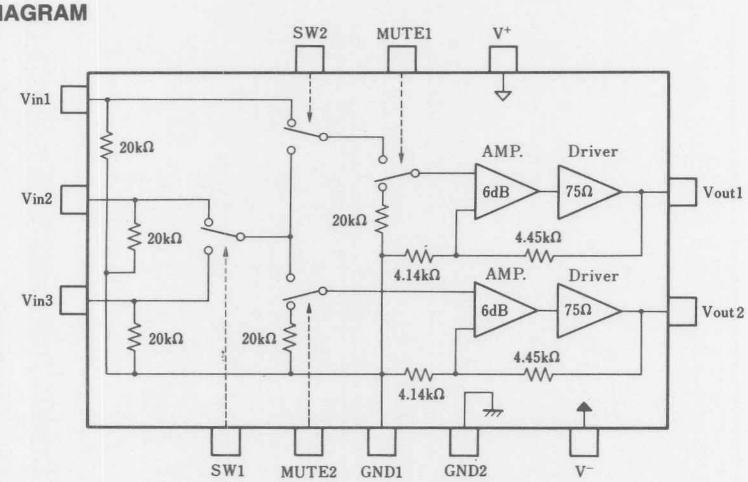
■ FEATURES

- 3 input 2 output
- Internal 6dB AMP.
- Internal 75Ω Driver Circuit
- Operating Voltage Dual (±4V～)
  Single (+8V～)
- Internal 2 Output Mute Function
- Package Outline DIP14, DMP14
- Bipolar Technology

■ RECOMMENDED OPERATING CONDITION

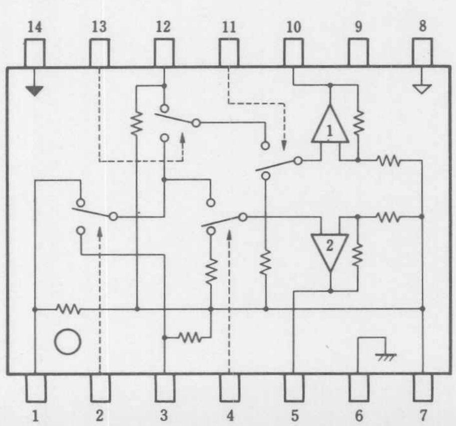
● Supply Voltage	Dual	±4.5V～±5.1V
	Single	+9V～+10.2V

■ BLOCK DIAGRAM



NJM2279D
NJM2279M

■ PIN CONFIGURATION



PIN FUNCTION

1. Vin3	8. V+
2. SW1	9. N.C.
3. Vin2	10. Vout1
4. MUTE2	11. MUTE1
5. Vout2	12. Vin1
6. GND2	13. SW2
7. GND1	14. V−

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

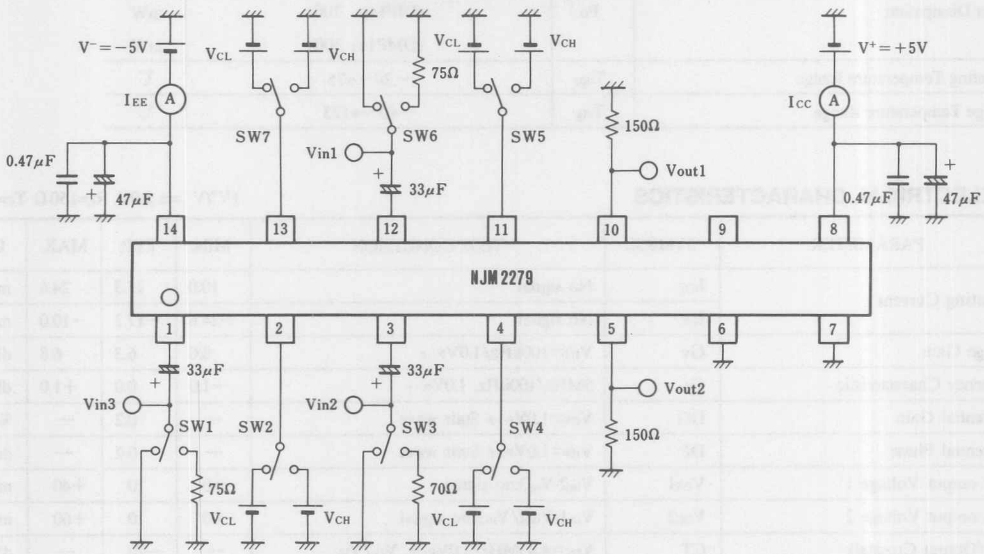
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+/V^-	±7.5	V
Power Dissipation	P_D	(DIP14) 700	mW
		(DMP14) 300	mW
Operating Temperature Range	T_{opr}	−20~+75	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+/V^-=±5.0V, R_L=150Ω Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	No signal	10.0	17.3	24.6	mA
	I_{EE}	No signal	−24.6	−17.3	−10.0	mA
Voltage Gain	G_V	V_{IN}=100kHz/1.0V_{P-P}	6.0	6.3	6.8	dB
Freguency Characteristic	G_f	5MHz/100kHz, 1.0V_{P-P}	−1.0	0.0	+1.0	dB
Differential Gain	DG	V_{IN}=1.0V_{P-P} Stair wave	—	0.2	—	%
Differential Phase	DP	V_{IN}=1.0V_{P-P} Stair wave	—	0.2	—	deg
Offset output Voltage 1	$V_{OS}1$	$V_{in}2$-$V_{in}3$:no signal	−40	0	+40	mV
Offset output Voltage 2	$V_{OS}2$	$V_{in}1$-$V_{in}2$/$V_{in}3$:no signal	−60	0	+60	mV
Input/Output Crosstalk	CT	V_{IN}=4.43MHz/1.0V_{P-P}, V_O/V_{IN}	—	−70	—	dB
MUTE Crosstalk	CT_M	V_{IN}=4.43MHz/1.0V_{P-P}, V_O/V_{IN}	—	−60	—	dB
Switch Change Voltage	V_{CH}		2.5	—	V^+	V
	V_{CL}		0.0	—	1.0	V
Total Harmonic Distortion	THD	V_{IN}=1kHz 1.25V_{P-P}	—	0.1		%
Input Impedance	R_{in}		—	20	—	kΩ

■ TEST CIRCUIT



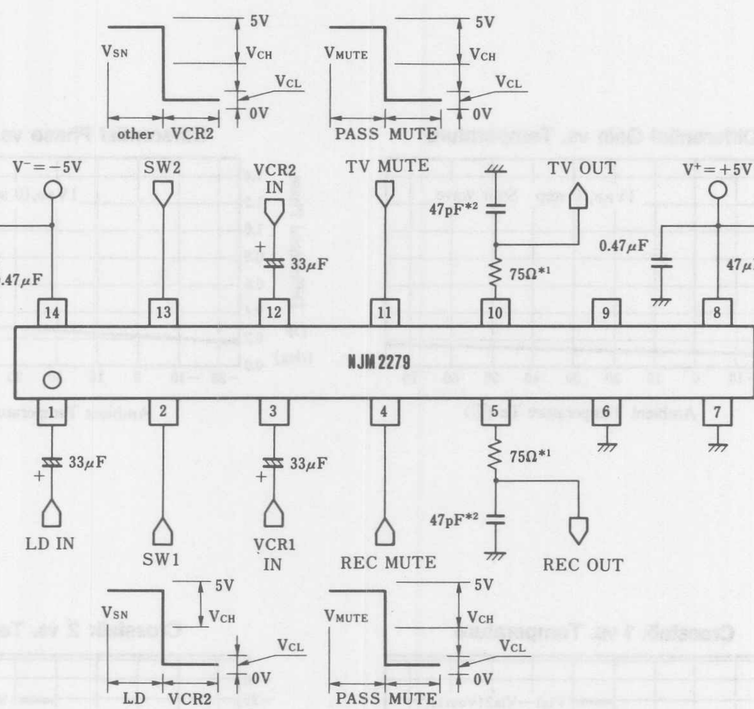
PARAMETER	SYMBOL	UNIT	INPUT TERMINAL	TEST TERMINAL	TEST CONDITION
Operating Current	I_{CC}	mA	—	8 pin	V_{in}1~3=0V, SW1/2・MUTE1/2=V_{CL}
	I_{EE}	mA	—	14 pin	〃
Voltage Gain	G_V	dB	1, 3, 12 pin	5, 10 pin	MUTE1/2=V_{CL}
Freguency Characteristic	G_f	dB	1, 3, 12 pin	5, 10 pin	〃
Differential Gain	DG	%	1, 3, 12 pin	5, 10 pin	〃
Differential Phase	DP	deg	1, 3, 12 pin	5, 10 pin	〃
Offset output Voltage 1	$V_{OS}1$	mV	—	5, 10 pin	V_{in}1~3=0V
Offset output Voltage 2	$V_{OS}2$	mV	—	5, 10 pin	V_{in}1~3=0V
Input/Output Crosstalk	CT	dB	1, 3, 12 pin	5, 10 pin	MUTE1/2=V_{CL}
MUTE Crosstalk	CT_M	dB	1, 3, 12 pin	5, 10 pin	MUTE1/2=V_{CL}
Switch Change Voltage	V_{CH}	V	—	—	
	V_{CL}	V	—	—	
Total Harmonic Distortion	THD	%	1, 3, 12 pin	5, 10 pin	

■ CONTROL SIGNAL-OUTPUT SIGNAL

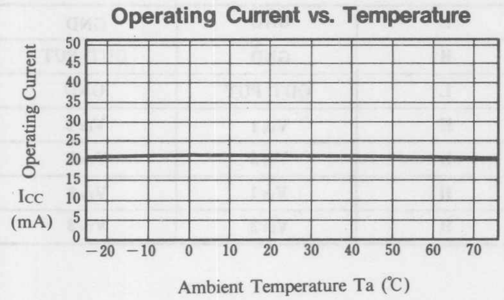
(L=V_{CL}, H=V_{CH}, X=LorH)

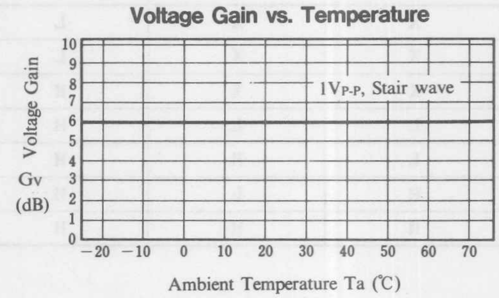
CONTROL SIGNAL				OUTPUT	
SW1 (2 pin)	SW2 (13pin)	MUTE1 (11pin)	MUTE2 (4 pin)	Vout1 (10pin)	Vout2 (5 pin)
X	X	L	L	GND	GND
X	X	L	H	GND	OUT PUT
X	X	H	L	OUT PUT	GND
L	L	H	H	V_{IN}1	V_{IN}2
L	H	H	H	V_{IN}2	V_{IN}2
H	L	H	H	V_{IN}1	V_{IN}3
H	H	H	H	V_{IN}3	V_{IN}3

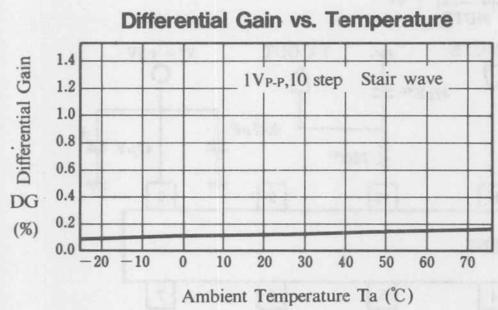
■ APPLICATION

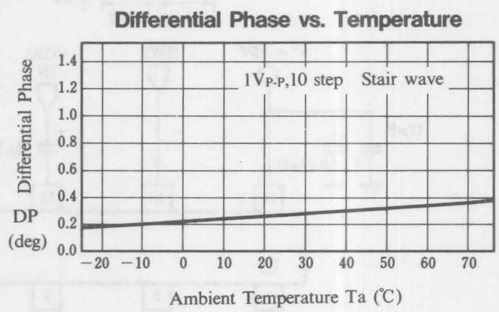


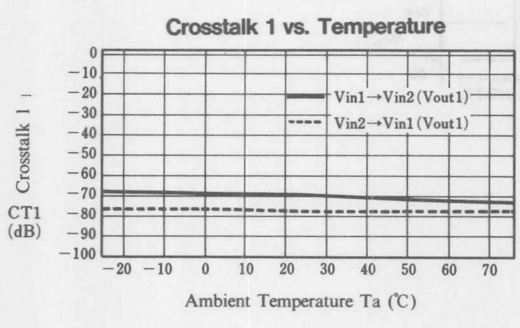
■ TYPICAL CHARACTERISTICS

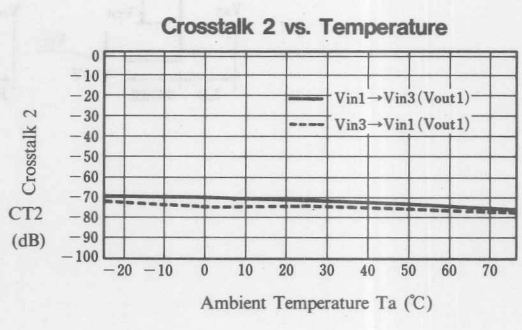






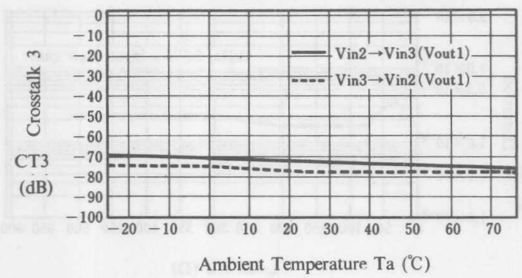




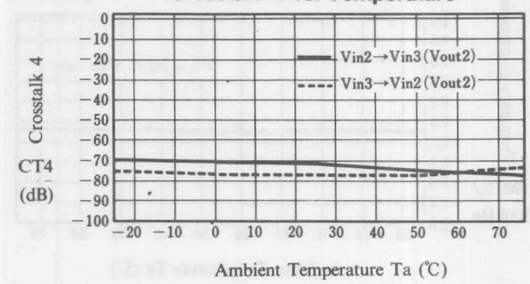


■ TYPICAL CHARACTERISTICS

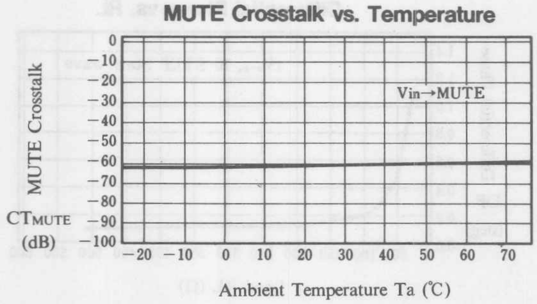
Crosstalk 3 vs. Temperature



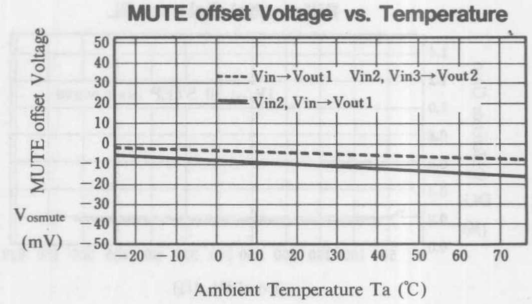
Crosstalk 4 vs. Temperature



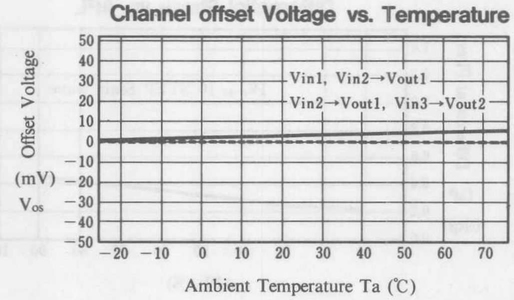
MUTE Crosstalk vs. Temperature



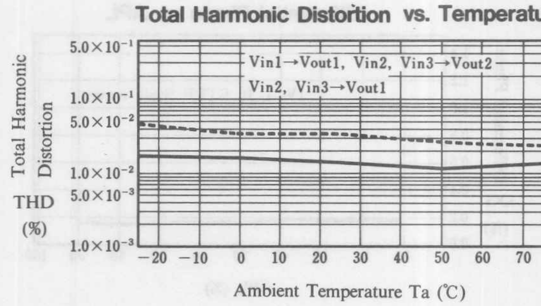
MUTE offset Voltage vs. Temperature



Channel offset Voltage vs. Temperature

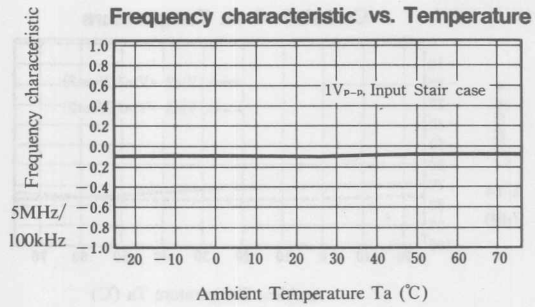


Total Harmonic Distortion vs. Temperature

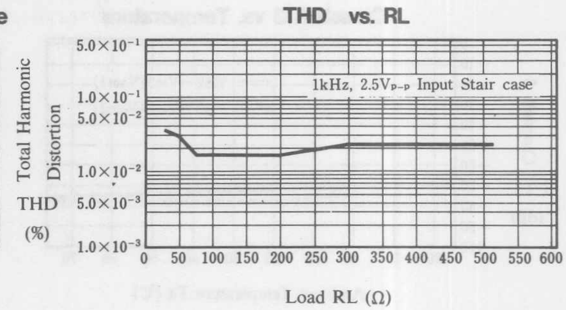


■ TYPICAL CHARACTERISTICS

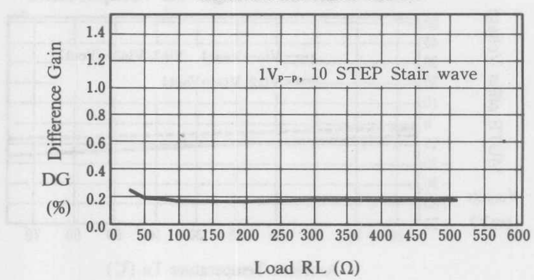
Frequency characteristic vs. Temperature



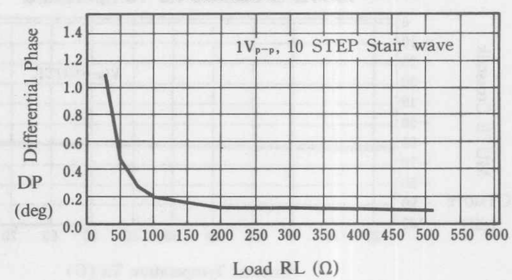
THD vs. RL



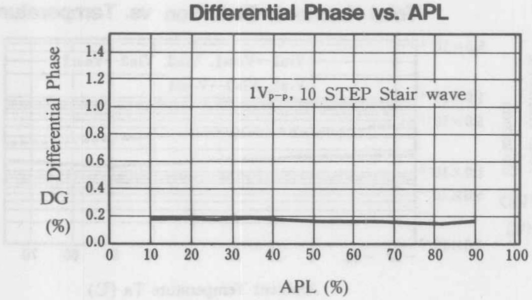
Differential Gain vs. RL



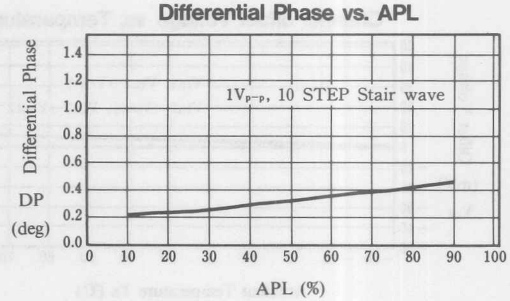
Differential Phase vs. RL



Differential Phase vs. APL

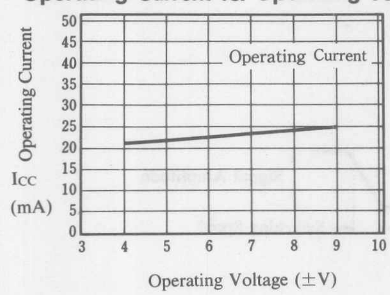


Differential Phase vs. APL

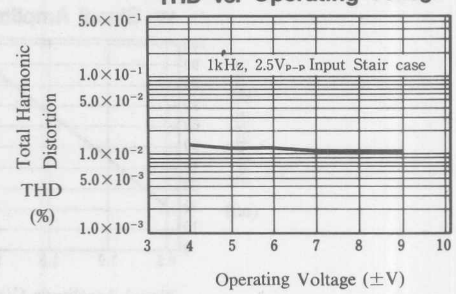


■ TYPICAL CHARACTERISTICS

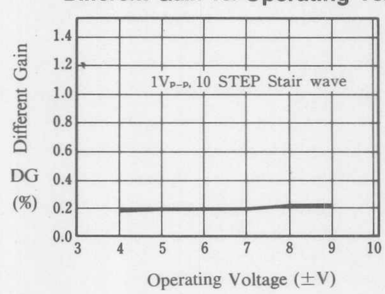
Operating Current vs. Operating Voltage



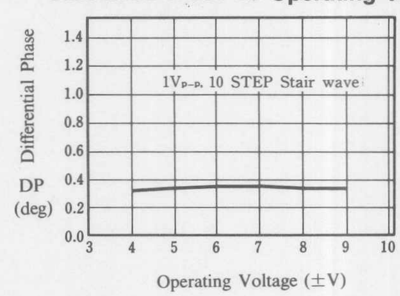
THD vs. Operating Voltsge



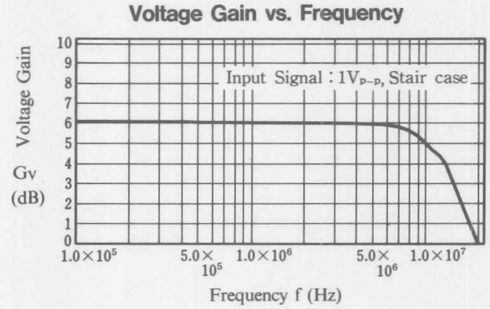
Different Gain vs. Operating Voltage



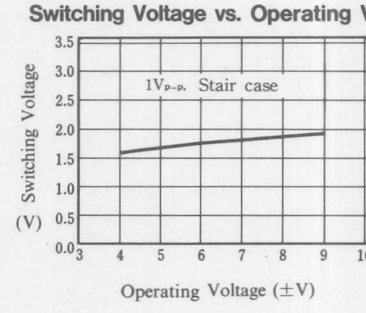
Differential Phase vs. Operating Voltage



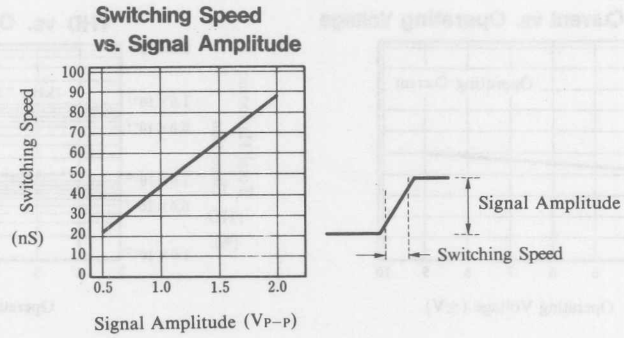
Voltage Gain vs. Frequency



Switching Voltage vs. Operating Voltage



■ TYPICAL CHARACTERISTICS

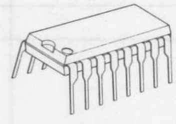


2-INPUT 3CHANNEL VIDEO SWITCH

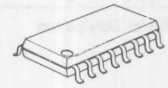
■ GENERAL DESCRIPTION

NJM2283 is a switching IC for switching over from one audio or video input signal to another. Internalizing 2 inputs and 1 output, and then each set of 3 can be operated independently. It is a higher efficiency video switch, featuring the supply voltage range 4.75 to 13.0V, the frequency feature 10MHz, and then Crosstalk 75dB (at 4.43MHz).

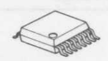
■ PACKAGE OUTLINE



NJM2283D



NJM2283M



NJM2283V

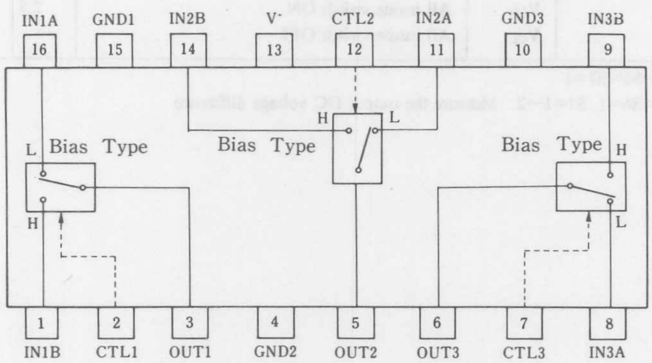
■ FEATURES

- 2 Input-1 Output 3 Circuits internalizing
- Wide Operating Voltage (4.75 ~ 13.0V)
- Crosstalk 75dB(at 4.43MHz)
- Wide Operating Supply Range 10MHz(2V_{P-P} Input)
- Wide Bandwidth Frequency
- Package Outline DIP16, DMP16, SSOP16

■ APPLICATIONS

VCR, Video Camera, AV-TV, Video Disk Player.

■ BLOCK DIAGRAM



NJM2283D
NJM2283M
NJM2283V

■ MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	14	V
Power Dissipation	P_D	(DIP16) 700 (DMP16) 350 (SSOP16) 300	mW mW mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

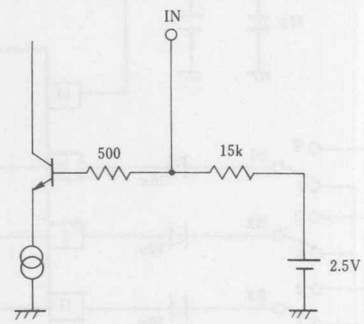
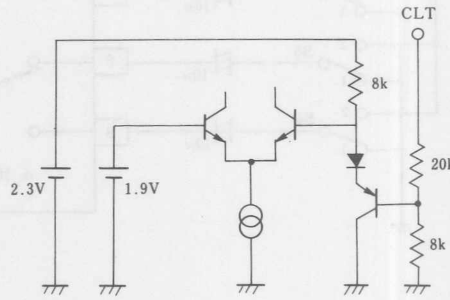
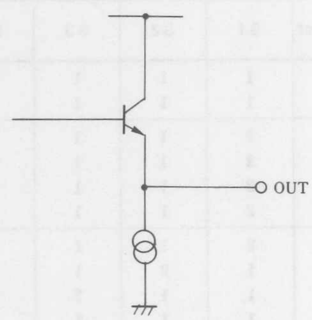
(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	I_{CC1}	V^+=5V (Note1)	8.3	11.8	15.3	mA
Operating Current (2)	I_{CC2}	V^+=9V (Note1)	10.4	14.8	19.2	mA
Voltage Gain	G_V	V_I =100kHz, $2V_{P-P}$, V_O/V_I	−0.6	−0.1	+0.4	dB
Frequency Gain	G_F	V_I =$2V_{P-P}$, V_O(10MHz)/V_O(100kHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_I =$2V_{P-P}$, Standard Staircase Signal	—	0.3	—	%
Differential Phasa	DP	V_I =$2V_{P-P}$, Standard Staircase Signal	—	0.3	—	deg
Output Offset Voltage	V_{OS}	(Note2)	−10	0	+10	mV
Crosstalk	CT	V_I =$2V_{P-P}$, 4.43MHz, V_O/V_I	—	−75	—	dB
Switch Change Over Voltage	V_{CH}	All inside switch ON	2.5	—	—	V
Switch Change Over Voltage	V_{CL}	All inside switch OFF	—	—	1.0	V

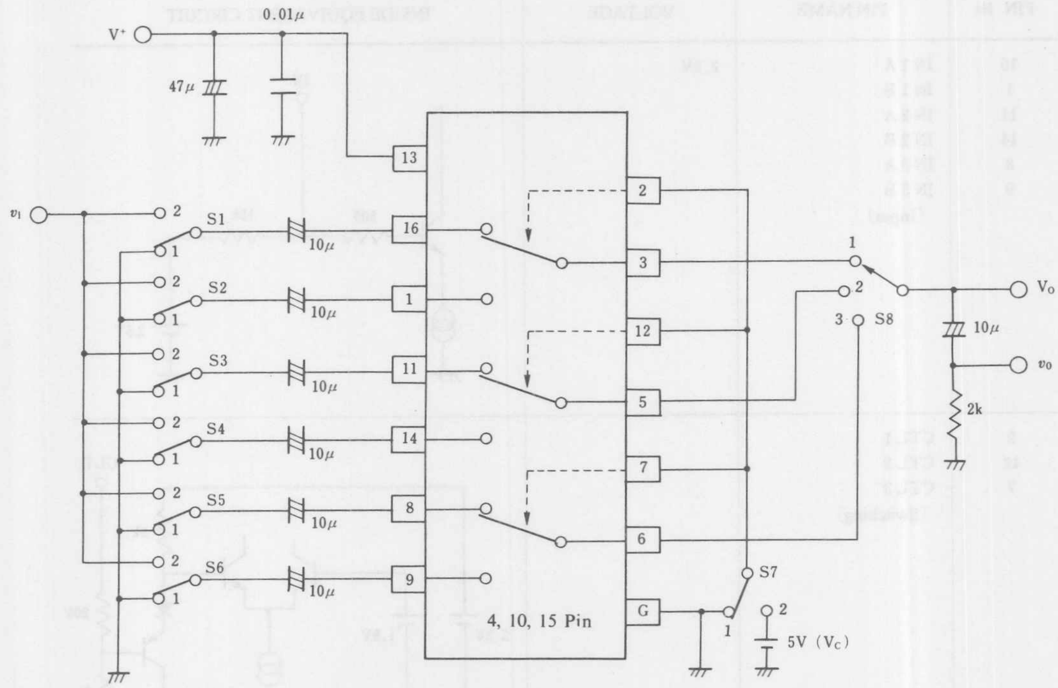
(Note1) S1=S2=S3=S4=S5=S6=S7=1

(Note2) S1=S2=S3=S4=S5=S6=1, S7=1→2 Measure the output DC voltage difference

■ TERMINAL EXPLANATION

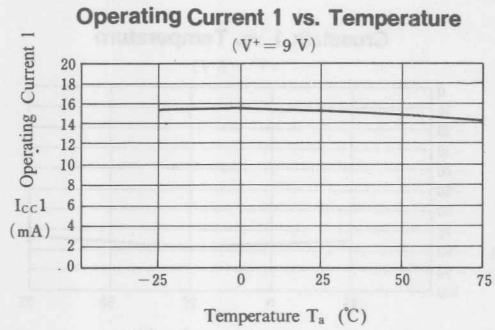
PIN No.	PIN NAME	VOLTAGE	INSIDE EQUIVALENT CIRCUIT
16 1 11 14 8 9	IN 1 A IN 1 B IN 2 A IN 2 B IN 3 A IN 3 B 〔Input〕	2.5V	
2 12 7	CTL 1 CTL 2 CTL 3 〔Switching〕		
3 5 6	OUT 1 OUT 2 OUT 3 〔Output〕	1.8 V	
13	V^+	5 V	
15 4 10	GND 1 GND 2 GND 3		

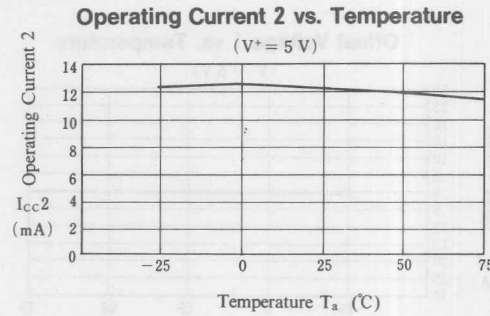
■ TEST CIRCUIT

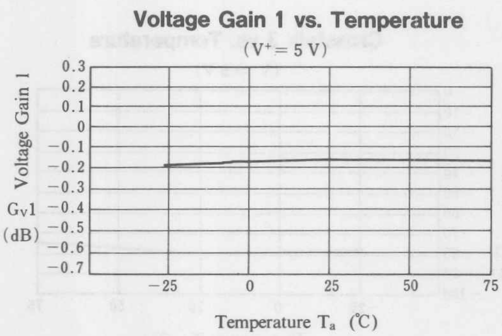


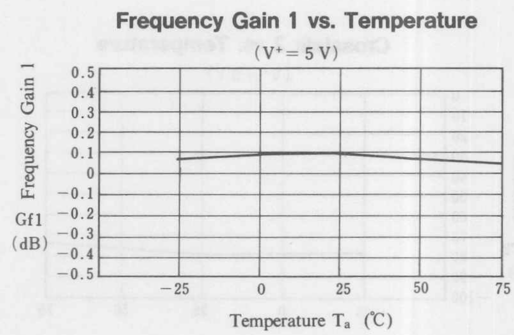
Parameter	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	Test Part
I_{CC1}	1	1	1	1	1	1	1	1	V^+
I_{CC2}	1	1	1	1	1	1	1	1	
G_{v1}	2	1	1	1	1	1	1	1	v_O
G_{f1}	2	1	1	1	1	1	1	1	
DG_1	2	1	1	1	1	1	1	1	
DP_1	2	1	1	1	1	1	1	1	
CT 1	2	1	1	1	1	1	2	1	v_O
CT 2	1	2	1	1	1	1	1	1	
CT 3	1	1	2	1	1	1	2	2	
CT 4	1	1	1	2	1	1	1	2	
CT 5	1	1	1	1	2	1	2	3	
CT 6	1	1	1	1	1	2	1	3	
V_{OS1}	1	1	1	1	1	1	1/2	1	V_O
V_{C1}	1/2	2/1	1	1	1	1	V_C	1	V_C
THD	2	1	1	1	1	1	1	1	v_O

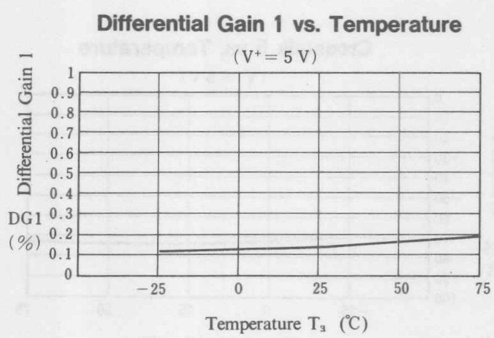
■ TYPICAL CHARACTERISTICS

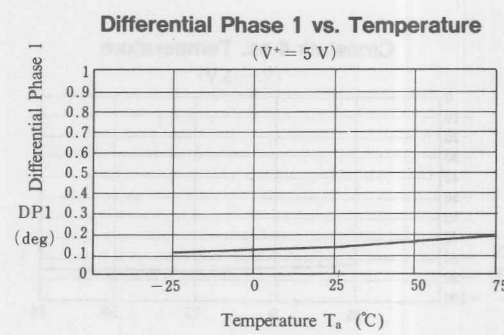








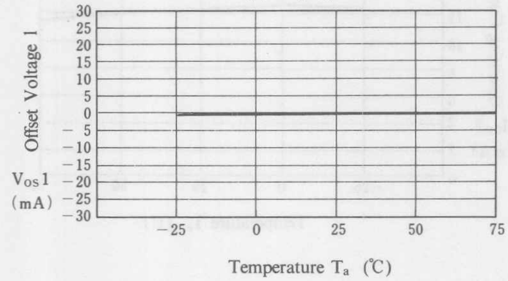




■ TYPICAL CHARACTERISTICS

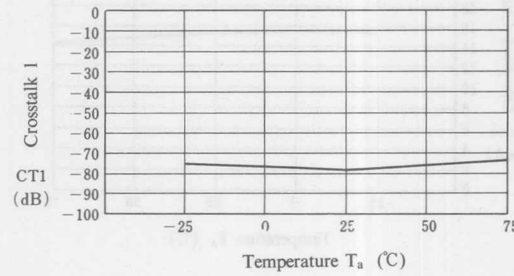
Offset Voltage 1 vs. Temperature

(V+ = 5 V)



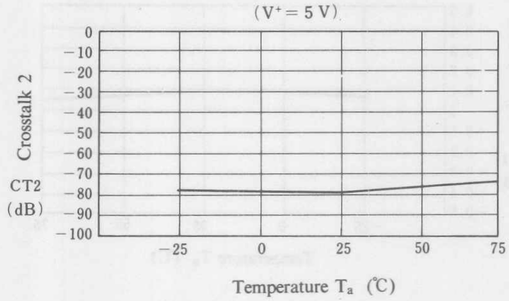
Crosstalk 1 vs. Temperature

(V+ = 5 V)



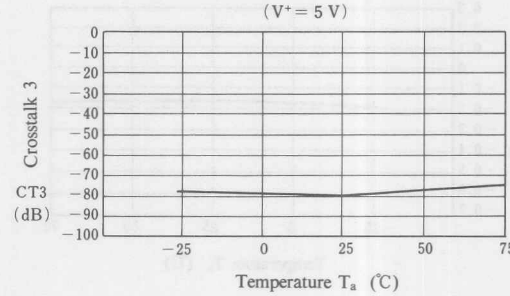
Crosstalk 2 vs. Temperature

(V+ = 5 V)



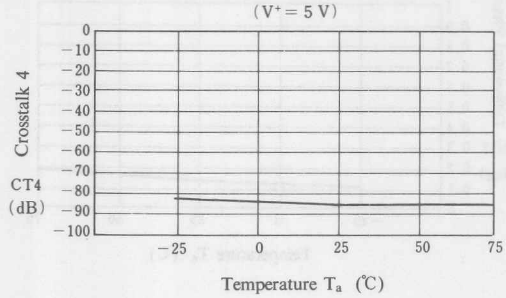
Crosstalk 3 vs. Temperature

(V+ = 5 V)



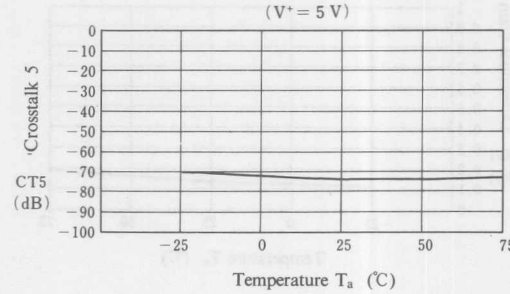
Crosstalk 4 vs. Temperature

(V+ = 5 V)



Crosstalk 5 vs. Temperature

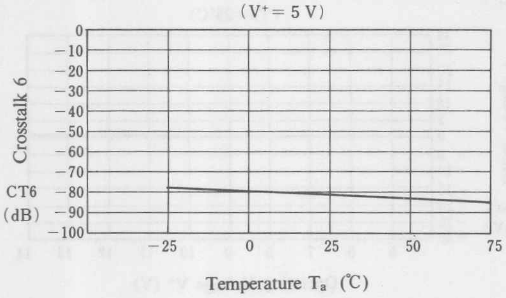
(V+ = 5 V)



■ TYPICAL CHARACTERISTICS

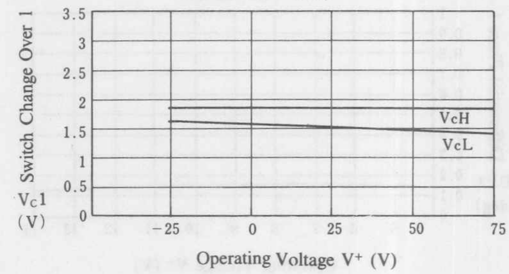
Crosstalk 6 vs. Temperature

($V^+ = 5$ V)



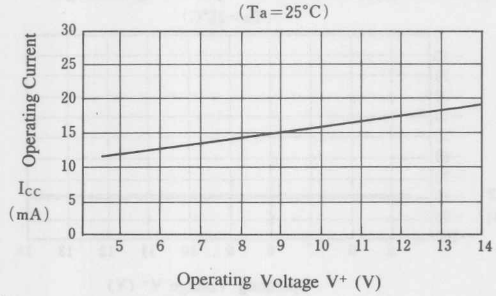
Switch Change Over 1 vs. Operating Voltage

($V^+ = 5$ V)



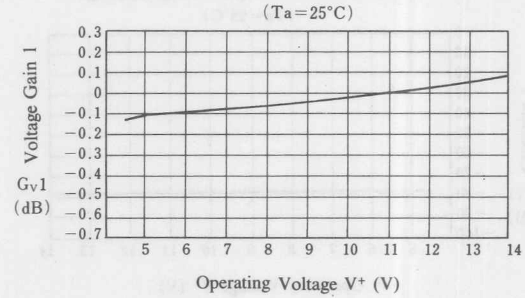
Operating Current vs. Operating Voltage

(Ta=25°C)



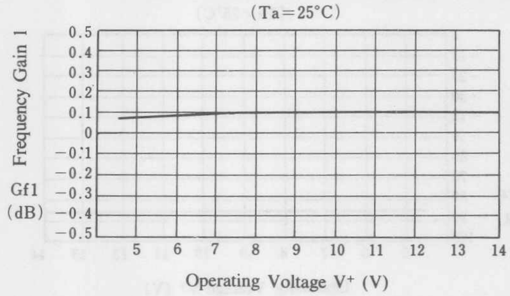
Voltage Gain 1 vs. Operating Voltage

(Ta=25°C)



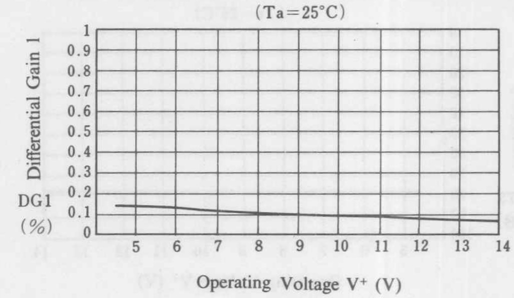
Frequency Gain 1 vs. Operating Voltage

(Ta=25°C)



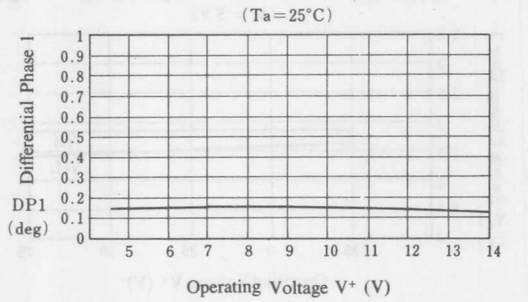
Differential Gain 1 vs. Operating Voltage

(Ta=25°C)

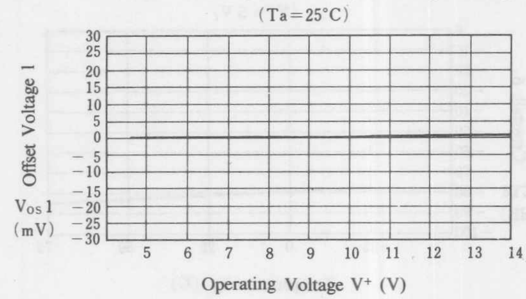


■ TYPICAL CHARACTERISTICS

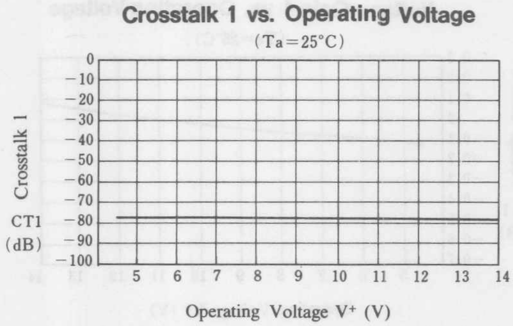
Differential Phase 1 vs. Operating Voltage



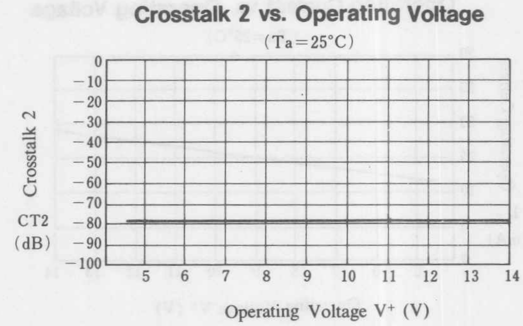
Offset Voltage 1 vs. Operating Voltage



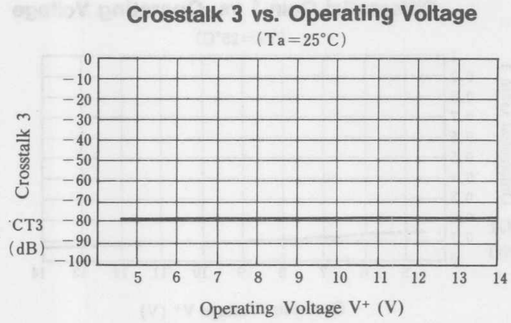
Crosstalk 1 vs. Operating Voltage



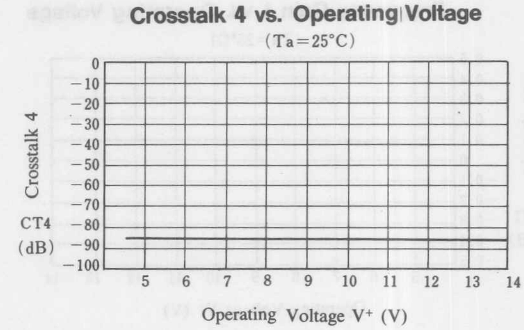
Crosstalk 2 vs. Operating Voltage



Crosstalk 3 vs. Operating Voltage



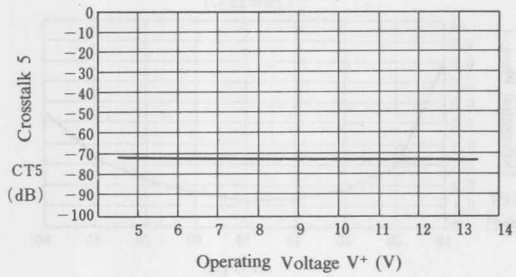
Crosstalk 4 vs. Operating Voltage



■ TYPICAL CHARACTERISTICS

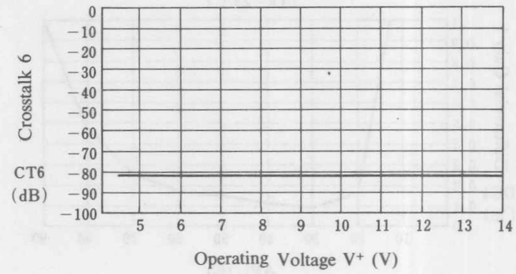
Crosstalk 5 vs. Operating Voltage

(Ta=25°C)



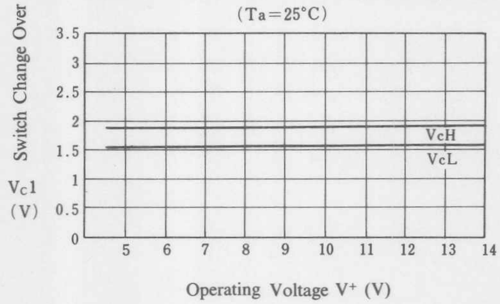
Crosstalk 6 vs. Operating Voltage

(Ta=25°C)



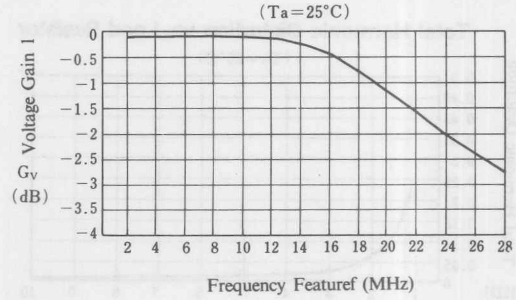
Switch Change Over 1 vs. Operating Voltage

(Ta=25°C)



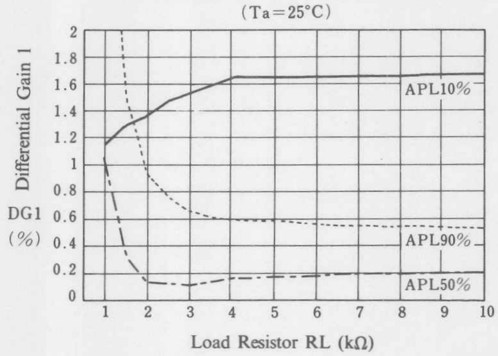
Voltage Gain 1 vs. Frequency Feature

(Ta=25°C)



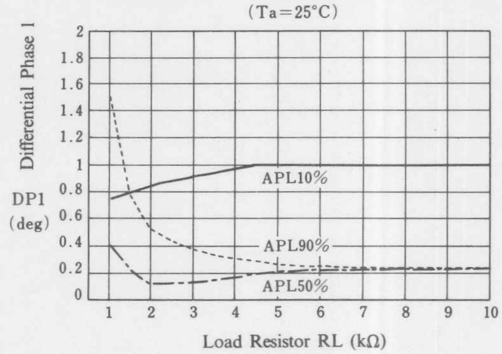
Differential Gain 1 vs. Load Resistor

(Ta=25°C)

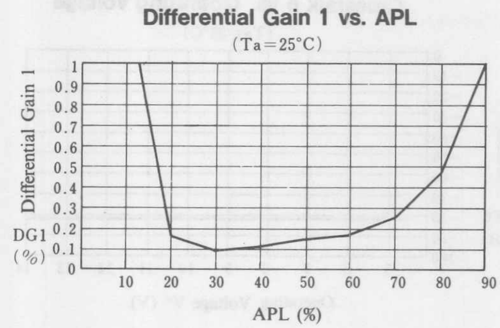


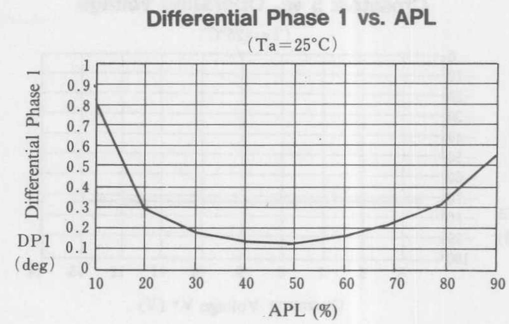
Differential Phase 1 vs. Load Resistor

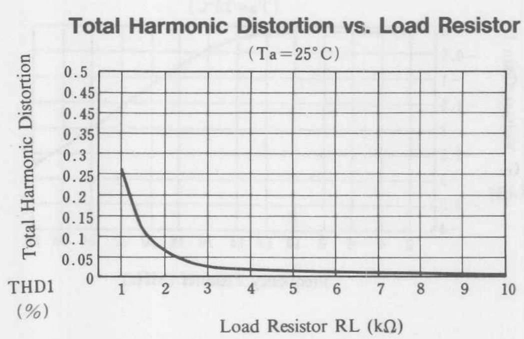
(Ta=25°C)



■ TYPICAL CHARACTERISTICS





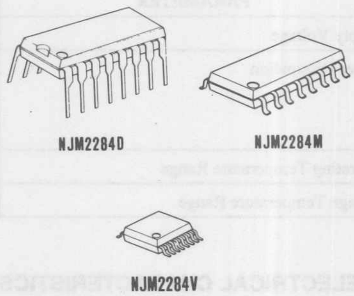


2-INPUT 3CHANNEL VIDEO SWITCH

■ GENERAL DESCRIPTION

NJM2284 is a switching IC for switching over from one audio or video input signal to another. Internalizing 2 inputs, 1 output, and then each set of 3 can be operated independently. One of them is a Clamp type" and it can be operated while DC level fixed in position of the video signal. It is a higher efficiency video switch, featuring the operating supply voltage 4.75 to 13.0V, the frequency feature 10MHz, and then the Crosstalk 75dB (at 4.43MHz).

■ PACKAGE OUTLINE



■ FEATURES

- 2 Input-1 Output Internalizing 3 Circuits (one of them is a Clamp type).
- Wide Operating Voltage
- Crosstalk 75dB(at 4.43MHz)
- Wide Bandwidth Frequency Feature 10MHz(2V_{P-P} Input)
- Package Outline DIP-16, DMP-16, SSOP-16

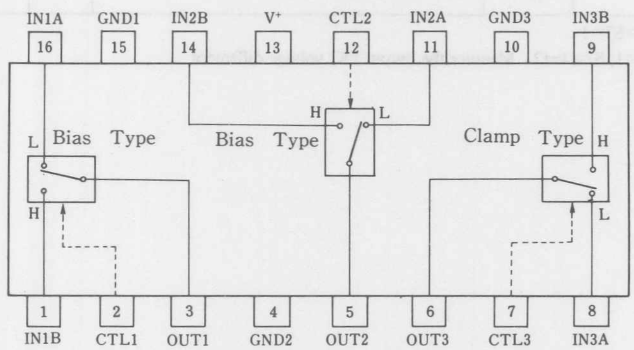
■ RECOMMENDED OPERATING CONDITION

- Supply Voltage V^+ 4.75~13.0V

■ APPLICATIONS

- VCR, Video Camera, AV-TV, Video Disk Player.

■ BLOCK DIAGRAM



NJM2284D
NJM2284M
NJM2284V

■ MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	14	V
Power Dissipation	P_D	(DIP16) 700 (DMP16) 350 (SSOP16) 300	mW mW mW
Operating Temperature Range	T_{opr}	−20〜+75	℃
Storage Temperature Range	T_{stg}	−40〜+125	℃

■ ELECTRICAL CHARACTERISTICS

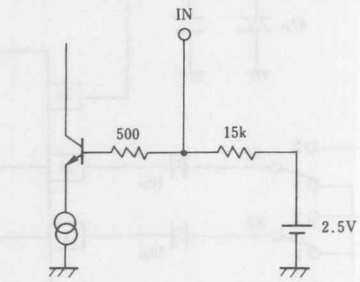
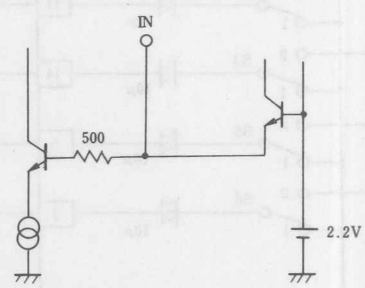
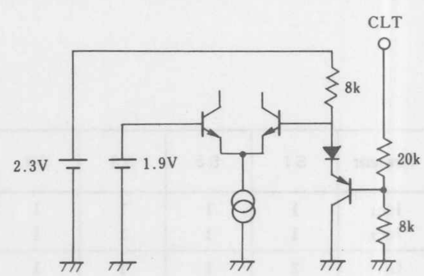
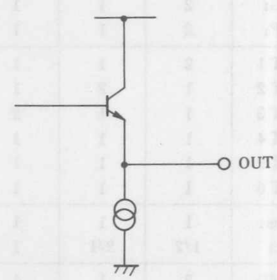
(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	I_{CC1}	V^+=5V (Note1)	8.1	11.6	15.1	mA
Operating Current (2)	I_{CC2}	V^+=9V (Note1)	10.2	14.6	19.0	mA
Voltage Gain	Gv	V_I =100kHz, $2V_{P-P}$, V_O/V_I	−0.6	−0.1	+0.4	dB
Frequency Gain	G_F	V_I =$2V_{P-P}$, V_O(10MHz)/V_O(100kHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_I =$2V_{P-P}$, Standard Staircase Signal	—	0.3	—	%
Differential Phasa	DP	V_I =$2V_{P-P}$, Standard Staircase Signal	—	0.3	—	deg
Output Offset Voltage	V_{OS}	(Note2)	−10	0	+10	mV
Crosstalk	CT	V_I =$2V_{P-P}$, 4.43MHz, V_O/V_I	—	−75	—	dB
Switch Change Over Voltage	V_{CH}	All inside Switch ON	2.5	—	—	V
Switch Change Over Voltage	V_{CL}	All inside Switch OFF	—	—	1.0	V

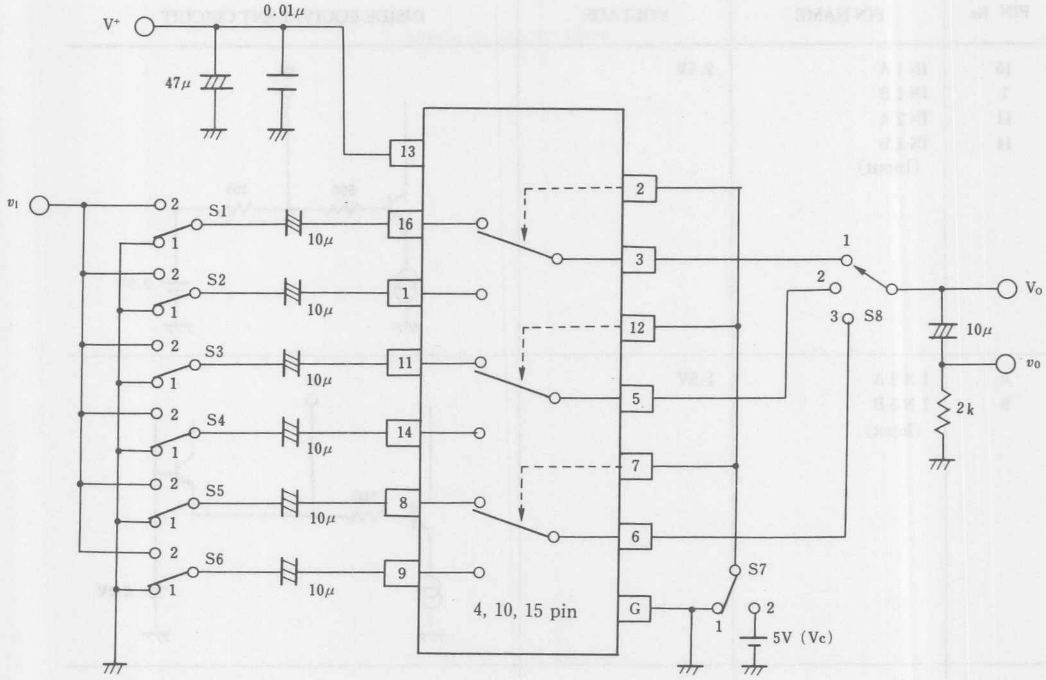
(Note1) S1=S2=S3=S4=S5=S6=S7=1

(Note2) S1=S2=S3=S4=S5=S6=1, S7=1→2 Measure the output DC voltage difference

■ TERMINAL EXPLANATION

PIN No.	PIN NAME	VOLTAGE	INSIDE EQUIVALENT CIRCUIT
16 1 11 14	IN 1 A IN 1 B IN 2 A IN 2 B 〔Input〕	2.5V	
8 9	I N 3 A I N 3 B 〔Input〕	1.5V	
2 12 7	CTL 1 CTL 2 CTL 3 〔Switching〕		
3 5	OUT 1 OUT 2	1.8V	
6	OUT 3 〔Output〕	0.8V	
13	V+	5 V	
15 4 10	GND 1 GND 2 GND 3		

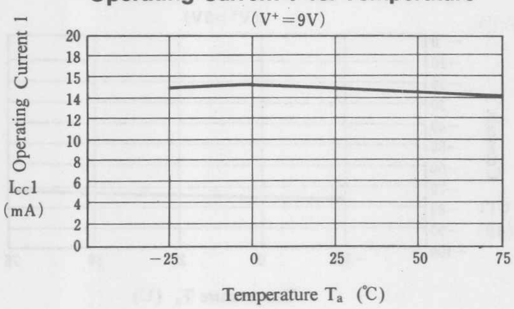
■ TEST CIRCUIT



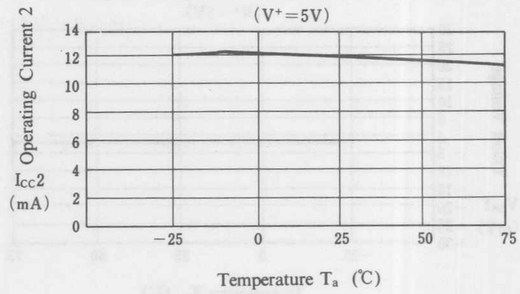
Parameter	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	Test Part
I_{CC1}	1	1	1	1	1	1	1	1	V^+
I_{CC2}	1	1	1	1	1	1	1	1	
G_{v1}	2	1	1	1	1	1	1	1	v_O
G_{f1}	2	1	1	1	1	1	1	1	
DG_1	2	1	1	1	1	1	1	1	
DP_1	2	1	1	1	1	1	1	1	
CT 1	2	1	1	1	1	1	2	1	v_O
CT 2	1	2	1	1	1	1	1	1	
CT 3	1	1	2	1	1	1	2	2	
CT 4	1	1	1	2	1	1	1	2	
CT 5	1	1	1	1	2	1	2	3	
CT 6	1	1	1	1	1	2	1	3	
V_{OS1}	1	1	1	1	1	1	1/2	1	V_O
V_{C1}	1/2	2/1	1	1	1	1	V_C	1	V_C
THD	2	1	1	1	1	1	1	1	v_O

■ TYPICAL CHARACTERISTICS

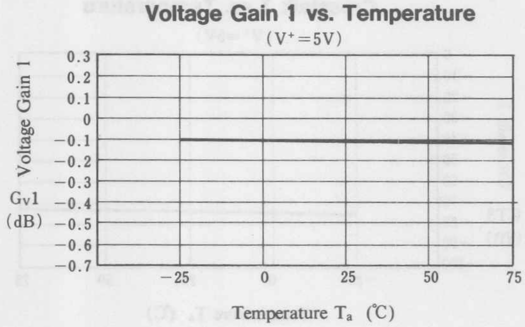
Operating Current 1 vs. Temperature



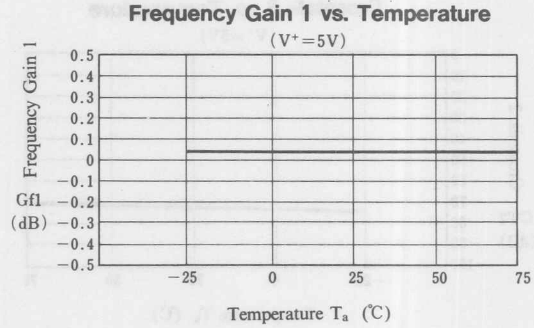
Operating Current 2 vs. Temperature



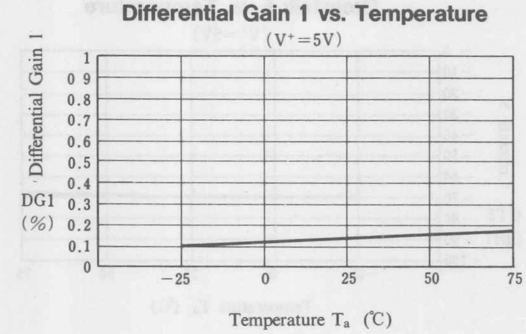
Voltage Gain 1 vs. Temperature



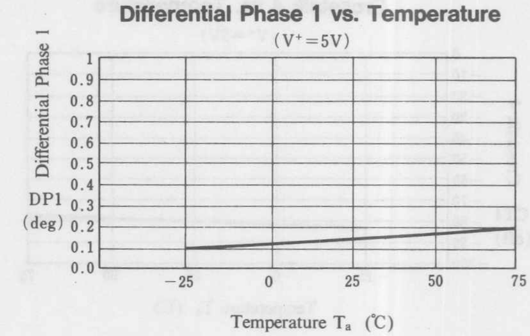
Frequency Gain 1 vs. Temperature



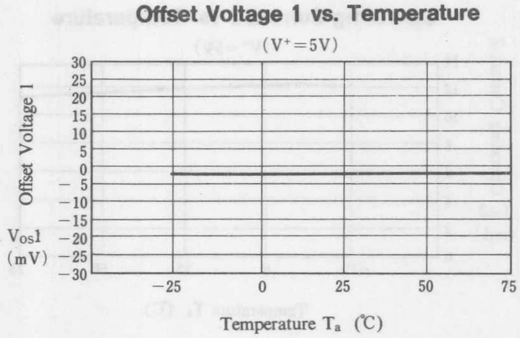
Differential Gain 1 vs. Temperature

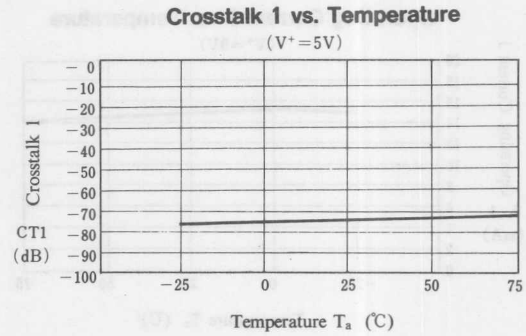


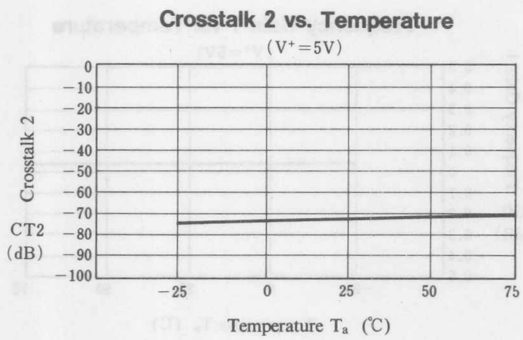
Differential Phase 1 vs. Temperature

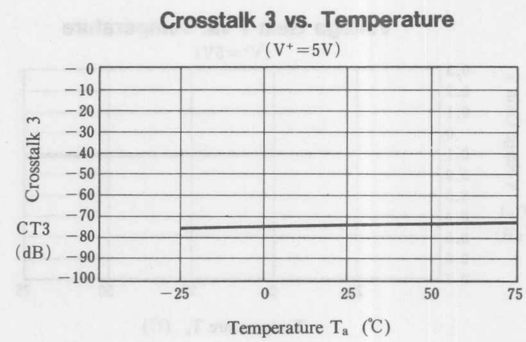


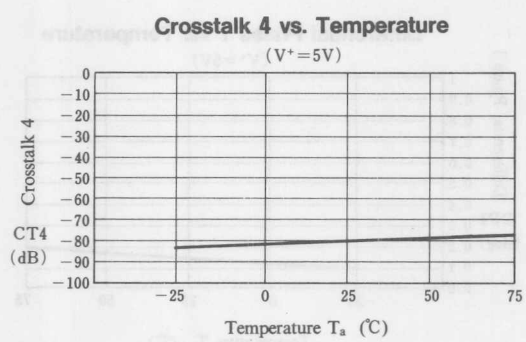
■ TYPICAL CHARACTERISTICS

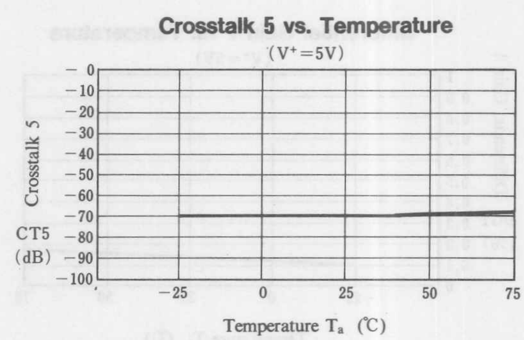






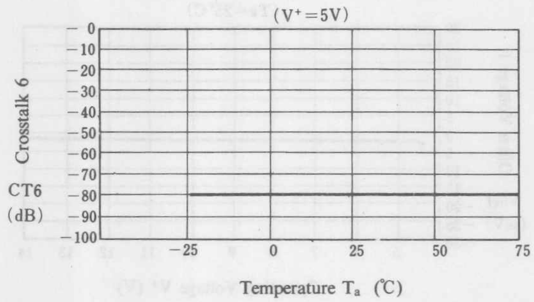




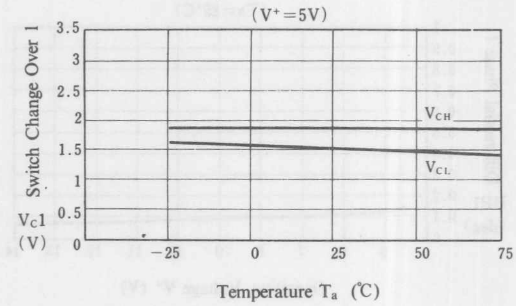


■ TYPICAL CHARACTERISTICS

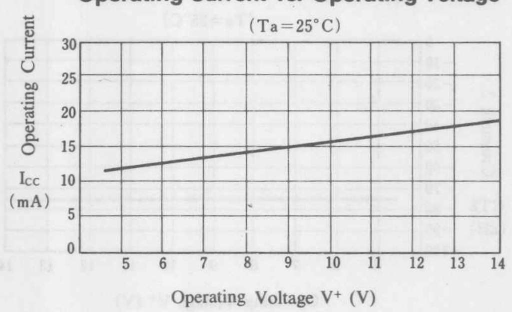
Crosstalk 6 vs. Temperature



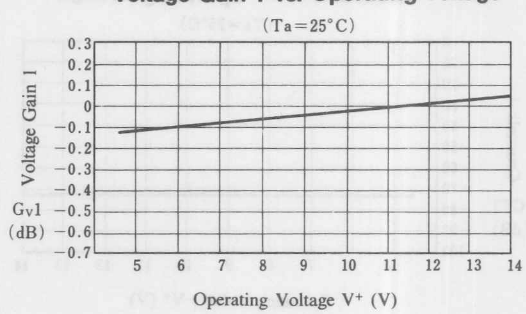
Switch Change Over 1 vs. Temperature



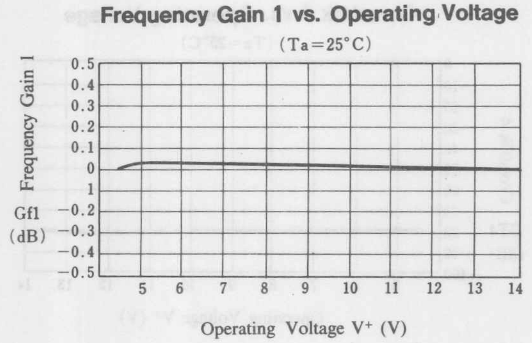
Operating Current vs. Operating Voltage



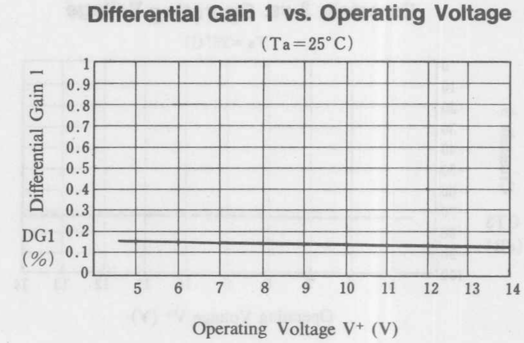
Voltage Gain 1 vs. Operating Voltage



Frequency Gain 1 vs. Operating Voltage

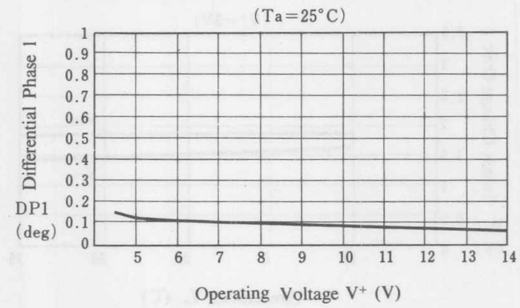


Differential Gain 1 vs. Operating Voltage

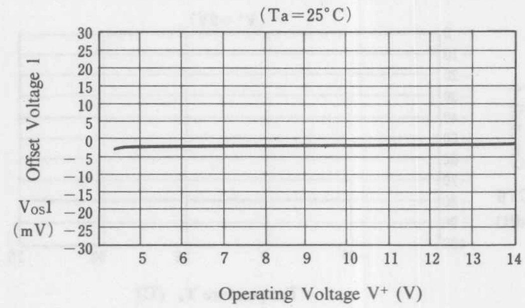


■ TYPICAL CHARACTERISTICS

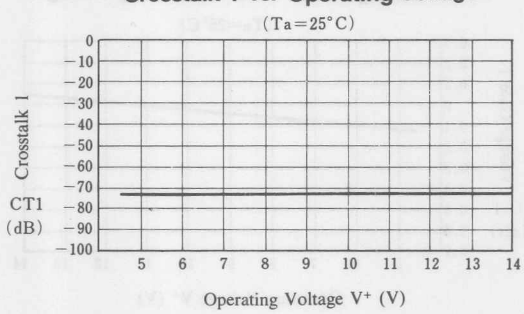
Differential Phase 1 vs. Operating Voltage



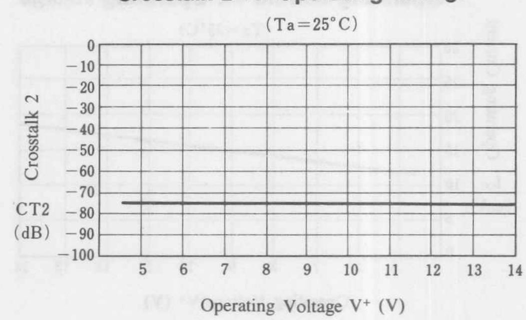
Offset Voltage 1 vs. Operating Voltage



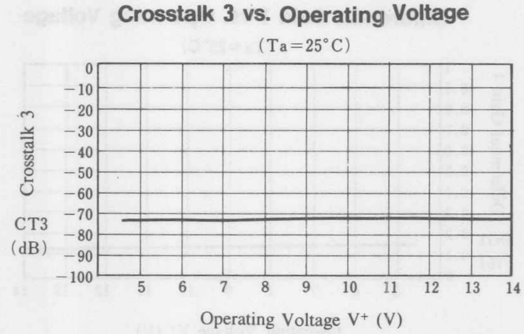
Crosstalk 1 vs. Operating Voltage



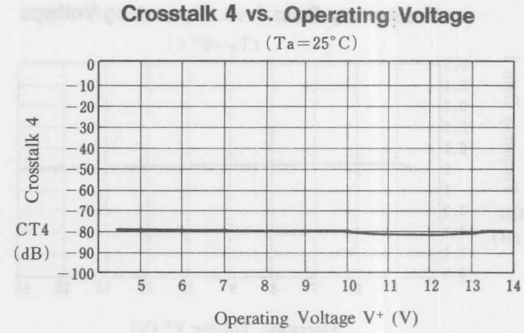
Crosstalk 2 vs. Operating Voltage



Crosstalk 3 vs. Operating Voltage

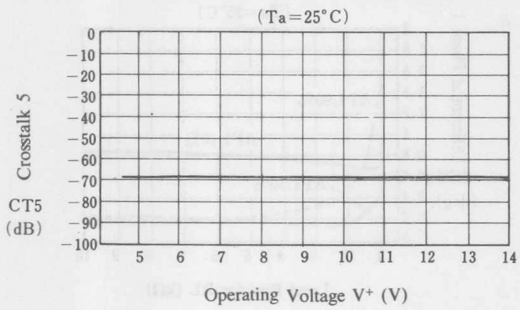


Crosstalk 4 vs. Operating Voltage

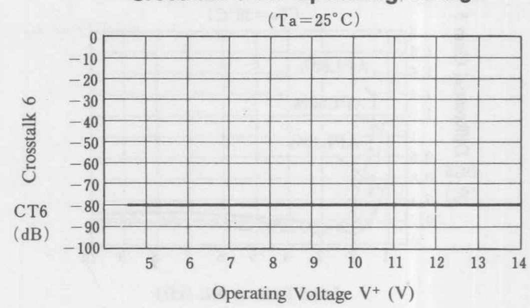


■ TYPICAL CHARACTERISTICS

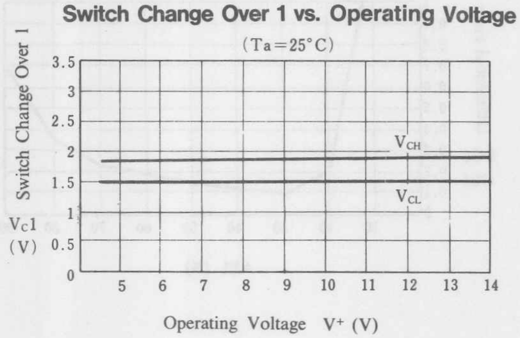
Crosstalk 5 vs. Operating Voltage



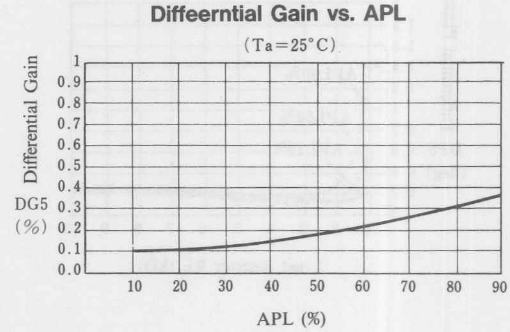
Crosstalk 6 vs. Operating Voltage



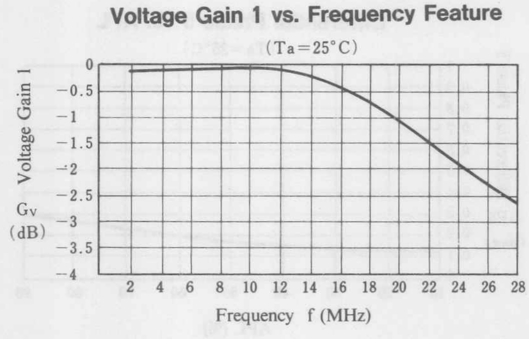
Switch Change Over 1 vs. Operating Voltage



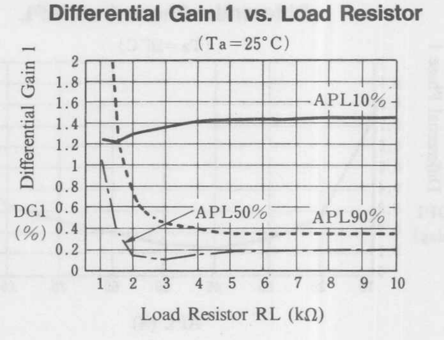
Differntial Gain vs. APL



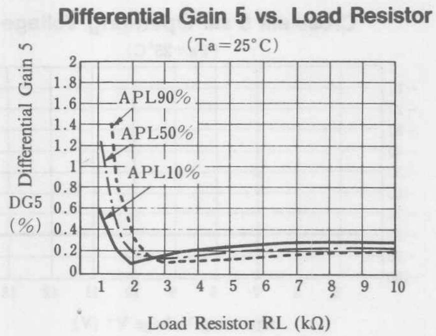
Voltage Gain 1 vs. Frequency Feature

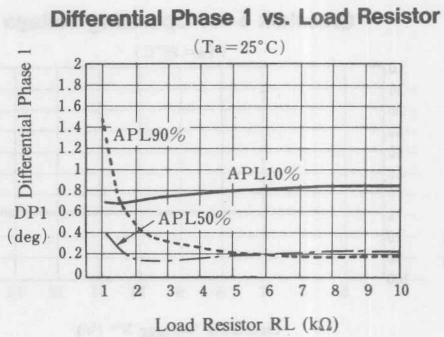


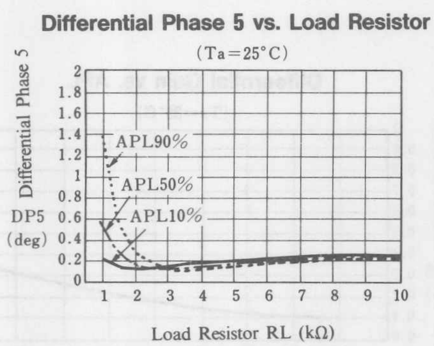
Differential Gain 1 vs. Load Resistor

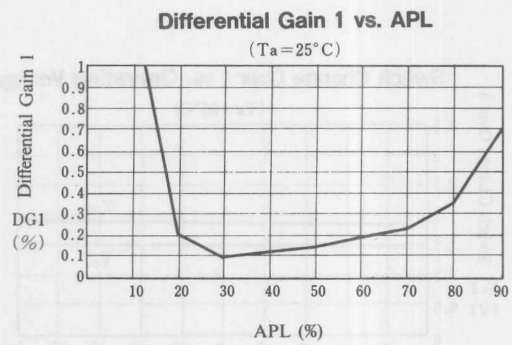


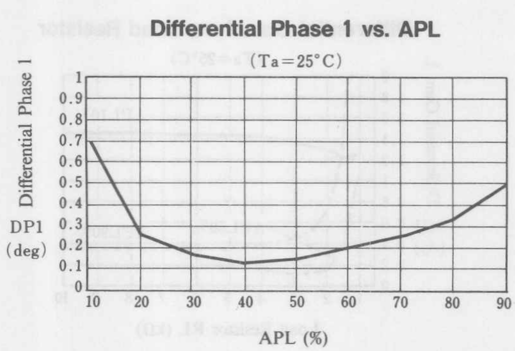
■ TYPICAL CHARACTERISTICS

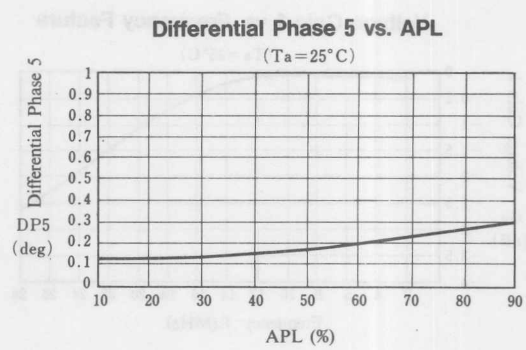






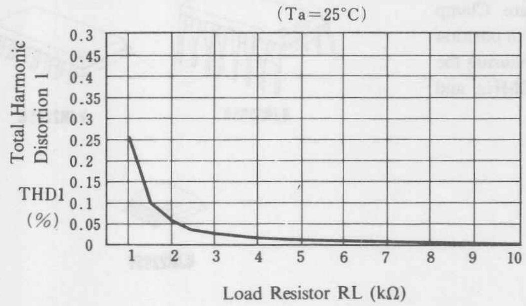






■ TYPICAL CHARACTERISTICS

Total Harmonic Distortion 1 vs. Load Resistor

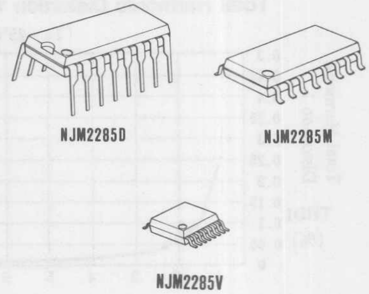


2-INPUT 3CHANNEL VIDEO SWITCH

■ GENERAL DESCRIPTION

NJM2285 is a switching IC for switching over from one audio or video input signal to another. Internalizing 2 inputs, 1 output, and then each set of 3 can be operated independently. Two of them are Clamp type", and they can be operated while setting DC level fixed in position of the video signal. It is a higher efficiency video switch, featuring the operating supply voltage 5 to 12V, the frequency feature 10MHz, and then the crosstalk 75dB (at 4.43MHz).

■ PACKAGE OUTLINE



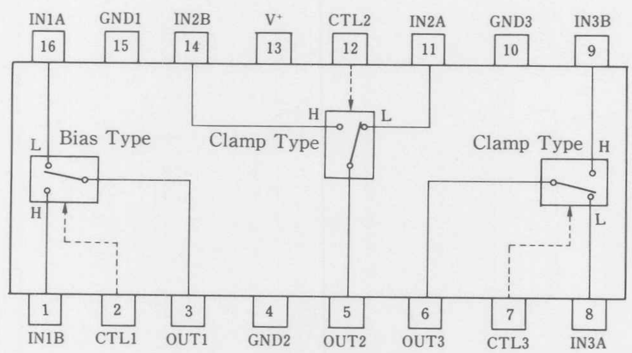
■ FEATURES

- 2 Input-1 Output
  Internalizing 3 Circuits (Two of them are Clamp type).
- Wide Operating Supply Voltage (4.75~13.0V)
- Crosstalk 75dB(at 4.43MHz)
- Wide Bandwidth Frequency Feature 10MHz(2V$_{P-P}$ Input)
- Package Outline DIP16, DMP16, SSOP16
- Bipolar Technology

■ APPLICATIONS

- VCR, Video Camera, AV-TV, Video Disk Player.

■ BLOCK DIAGRAM



NJM2285D
NJM2285M
NJM2285V

■ MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	14	V
Power Dissipation	P_D	(DIP16) 700 (DMP16) 350 (SSOP16) 300	mW mW mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

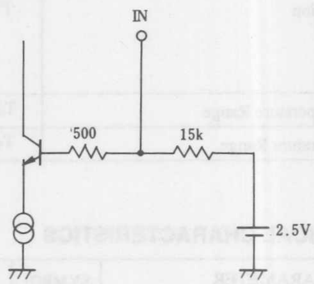
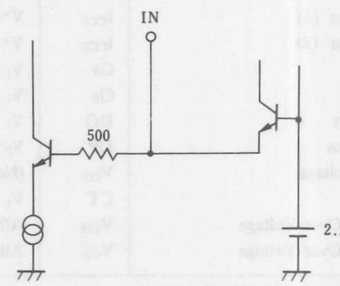
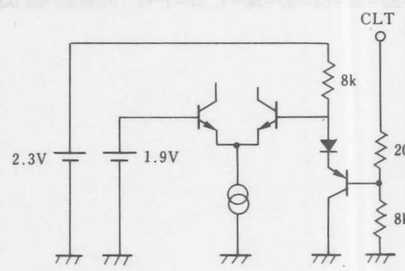
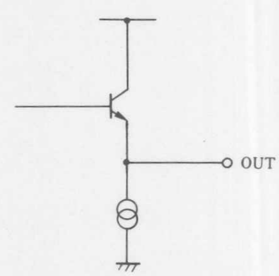
(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	I_{CC1}	V^+=5V (Notel)	8.0	11.4	14.8	mA
Operating Current (2)	I_{CC2}	V^+=9V (Notel)	10.0	14.3	18.6	mA
Voltage Gain	Gv	V_I =100kHz, $2V_{P-P}$,V_O/V_I	−0.6	−0.1	+0.4	dB
Frequency Gain	G_F	V_I =$2V_{P-P}$, V_O(10MHz)/V_O(100kHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_I =$2V_{P-P}$, Standard Staircase Signal	—	0.3	—	%
Differential Phasa	DP	V_I =$2V_{P-P}$, Standard Staircase Signal	—	0.3	—	deg
Output offset Voltage	V_{OS}	(Note2)	−10	0	+10	mV
Crosstalk	CT	V_I =$2V_{P-P}$, 4.43MHz, V_O/V_I	—	−75	—	dB
Switch Change Over Voltage	V_{CH}	All inside Switches ON	2.5	—	—	V
Switch Change Over Voltage	V_{CL}	All inside Switches OFF	—	—	1.0	V

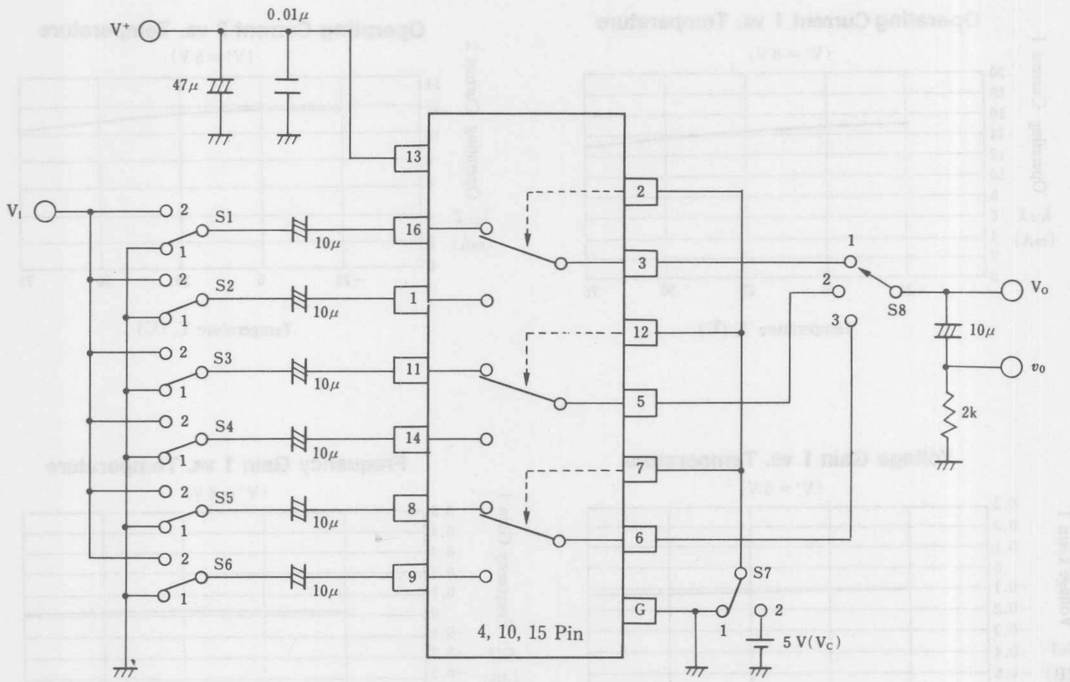
(Notel) S1=S2=S3=S4=S5=S6=S7=1

(Note2) S1=S2=S3=S4=S5=S6=1, S7=1→2 Measure the output DC voltage difference

■ TERMINAL EXPLANATION

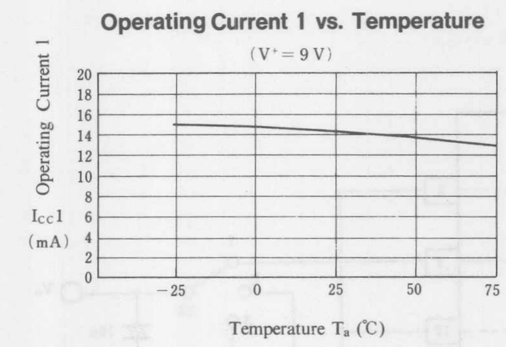
PIN No.	PIN NAME	VOLTAGE	INSIDE EQUIVALENT CIRCUIT
16 1	IN 1 A IN 1 B 〔Input〕	2.5V	
11 14 8 9	IN 2 A IN 2 B IN 3 A IN 3 B 〔Input〕	1.5V	
2 12 7	CTL 1 CTL 2 CTL 3 〔Switching〕		
3	OUT 1	1.8V	
5 6	OUT 2 OUT 3 〔Output〕	0.8V	
13	V+	5 V	
15 4 10	GND 1 GND 2 GND 3		

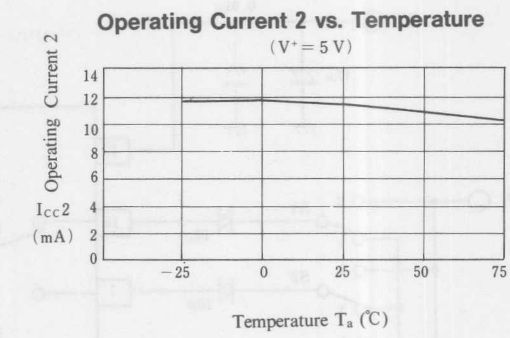
■ TEST CIRCUIT

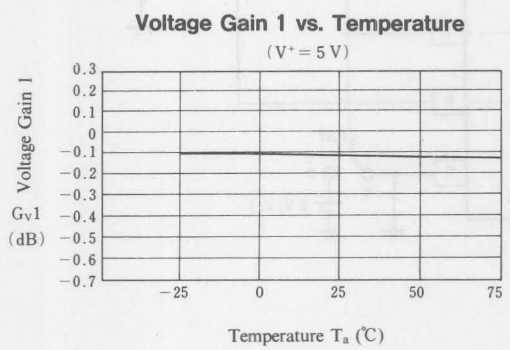


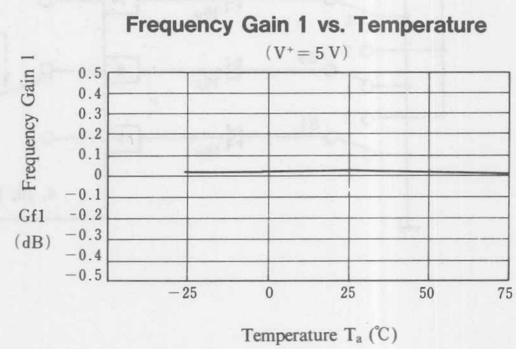
Parameter	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	Test Part
I_{CC1}	1	1	1	1	1	1	1	1	V^+
I_{CC2}	1	1	1	1	1	1	1	1	
G_{v1}	2	1	1	1	1	1	1	1	v_0
G_{f1}	2	1	1	1	1	1	1	1	
DG_1	2	1	1	1	1	1	1	1	
DP_1	2	1	1	1	1	1	1	1	
CT 1	2	1	1	1	1	1	2	1	v_0
CT 2	1	2	1	1	1	1	1	1	
CT 3	1	1	2	1	1	1	2	2	
CT 4	1	1	1	2	1	1	1	2	
CT 5	1	1	1	1	2	1	2	3	
CT 6	1	1	1	1	1	2	1	3	
V_{OS1}	1	1	1	1	1	1	1/2	1	V_O
V_{C1}	1/2	2/1	1	1	1	1	V_C	1	V_C
THD	2	1	1	1	1	1	1	1	v_0

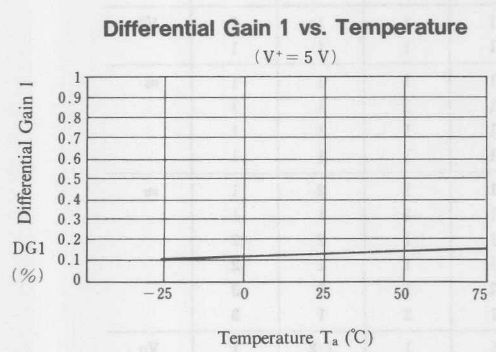
■ TYPICAL CHARACTERISTICS

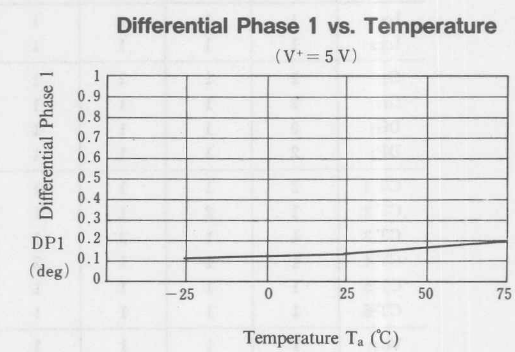






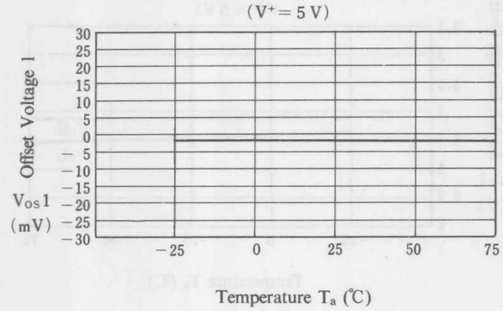




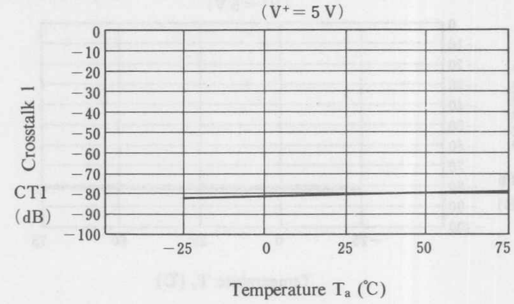


■ TYPICAL CHARACTERISTICS

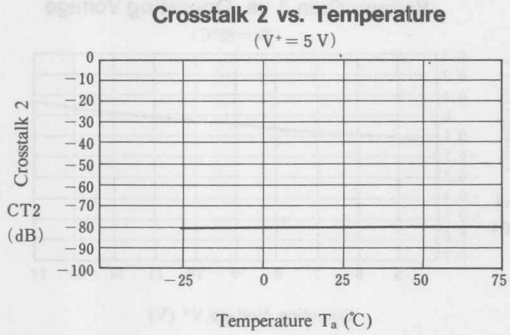
Offset Voltage 1 vs. Temperature



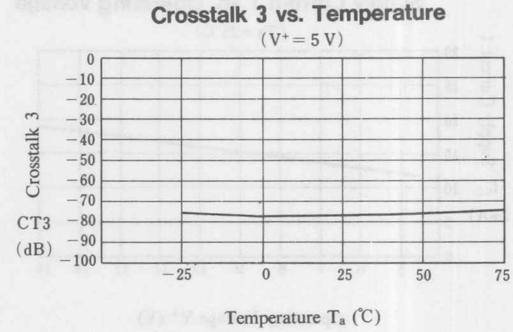
Crosstalk 1 vs. Temperature



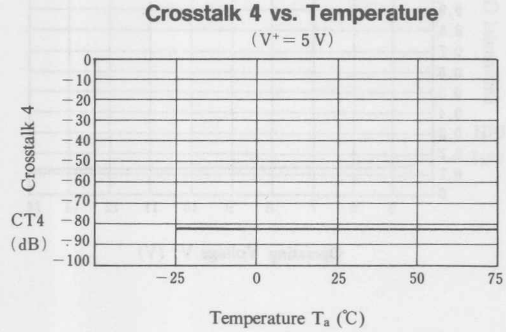
Crosstalk 2 vs. Temperature



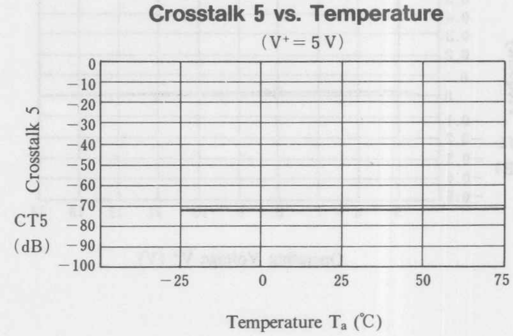
Crosstalk 3 vs. Temperature



Crosstalk 4 vs. Temperature

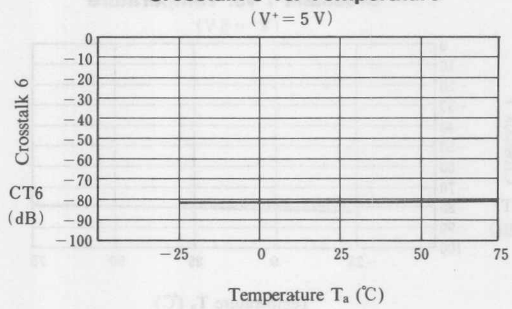


Crosstalk 5 vs. Temperature

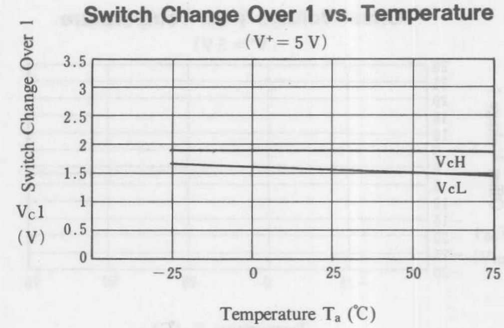


■ TYPICAL CHARACTERISTICS

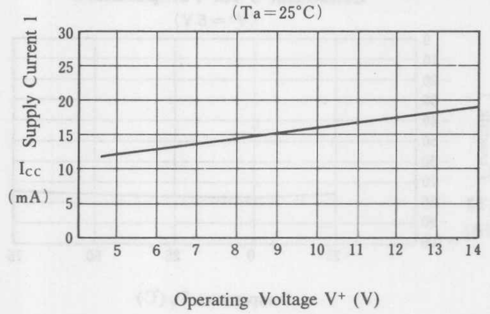
Crosstalk 6 vs. Temperature



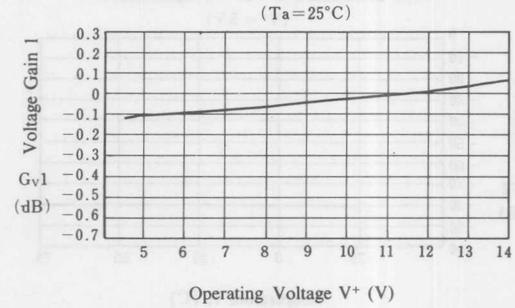
Switch Change Over 1 vs. Temperature



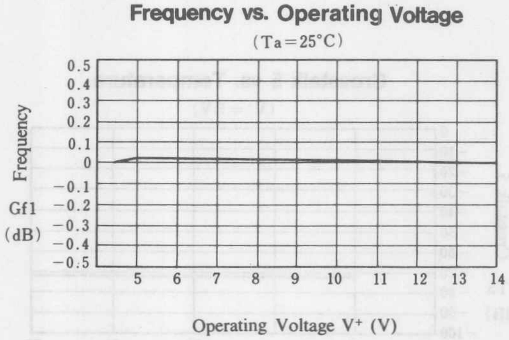
Supply Current 1 vs. Operating Voltage



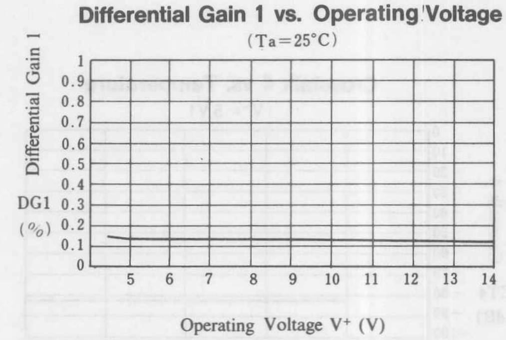
Voltage Gain 1 vs. Operating Voltage



Frequency vs. Operating Voltage

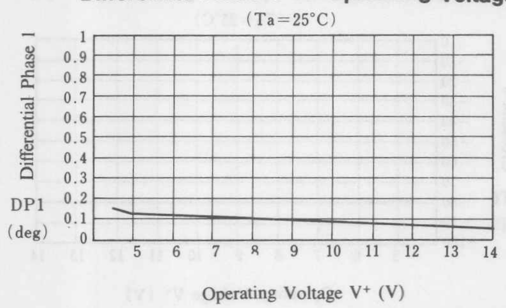


Differential Gain 1 vs. Operating Voltage

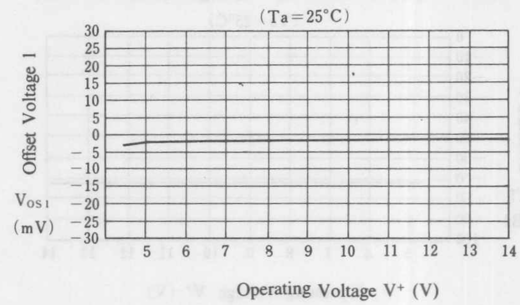


■ TYPICAL CHARACTERISTICS

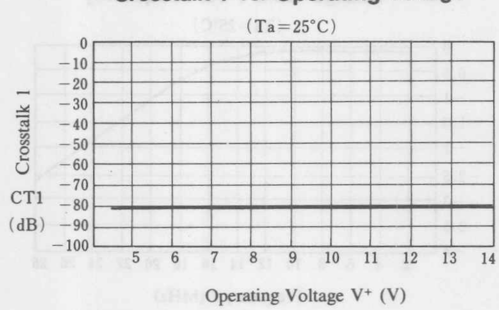
Differential Phase 1 vs. Operating Voltage



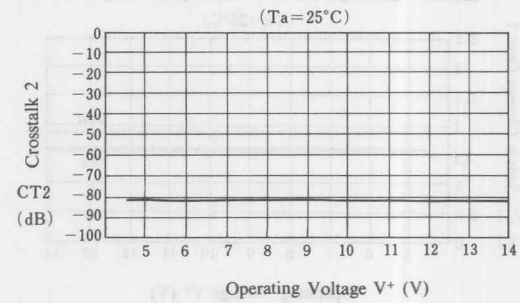
Offset Voltage 1 vs. Operating Voltage



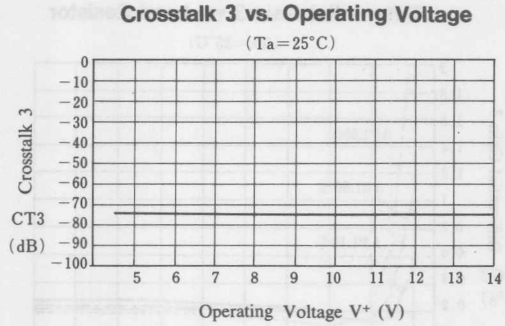
Crosstalk 1 vs. Operating Voltage



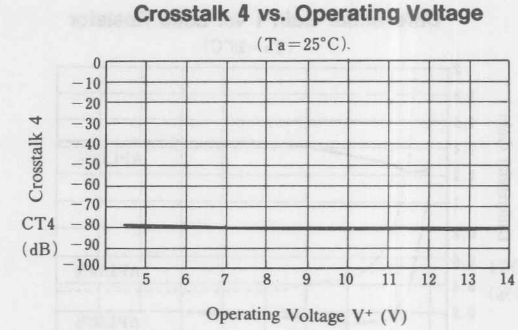
Crosstalk 2 vs. Operating Voltage



Crosstalk 3 vs. Operating Voltage

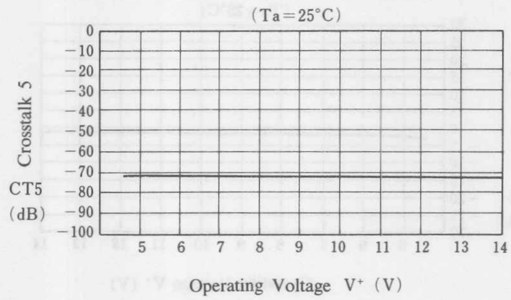


Crosstalk 4 vs. Operating Voltage

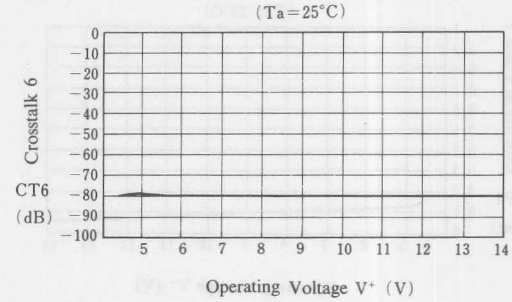


■ TYPICAL CHARACTERISTICS

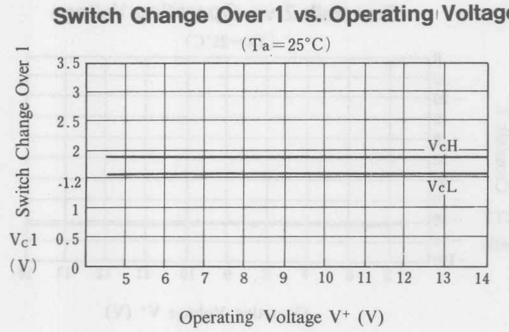
Crosstalk 5 vs. Operating Voltage V+ (V)



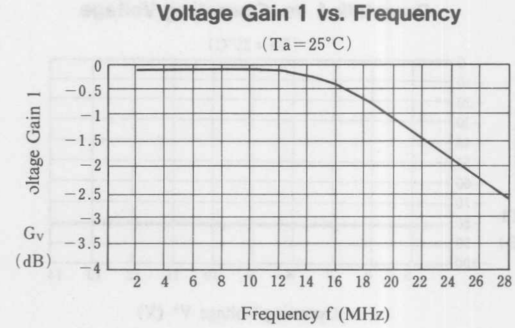
Crosstalk 6 vs. Operating Voltage V+ (V)



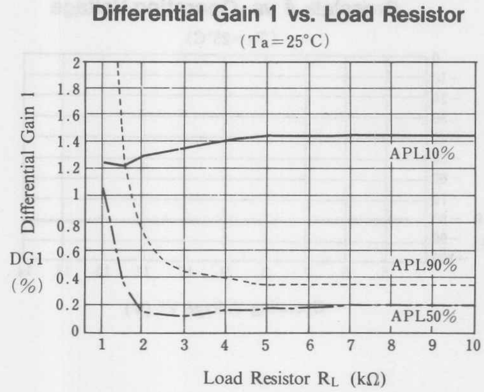
Switch Change Over 1 vs. Operating Voltage



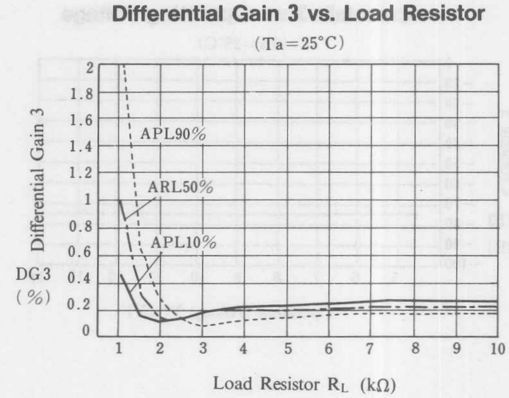
Voltage Gain 1 vs. Frequency



Differential Gain 1 vs. Load Resistor



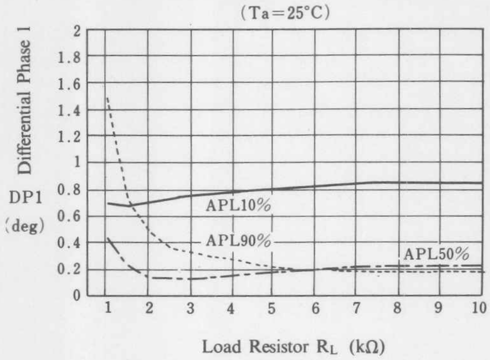
Differential Gain 3 vs. Load Resistor



■ TYPICAL CHARACTERISTICS

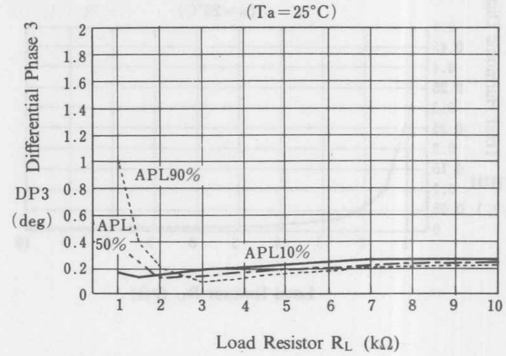
Differential Phase 1 vs. Load Resistor

(Ta=25°C)



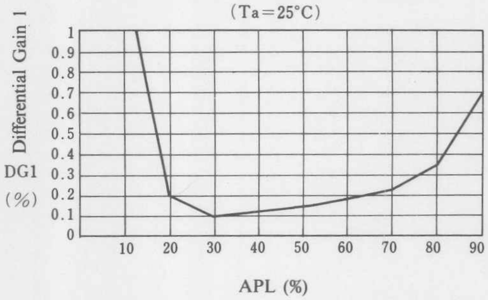
Differential Phase 3 vs. Load Resistor

(Ta=25°C)



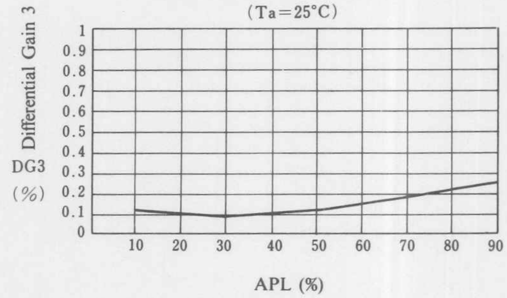
Differential Gain 1 vs. APL

(Ta=25°C)



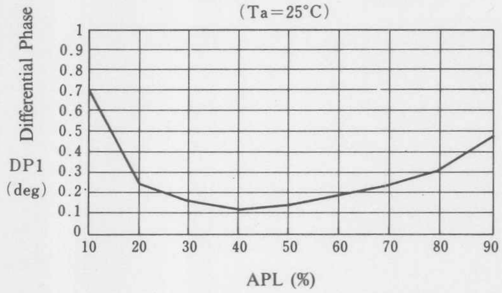
Differential Gain 3 vs. APL

(Ta=25°C)



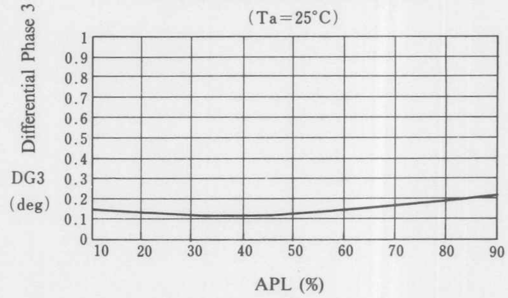
Differential Phase 1 vs. APL

(Ta=25°C)

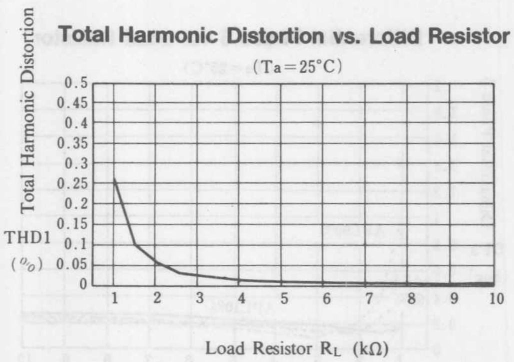


Differential Phase 3 vs. APL

(Ta=25°C)



■ TYPICAL CHARACTERISTICS

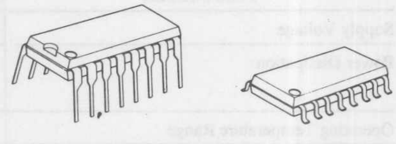


2-INPUT 3CHANNEL VIDEO SWITCH

■ GENERAL DESCRIPTION

NJM2286 is a switching IC for switching over from one audio or video input signal to another. Internalizing 2 inputs, 1 output, and then each set of 3 can be operated independently. They are a Clamp type" and it can be operated while DC level fixed in position of the video signal. It is a higher efficiency video switch, featuring the operating supply voltage 4.75 to 13.0V, the frequency feature 10MHz, and then the Crosstalk 75dB (at 4.43MHz).

■ PACKAGE OUTLINE



NJM2286D NJM2286M

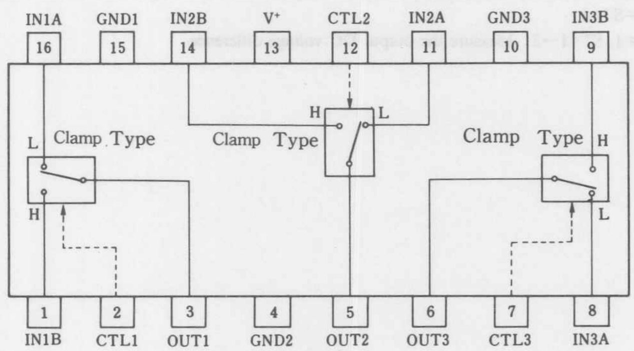
■ FEATURES

- 2 Input-1 Output Internalizing 3 Circuits (Clamp type).
- Wide Operating Voltage (4.75～13.0V)
- Crosstalk 75dB(at 4.43MHz)
- Wide Bandwidth Frequency Feature 10MHz(2V_{P-P} Input)
- Package Outline DIP16, DMP16
- Bipolar Technology

■ APPLICATIONS

- VCR, Video Camera, AV-TV, Video Disk Player.

■ BLOCK DIAGRAM



NJM2286D
NJM2286M

■ MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	14	V
Power Dissipation	P_D	(DIP16) 700 (DMP16) 350	mW mW
Operating Temperature Range	T_{opr}	−20∼+75	℃
Storage Temperature Range	T_{stg}	−40∼+125	℃

■ ELECTRICAL CHARACTERISTICS

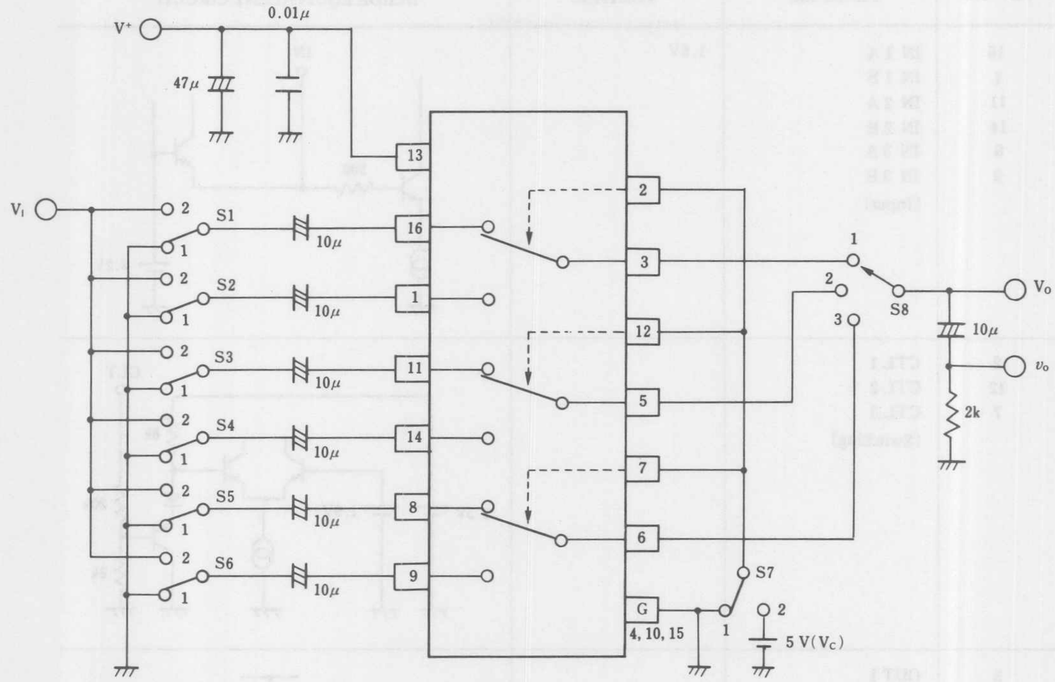
(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	I_{CC1}	V^+=5V (Note1)	8.0	11.4	14.8	mA
Operating Current (2)	I_{CC2}	V^+=9V (Note1)	10.0	14.3	18.6	mA
Voltage Gain	G_V	V_I =100kHz, $2V_{P-P}$, V_O/V_I	−0.6	−0.1	+0.4	dB
Frequency Gain	G_F	V_I =$2V_{P-P}$, V_O(10MHz)/V_O(100kHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_I =$2V_{P-P}$, Standard Staircase Signal	—	0.3	—	%
Differential Phasa	DP	V_I =$2V_{P-P}$, Standard Staircase Signal	—	0.3	—	deg
Output Offset Voltage	V_{OS}	(Note2)	−10	0	+10	mV
Crosstalk	CT	V_I =$2V_{P-P}$, 4.43MHz, V_O/V_I	—	−75	—	dB
Switch Change Over Voltage	V_{CH}	All inside Switch ON	2.5	—	—	V
Switch Change Over Voltage	V_{CL}	All inside Switch OFF	—	—	1.0	V

(Note1) S1=S2=S3=S4=S5=S6=S7=1

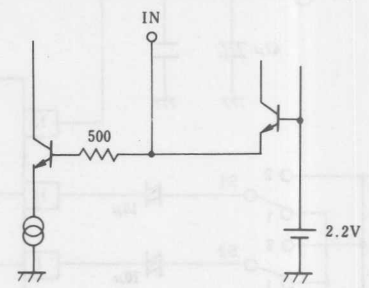
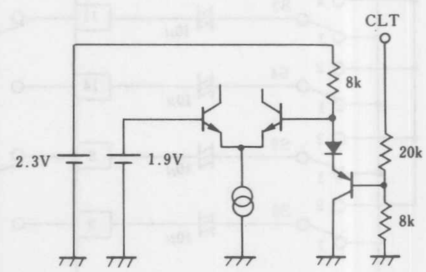
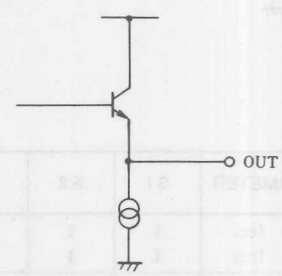
(Note2) S1=S2=S3=S4=S5=S6=1, S7=1→2 Measure the output DC voltage difference

■ TEST CIRCUIT



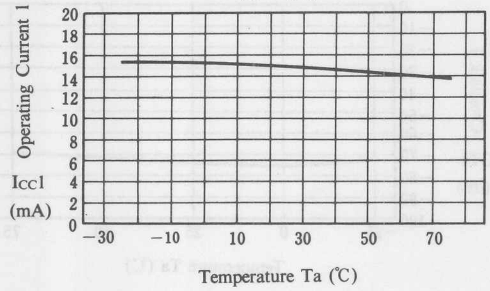
PARAMETER	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	TEST PART
I_{CC1}	1	1	1	1	1	1	1	1	V^+
I_{CC2}	1	1	1	1	1	1	1	1	
G_{v1}	2	1	1	1	1	1	1	1	v_O
G_{f1}	2	1	1	1	1	1	1	1	
DG_1	2	1	1	1	1	1	1	1	
DP_1	2	1	1	1	1	1	1	1	
CT 1	2	1	1	1	1	1	2	1	v_O
CT 2	1	2	1	1	1	1	1	1	
CT 3	1	1	2	1	1	1	2	2	
CT 4	1	1	1	2	1	1	1	2	
CT 5	1	1	1	1	2	1	2	3	
CT 6	1	1	1	1	1	2	1	3	
V_{OS1}	1	1	1	1	1	1	1/2	1	V_O
V_{C1}	1/2	2/1	1	1	1	1	V_C	1	V_C
THD	2	1	1	1	1	1	1	1	v_O

■ TERMINAL EXPLANATION

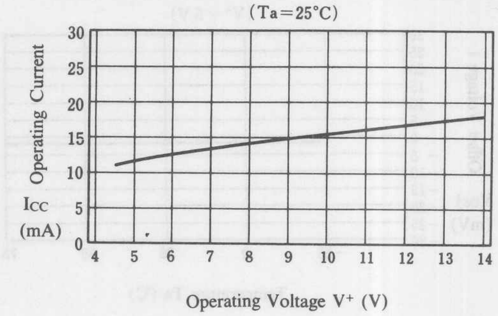
PIN No.	PIN NAME	VOLTAGE	INSIDE EQUIVALENT CIRCUIT
16 1 11 14 8 9	IN 1 A IN 1 B IN 2 A IN 2 B IN 3 A IN 3 B 〔Input〕	1.5V	
2 12 7	CTL 1 CTL 2 CTL 3 〔Switching〕		
3 5 6	OUT 1 OUT 2 OUT 3 〔Output〕	0.8V	
13	V^+	5 V	
15 4 10	GND 1 GND 2 GND 3		

■ TYPICAL CHARACTERISTICS

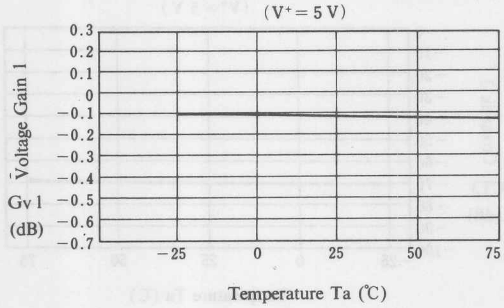
Operating Current 1 vs. Temperature
($V^+=9V$)



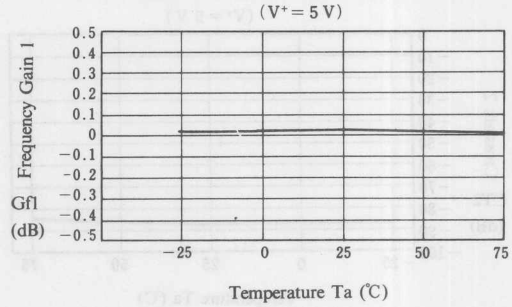
Operating Current vs. Operating Voltage
(Ta=25°C)



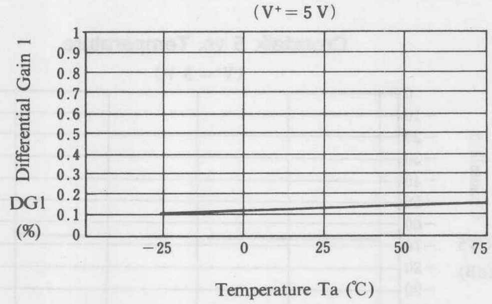
Voltage Gain 1 vs. Temperature
($V^+=5$ V)



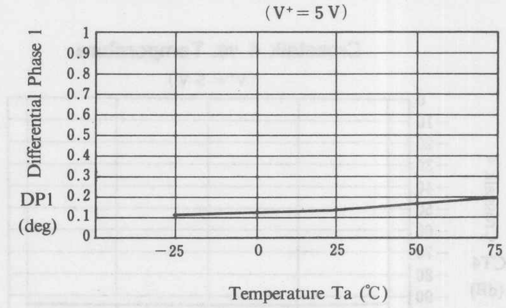
Frequency Gain 1 vs. Temperature
($V^+=5$ V)



Differential Gain 1 vs. Temperature
($V^+=5$ V)

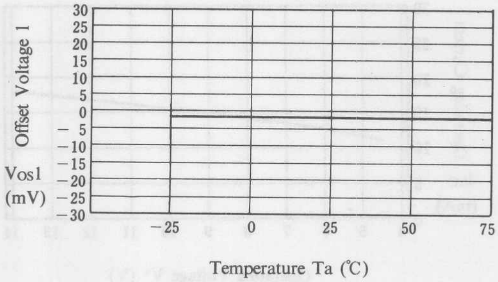


Differential Phase 1 vs. Temperature
($V^+=5$ V)

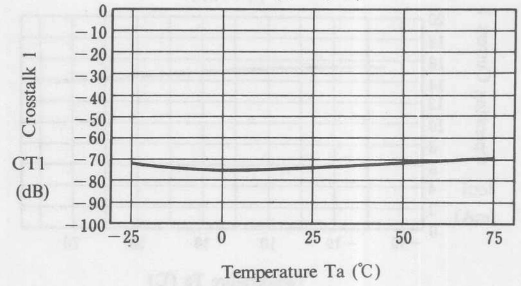


■ TYPICAL CHARACTERISTICS

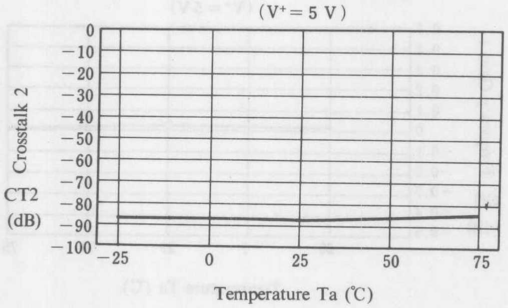
Offset Voltage vs. Temperature
(V^+ = 5 V)



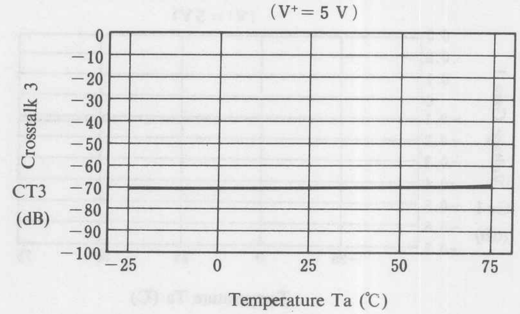
Crosstalk 1 vs. Temperature
(V^+ = 5 V)



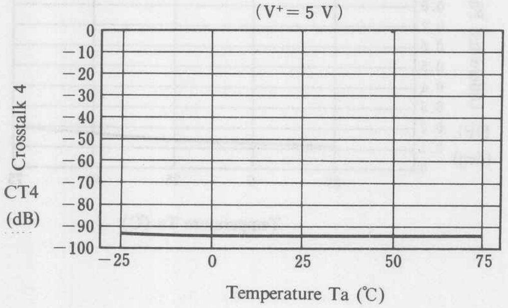
Crosstalk 2 vs. Temperature
(V^+ = 5 V)



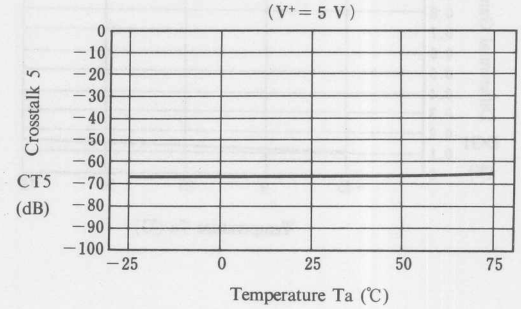
Crosstalk 3 vs. Temperature
(V^+ = 5 V)



Crosstalk 4 vs. Temperature
(V^+ = 5 V)

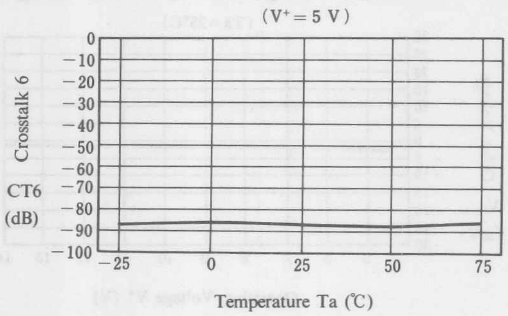


Crosstalk 5 vs. Temperature
(V^+ = 5 V)

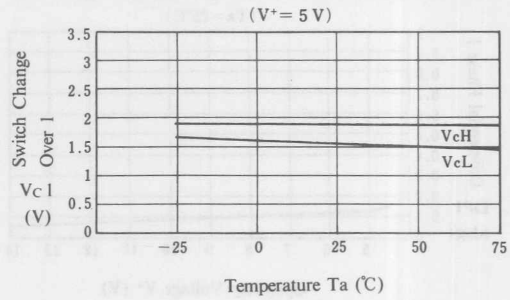


■ TYPICAL CHARACTERISTICS

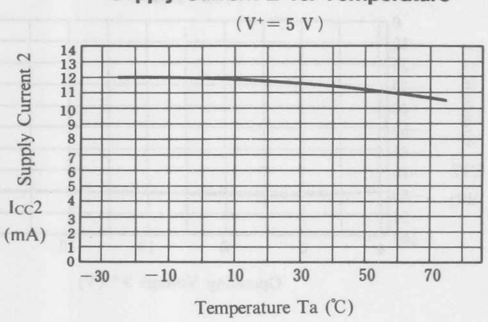
Crosstalk 6 vs. Temperature



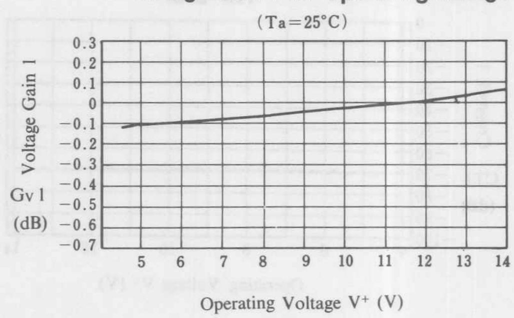
Switch Change Over 1 vs. Temperature



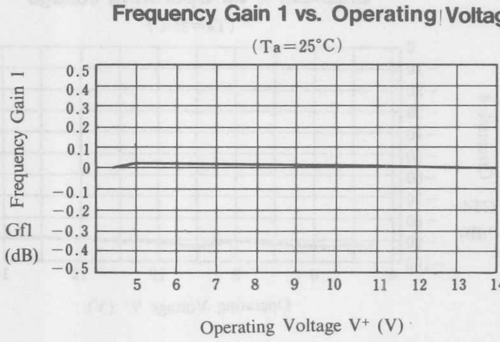
Supply Current 2 vs. Temperature



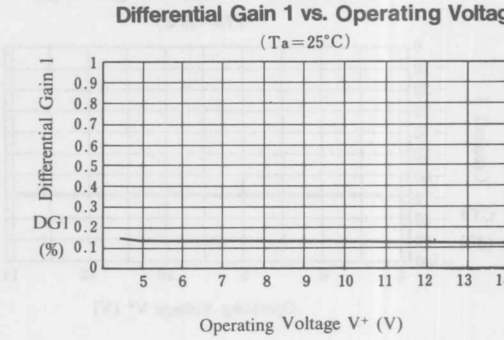
Voltage Gain 1 vs. Operating Voltage



Frequency Gain 1 vs. Operating Voltage

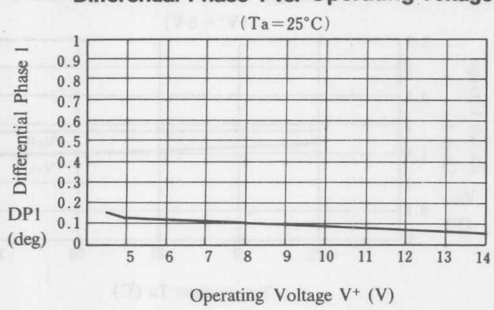


Differential Gain 1 vs. Operating Voltage

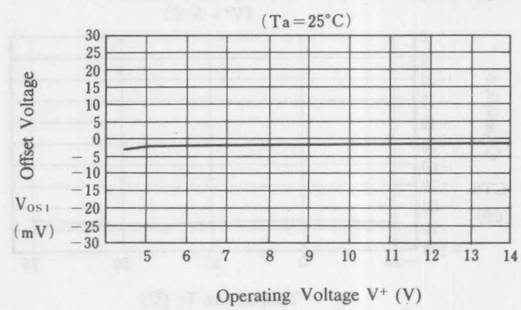


■ TYPICAL CHARACTERISTICS

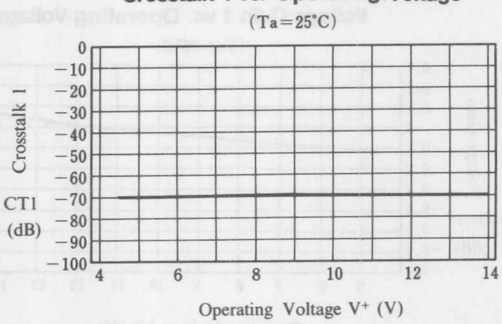
Differential Phase 1 vs. Operating Voltage



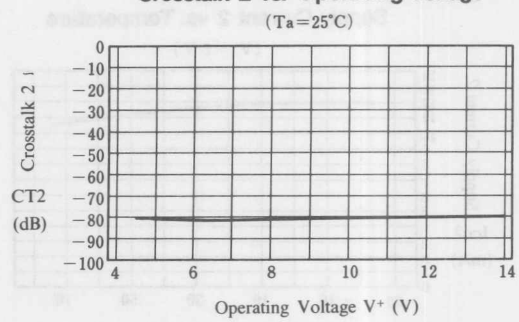
Offset Voltage 1 vs. Operating Voltage



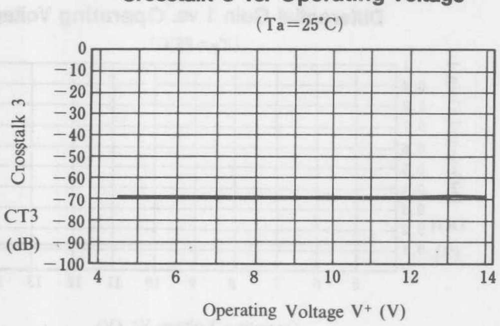
Crosstalk 1 vs. Operating Voltage



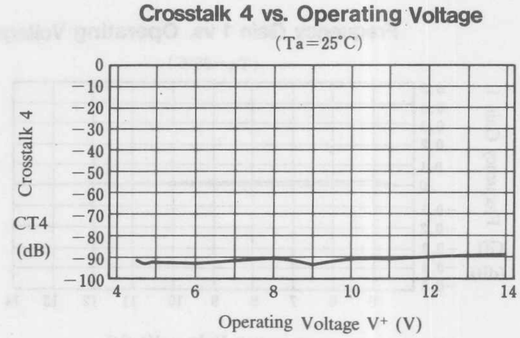
Crosstalk 2 vs. Operating Voltage



Crosstalk 3 vs. Operating Voltage

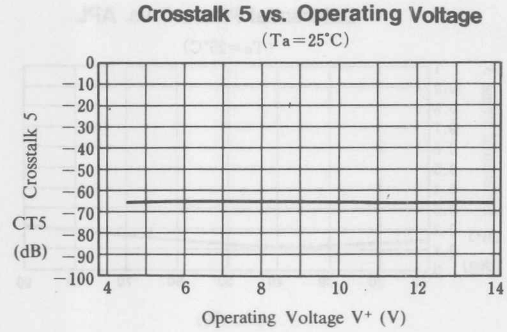


Crosstalk 4 vs. Operating Voltage

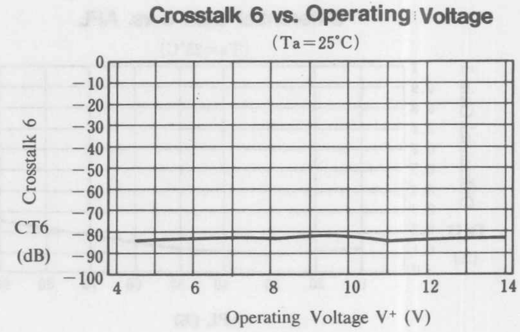


■ TYPICAL CHARACTERISTICS

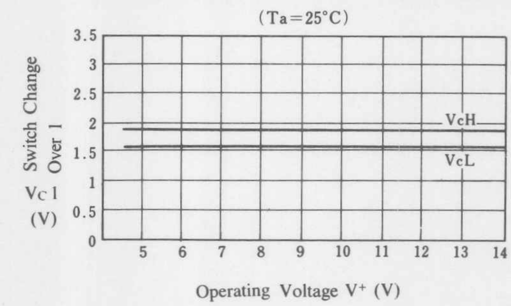
Crosstalk 5 vs. Operating Voltage



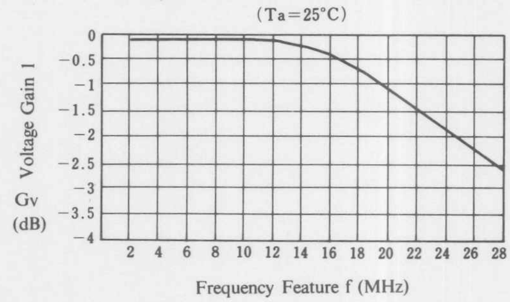
Crosstalk 6 vs. Operating Voltage



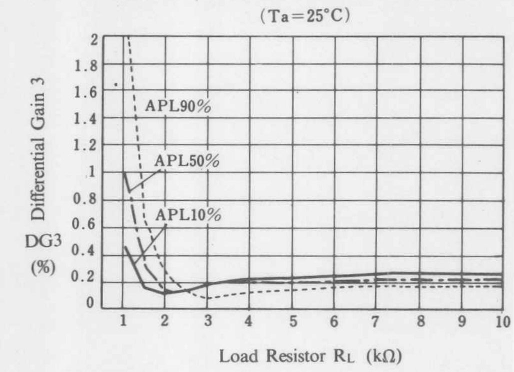
Switch Change Over 1 vs. Operating Voltage



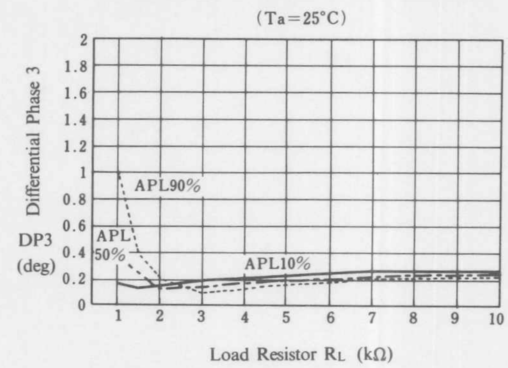
Voltage Gain 1 vs. Frequency Feature



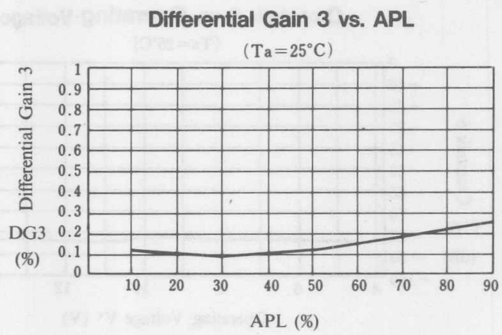
Differential Gain 3 vs. Load Resistor

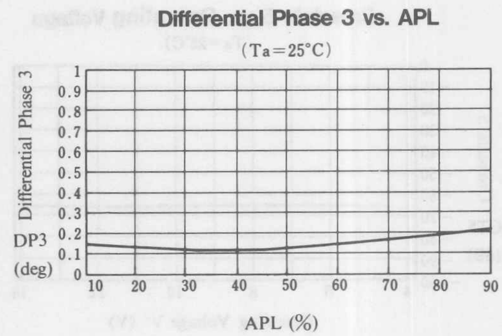


Differential Phase 3 vs. Load Resistor



■ TYPICAL CHARACTERISTICS



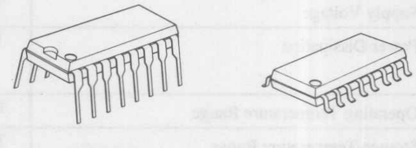


4-INPUT 1MUTE VIDEO SWITCH

■ GENERAL DESCRIPTION

The NJM2293 is a switching IC for switching over from one audio or video input signal to another. It is a higher efficiency video switch, featuring the operating voltage 4.75 to 13V, the frequency feature 7MHz, and then the Crosstalk 75dB (at 4.43MHz).

■ PACKAGE OUTLINE



NJM2293D NJM2293M

■ FEATURES

- 4 Input-1 Output
- Operating Voltage (+4.75V~+13V)
- Crosstalk 75dB(at 4.43MHz)
- Wide Bandwidth Frequency 7MHz(2V_{P-P} Input)
- Package Outline DIP16, DMP16.
- Bipolar Technology

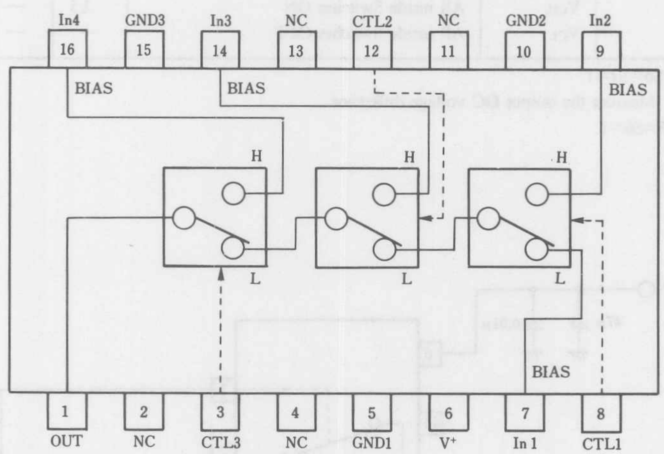
■ RECOMMENDED OPERATING CONDITION

- Operating Voltage V^+ 4.75~13.0V

■ APPLICATIONS

- VCR, Video Camera, AV-TV, Video Disk Player.

■ BLOCK DIAGRAM



NJM2293D
NJM2293M

■ MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	14	V
Power Dissipation	P_D	(DIP-16) 700	mW
		(DMP-16) 350	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	$I_{CC}1$	V^+=5V (Note1)	4.5	6.5	8.5	mA
Operating Current (2)	$I_{CC}2$	V^+=9V (Note1)	5.8	8.3	10.8	mA
Voltage Gain	G_V	V_I =100kHz, $2V_{P-P}$, V_O/V_I	−0.7	−0.2	+0.3	dB
Frequency Gain (1)	G_F1	V_I =$2V_{P-P}$, V_O(7MHz)/V_O(100kHz)	−1.0	0	+1.0	dB
Frequency Gain (2)	G_F2	V_I =$1V_{P-P}$, V_O(10MHz)/V_O(100kHz)	—	0	—	dB
Differential Gain	DG	V_I =$2V_{P-P}$, Standerd Staircase Signal	—	0.3	—	%
Differential Phasa	DP	V_I =$2V_{P-P}$, Standerd Staircase Signal	—	0.3	—	deg
OutPut offset Voltage	V_{OS}	(Note2)	−4.5	0	+45	mV
Crosstalk	CT	V_I =$2V_{P-P}$, 4.43MHz, V_O/V_I	—	−75	—	dB
Switch Change Over Voltage	V_{CH}	All inside Switches ON	2.5	—	—	V
Switch Change Over Voltage	V_{CL}	All inside Switches OFF	—	—	1.0	V

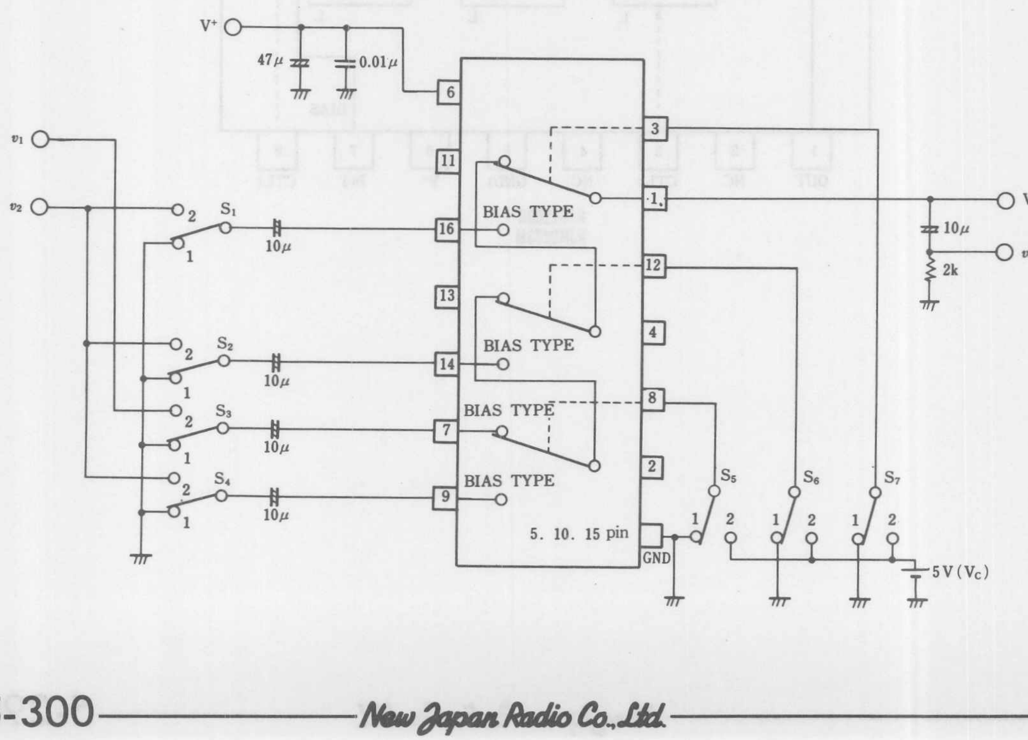
(Note1) S1=S2=S3=S4=S5=S6=S7=1

(Note2) S1=S2=S3=S4=1 Measure the output DC voltage difference

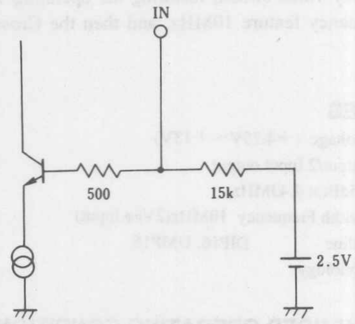
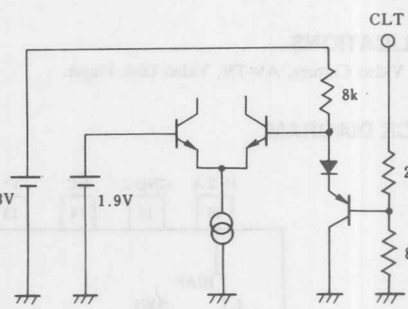
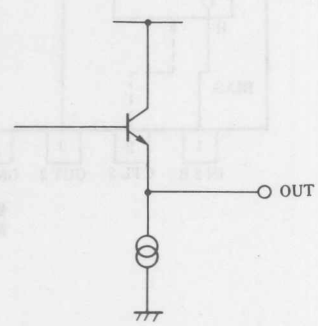
a) S5=S6=S7=1, b) S7=2, S5=S6=1

c) S6=2, S5=1 d) S5=2

■ TEST CIRCUIT



■ TERMINAL EXPLANATION

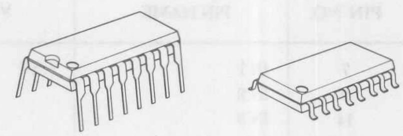
PIN NO.	PIN NAME	VOLTAGE	INSIDE EQUIVALENT CIRCUIT
7 9 14 16	IN 1 IN 2 IN 3 IN 4 〔Input〕	2.5V	
8 12 3	CTL1 CTL2 CTL3 〔Switching〕		
1	OUT 〔Output〕	1.8V	
6	V+	5 V	
5 10 15	GND 1 GND 2 GND 3		

3-INPUT/2-INPUT VIDEO SWITCH

■ GENERAL DESCRIPTION

The NJM2503 is a switching IC for switching over from one audio or video input signal to another. Internalizing 3 input-1 output, and 2 input-1 output and then each set can be operated independently. It is a higher efficiency video switch, featuring the operating voltage 4.75 to 13V, the frequency feature 10MHz, and then the Crosstalk 75dB (at 4.43MHz).

■ PACKAGE OUTLINE



NJM2503D NJM2503M

■ FEATURES

- Operating Voltage (+4.75V ~ +13V)
- 3 Input-1 Output/2 Input output
- Crosstalk 75dB(at 4.43MHz)
- Wide Bandwidth Frequency 10MHz(2V_{P-P} Input)
- Package Outline DIP16, DMP16
- Bipolar Technology

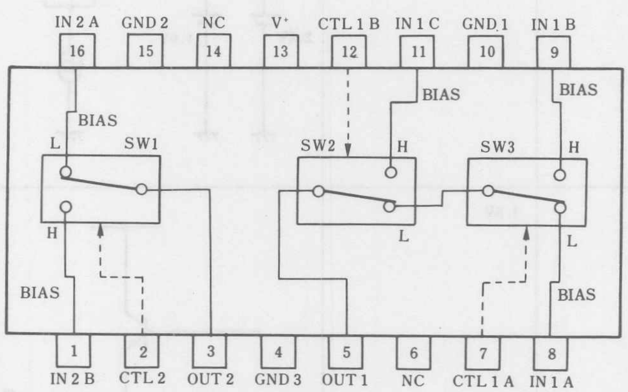
■ RECOMMENDED OPERATING CONDITION

- Operating Voltage V^+ 4.75~13.0V

■ APPLICATIONS

- VCR, Video Camera, AV-TV, Video Disk Player.

■ BLOCK DIAGRAM



NJM2503D
NJM2503M

■ MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	14	V
Power Dissipation	P_D	(DIP 16) 700	mW
		(DMP 16) 350	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

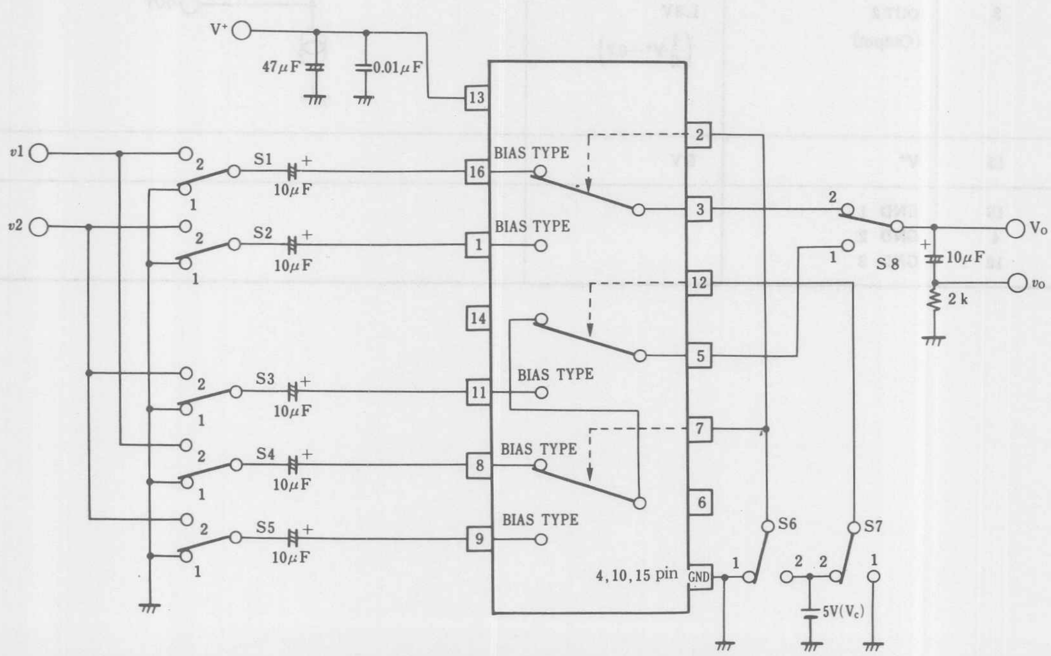
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	$I_{CC}1$	V^+=5V (Note1)	6.8	9.8	12.8	mA
Operating Current (2)	$I_{CC}2$	V^+=9V (Note1)	8.7	12.5	16.3	mA
Voltage Gain	G_V	V_I =100kHz, $2V_{P-P}$, V_O/V_I	−0.6	−0.1	+0.4	dB
Frequency Gain	G_F 1	V_I =$2V_{P-P}$, V_O(10MHz)/V_O(100kHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_I =$2V_{P-P}$, Standerd Staircase Signal	—	0.3	—	%
Differential Phasa	DP	V_I =$2V_{P-P}$, Standerd Staircase Signal	—	0.3	—	deg
OutPut offset Voltage (1)	$V_{OS}1$	(Note2)	−10	0	+10	mV
OutPut offset Voltage (2)	$V_{OS}2$	(Note3)	−25	0	+25	mV
Crosstalk	CT	V_I =$2V_{P-P}$, 4.43MHz, V_O/V_I	—	−75	—	dB
Switch Change Over Voltage	V_{CH}	All inside Switches ON	2.5	—	—	V
Switch Change Over Voltage	V_{CL}	All inside Switches OFF	—	—	1.0	V

(Note1) S1=S2=S3=S4=S5=S6=S7=1

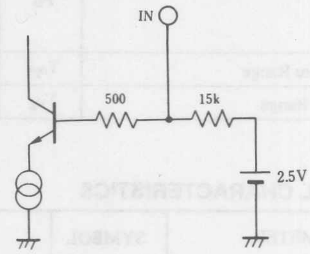
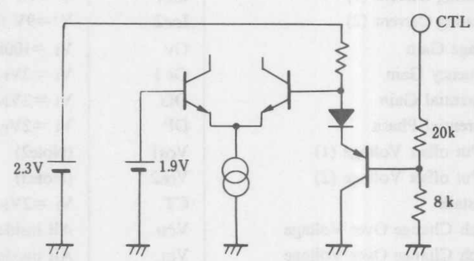
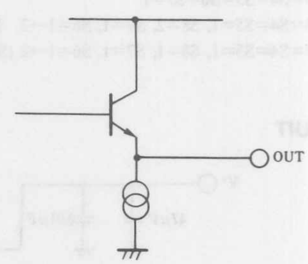
(Note2) S1=S2=S3=S4=S5=1, S8=2, S7=1, S6=1→2 Measure the output DC voltage difference

(Note3) S1=S2=S3=S4=S5=1, S8=1, S7=1, S6=1→2 (S6=1, S7=1→2) Measure the output DC voltage difference

■ TEST CIRCUIT



■ TERMINAL EXPLANATION

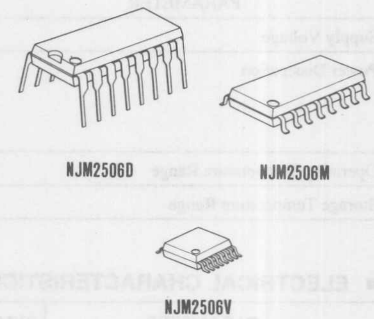
PIN No.	PIN NAME	VOLTAGE	INSIDE EQUIVALENT CIRCUIT
8 9 11 16 1	IN 1 A IN 1 B IN 1 C IN 2 A IN 2 B 〔Input〕	2.5V $\left(\frac{1}{2}V^{+}\right)$	
7 12 2	CTL 1 A CTL 1 B CTL 2 〔Switching〕		
5	OUT 1 〔Output〕	1.8V $\left(\frac{1}{2}V^{+}-0.7\right)$	
3	OUT 2 〔Output〕	1.8V $\left(\frac{1}{2}V^{+}-0.7\right)$	
13	V^{+}	5 V	
15 4 10	GND 1 GND 2 GND 3		

3-INPUT/2-INPUT VIDEO SWITCH

■ GENERAL DESCRIPTION

The NJM2506 is video switch for video and audio signal. It contains 3 input-1 output and 2 input-1 output video switch. 3 input-1 output switch has clamp function and so is applied to fixed DC level of video signal. Its operatiing voltage is 4.75 to 13V and bahdwidth is 10MHz. Crosstalk is 75dB (at f=4.43MHz).

■ PACKAGE OUTLINE



■ FEATURES

- Wide Operating Supply Range (+4.75V ~ +13V)
- 3 Input-1 Output and 2 Input-1 Output
- Internal Clamp Function
- Crosstalk 75dB(at 4.43MHz)
- Wide Frequency Range 10MHz($2V_{P-P}$ Input)
- Package Outline DIP16, DMP16, SSOP16
- Bipolar Technology

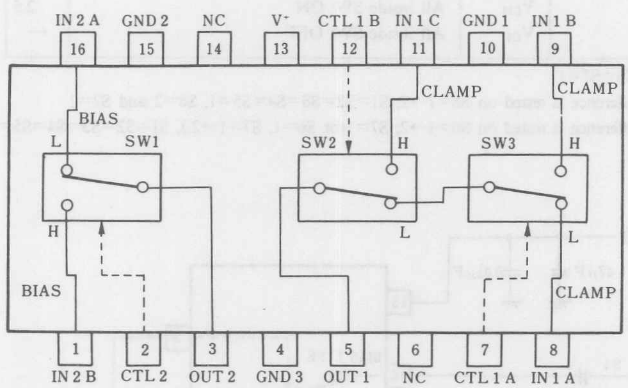
■ RECOMMENDED OPERATING CONDITION

- Operating Voltage V^+ 4.75~13.0V

■ APPLICATION

- VCR, Video Camera, AV-TV, Video Disk Player.

■ BLOCK DIAGRAM



NJM2506D
NJM2506M
NJM2506V

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	14	V
Power Dissipation	P_D	(DIP16) 700	mW
		(DMP16) 350	mW
		(SSOP16) 300	mW
Operating Temperature Range	T_{opr}	−20∼+75	℃
Storage Temperature Range	T_{stg}	−40∼+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

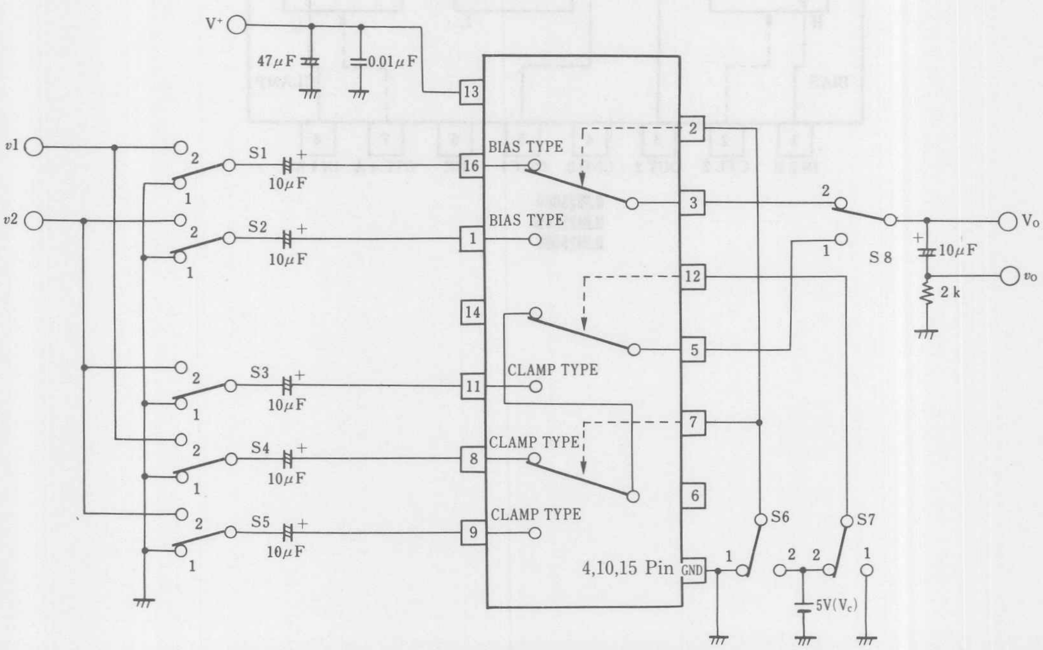
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	I_{CC1}	V^+=5V (Note1)	6.7	9.7	12.7	mA
Operating Current (2)	I_{CC2}	V^+=9V (Note1)	8.6	12.3	16.0	mA
Voltage Gain	G_V	V_I =2V_{P-P}/100khz, V_O/V_I	−0.6	−0.1	+0.4	dB
Frequency Response	G_f	V_I =2V_{P-P}, V_O(10MHz/100kHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_I =2V_{P-P}, Staircase Signal	—	0.3	—	%
Differential Phasa	DP	V_I =2V_{P-P}, Staircase Signal	—	0.3	—	deg
Output Offset Voltage (1)	V_{OS1}	(Note2)	−10	0	+10	mV
Output Offset Voltage (2)	V_{OS2}	(Note3)	−30	0	+30	mV
Crosstalk	CT	V_I =2V_{P-P}, 4.43MHz, V_O/V_I	—	−75	—	dB
Switch Change Voltage	V_{CH}	All inside SW: ON	2.5	—	—	V
Switch Change Voltage	V_{CL}	All inside SW: OFF	—	—	1.0	V

(Note 1): S1=S2=S3=S4=S5=S6=S7=1

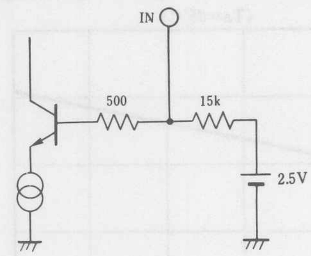
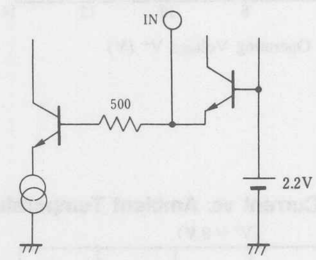
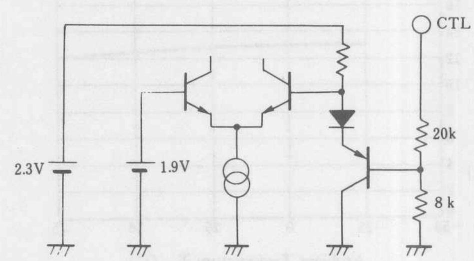
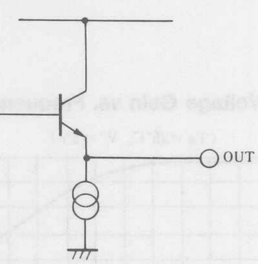
(Note 2): Output DC Voltage Difference is tested on S6=1→2, S1=S2=S3=S4=S5=1, S8=2 and S7=1

(Note 3): Output DC Voltage Difference is tested on S6=1→2, S7=1(or S6=1, S7=1→2,), S1=S2=S3=S4=S5=1 and S8=1

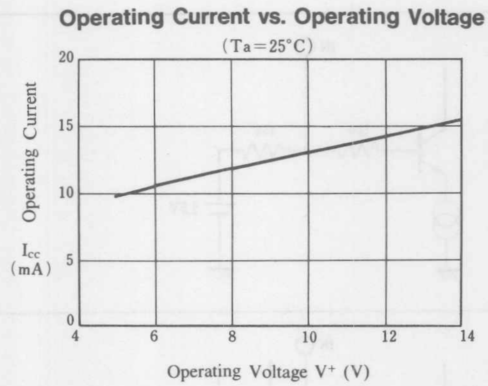
■ TEST CIRCUIT

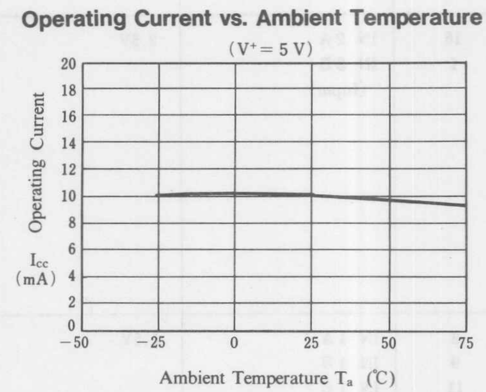


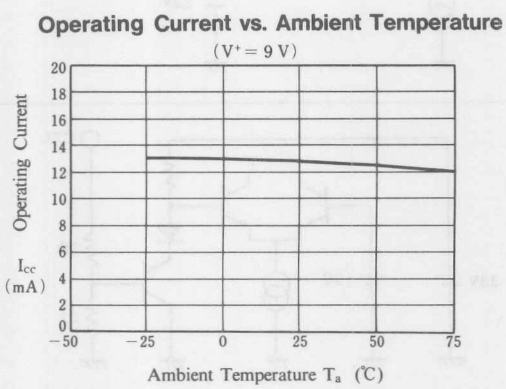
■ PIN FUNCTION

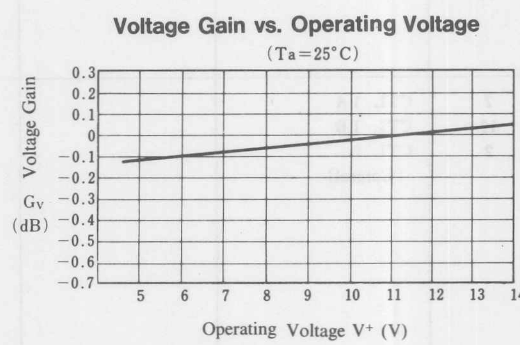
PIN No.	PIN NAME	DC VOLTAGE	INSIDE EQUIVALENT CIRCUIT
16 1	IN 2 A IN 2 B 〔Input〕	2.5V	
8 9 11	IN 1 A IN 1 B IN 1 C 〔Input〕	1.5V	
7 12 2	CTL 1 A CTL 1 B CTL 2 〔Control〕		
5	OUT 1 〔Output〕	1.8V	
3	OUT 2 〔Output〕	0.8V	
13	V+	5 V	
15 4 10	GND 1 GND 2 GND 3		

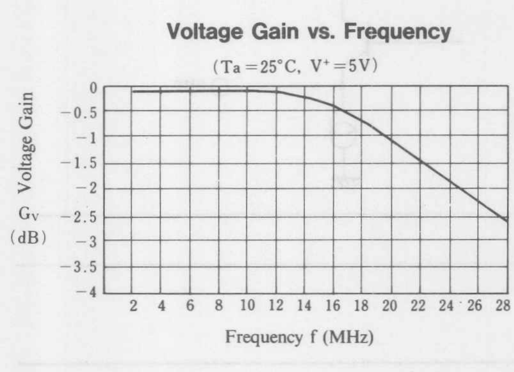
■ **TYPICAL CHARACTERISTICS** (Ta=+25℃)

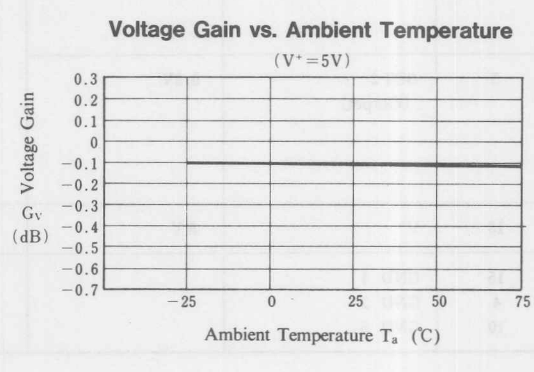




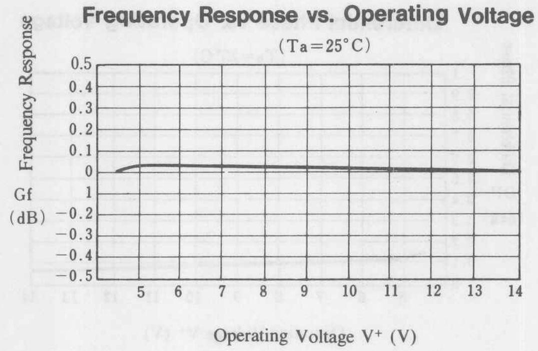


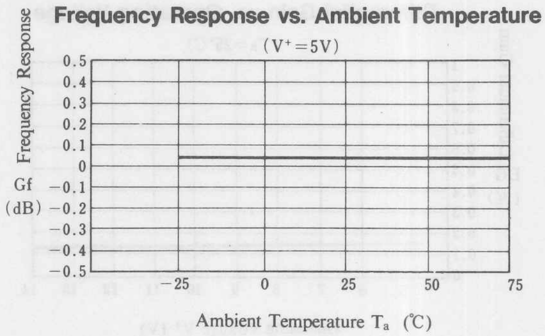


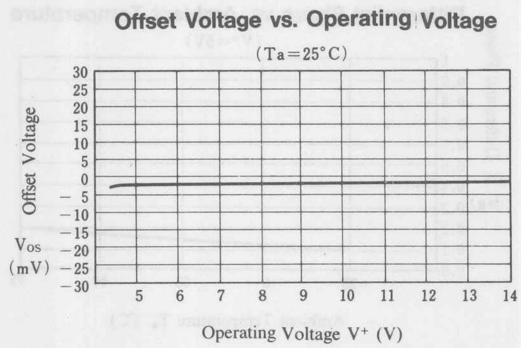


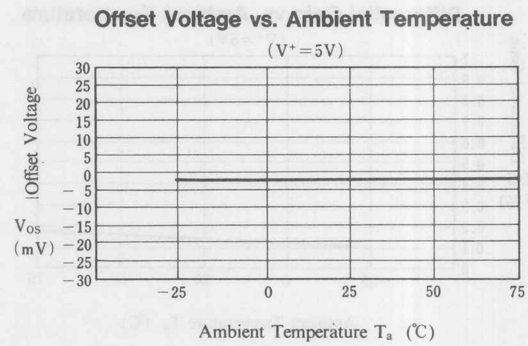


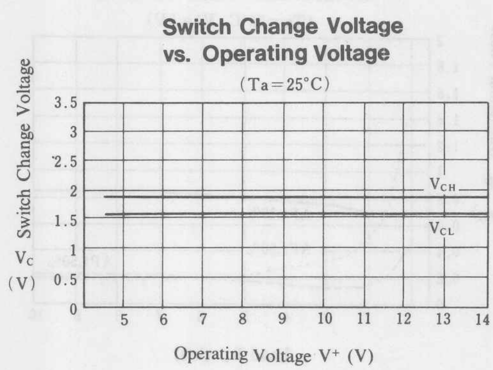
■ **TYPICAL CHARACTERISTICS** (Ta=+25℃)

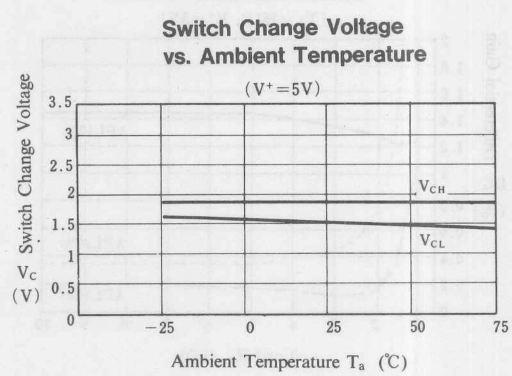




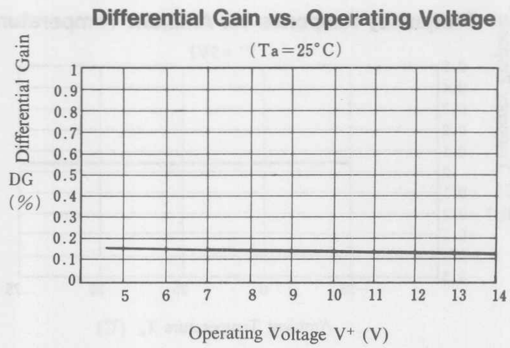


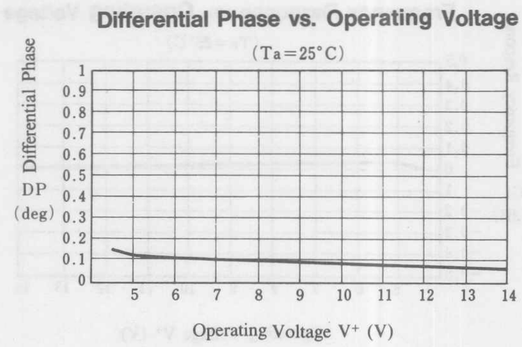


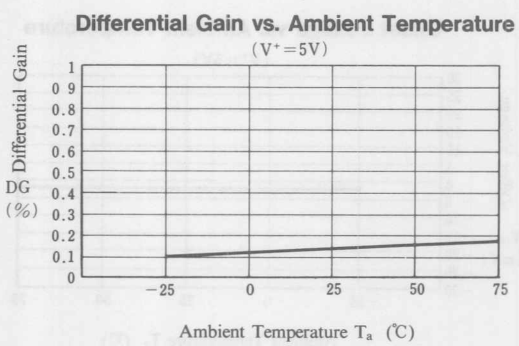


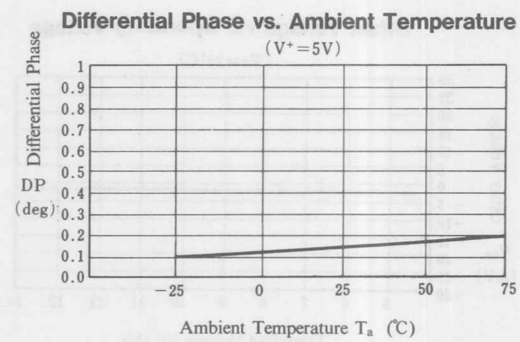


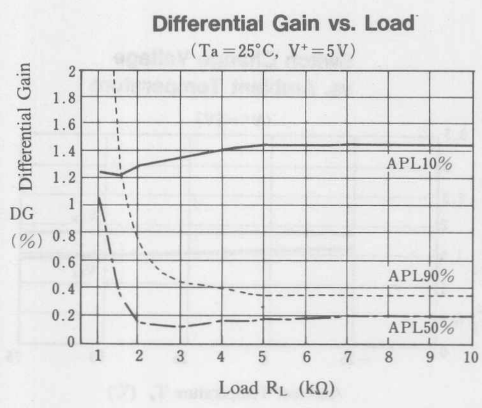
■ **TYPICAL CHARACTERISTICS** (Ta=+25℃)

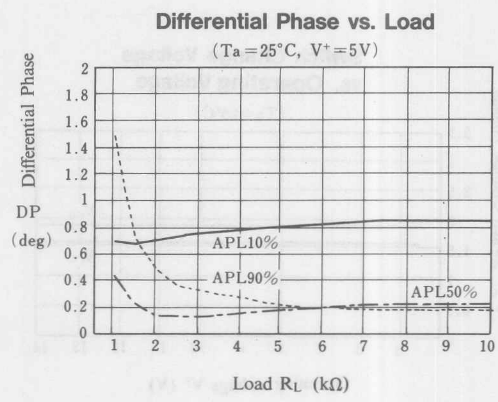








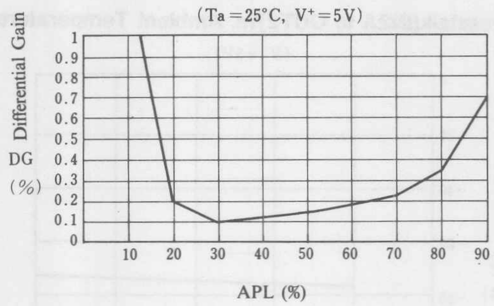




■ TYPICAL CHARACTERISTICS (Ta=+25℃)

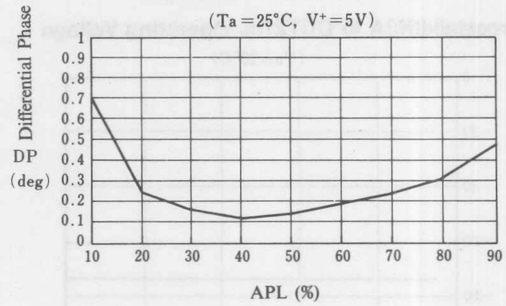
Differential Gain vs. APL

(Ta=25°C, V+=5V)



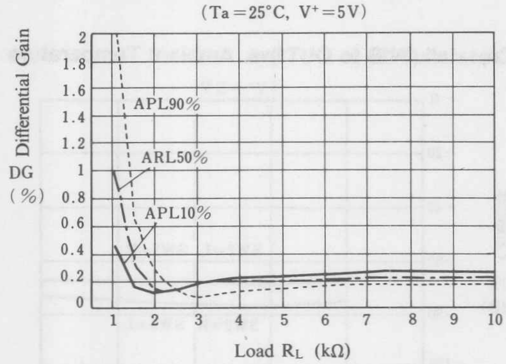
Differential Phase vs. APL

(Ta=25°C, V+=5V)



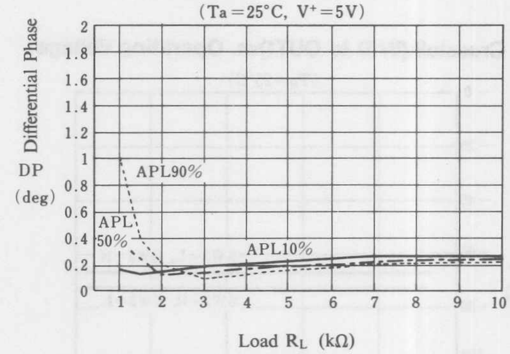
Differential Gain vs. Load

(Ta=25°C, V+=5V)



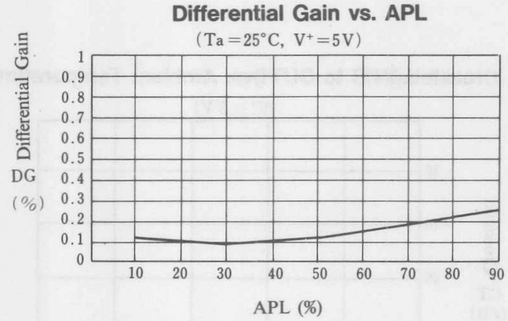
Differential Phase vs. Load

(Ta=25°C, V+=5V)



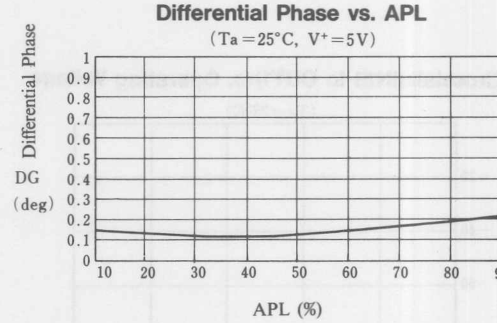
Differential Gain vs. APL

(Ta=25°C, V+=5V)

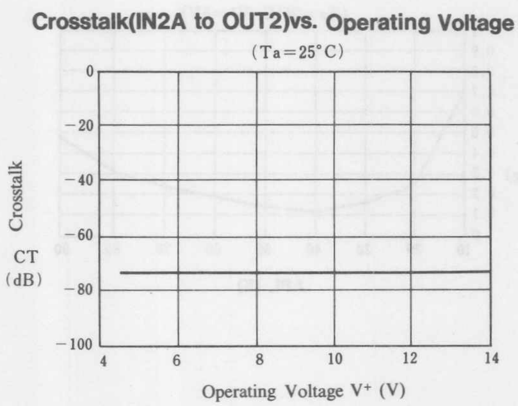


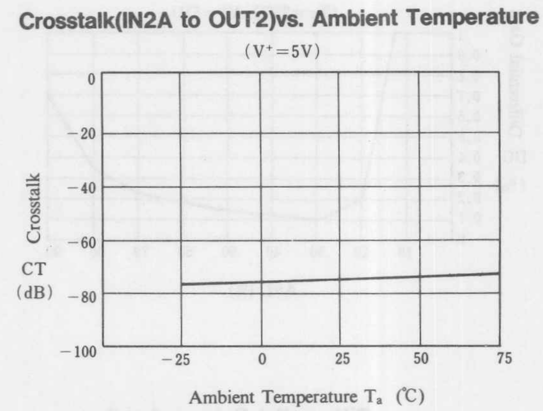
Differential Phase vs. APL

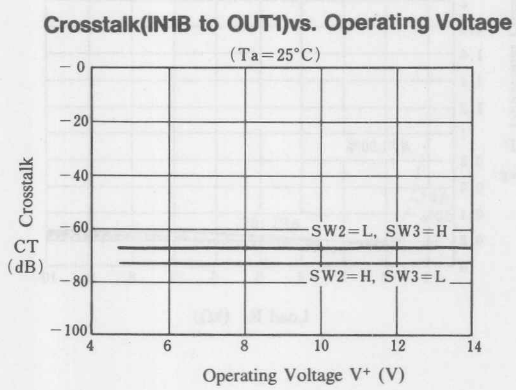
(Ta=25°C, V+=5V)

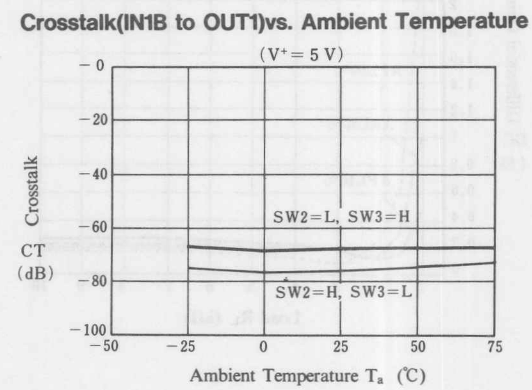


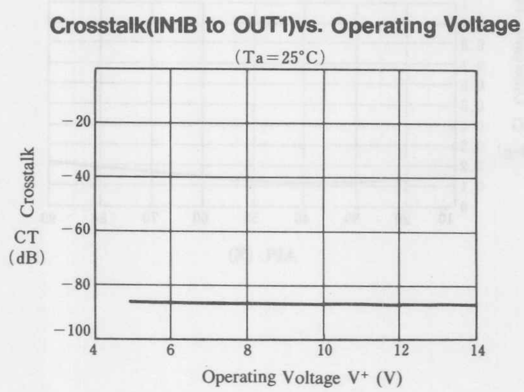
■ **TYPICAL CHARACTERISTICS** (Ta=+25℃)

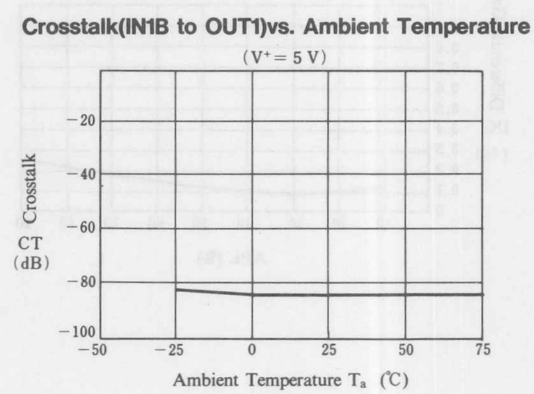






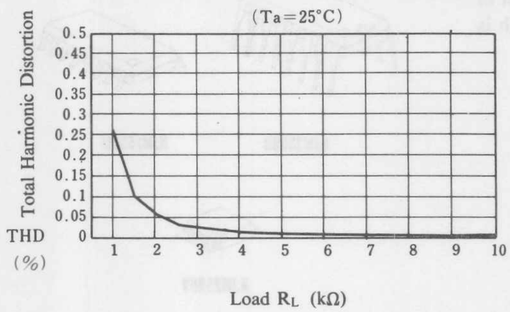






■ **TYPICAL CHARACTERISTICS** (Ta=+25℃)

Total Harmonic Distortion vs. Load

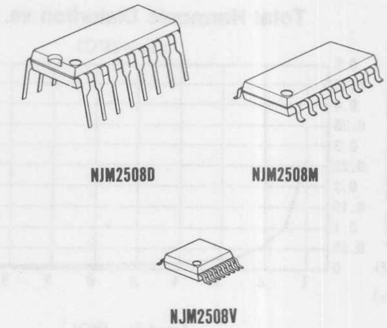


3-INPUT/2-INPUT VIDEO SWITCH

■ GENERAL DESCRIPTION

The NJM2508 is video switch for video and audio signal. It contanins 3 input-1 output and 2 input-1 output video switch. One input terminal has clamp function and so is applied to fixed DC level of video signal. Its operating voltage is 4.75 to 13V and bandwidth is 10MHz. Crosstalk is 75dB (at f=4.43MHz).

■ PACKAGE OUTLINE



■ FEATURES

- Operating Voltage (+4.75V～+13V)
- 3 Input-1 Output and 2 Input-1 Output
- Crosstalk 75dB(at 4.43MHz)
- Wide Frequency Range 10MHz(2V_{P-P} Input)
- Package Outline DIP16, DMP16, SSOP16
- Bipolar Technology

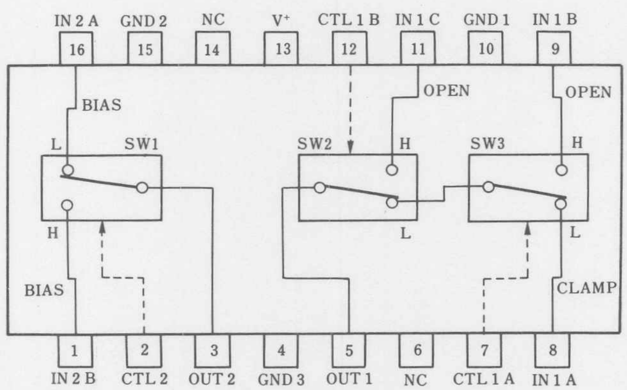
■ RECOMMENDED OPERATING CONDITION

- Operating Voltage V^+ 4.75～13.0V

■ APPLICATION

- VTR, Video Camera, AV-TV, Video Disk Player.

■ BLOCK DIAGRAM



NJM2508D
NJM2508M
NJM2508V

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	14	V
Power Dissipation	P_D	(DIP16) 700	mW
		(DMP16) 350	mW
		(SSOP16) 300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

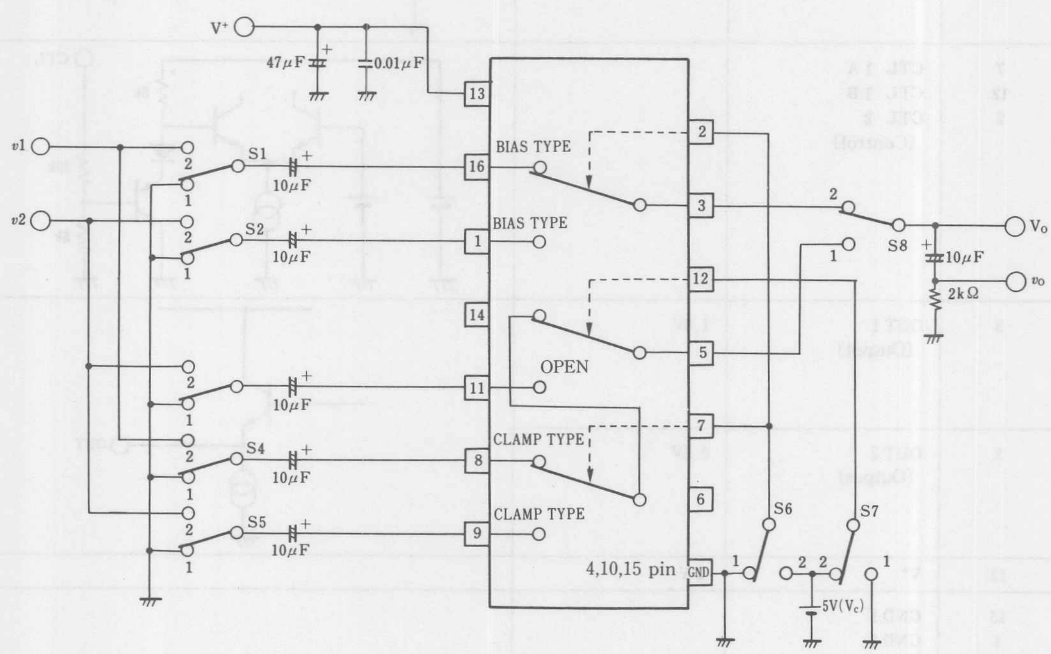
■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

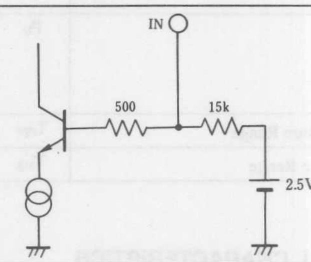
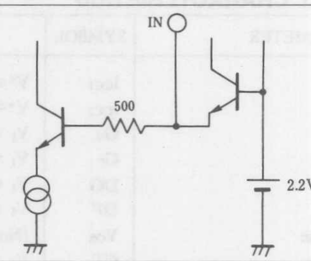
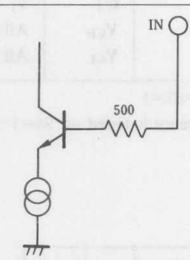
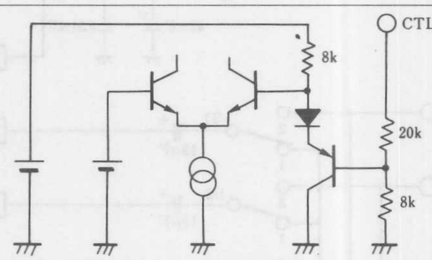
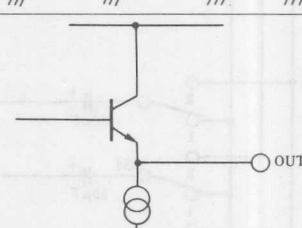
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current 1	I_{CC1}	V^+=5V (Note1)	6.6	9.4	12.3	mA
Operating Current 2	I_{CC2}	V^+=9V (Note1)	8.0	11.5	15.0	mA
Voltage Gain	G_V	V_I =2V_{P-P}/100kHz, V_O/V_I	−0.6	−0.1	+0.4	dB
Frequency Response	G_f	V_I =2V_{P-P}, V_O(10MHz/100MHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_I =2V_{P-P} Staircase Signal	−	0.3	−	%
Differential Phasa	DP	V_I =2V_{P-P} Staircase Signal	−	0.3	−	deg
Output Offset Voltage	V_{OS}	(Note2)	−10	0	+10	mV
Crosstalk	CT	V_I =2V_{P-P}, 4.43MHz, V_O/V_I	−	−75	−	dB
Switch Change Voltage	V_{CH}	All inside SW: ON	2.5	−	−	V
Switch Change Voltage	V_{CL}	All inside SW: OFF	−	−	1.0	V

(Note1) S1=S2=S3=S4=S5=S6=S7=1
(Note2) Output DC Voltage Difference is tested on S6=1→2, S1=S2=S3=S4=S5=1, S8=2 and S7=1

■ TEST CIRCUIT

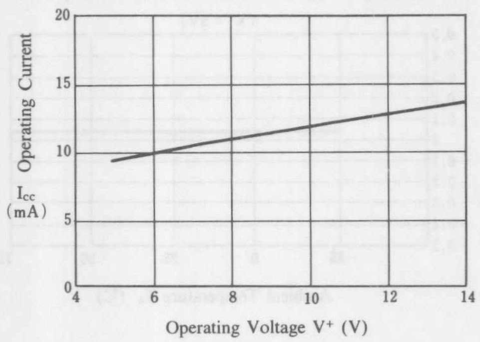


■ PIN FUNCTION

PIN NO.	PIN NAME	DC VOLTAGE	INSIDE EQUIVALENT CIRCUIT
16 1	IN 2 A IN 2 B 〔Input〕	2.5V	
8	IN 1 A 〔Input〕	1.5V	
9 11	IN 1 B IN 1 C 〔Input〕		
7 12 2	CTL 1 A CTL 1 B CTL 2 〔Control〕		
5	OUT 1 〔Output〕	1.8V	
3	OUT 2 〔Output〕	0.8V	
13	V+	5 V	
15 4 10	GND 1 GND 2 GND 3		

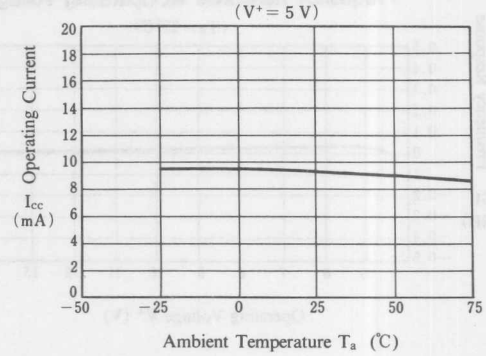
■ TYPICAL CHARACTERISTICS (Ta=+25℃)

Operating Current vs. Operating Voltage



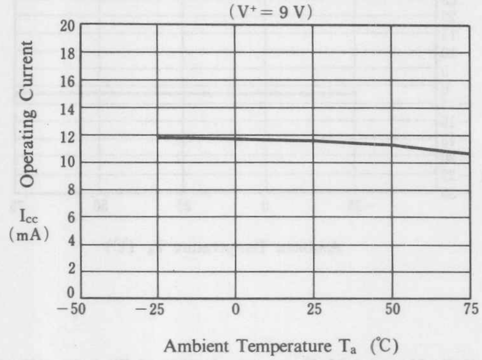
Operating Current vs. Ambient Temperature

(V^+ = 5 V)



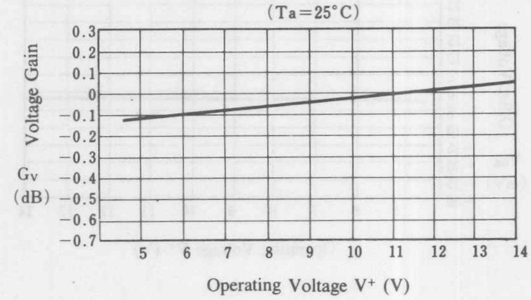
Operating Current vs. Ambient Temperature

(V^+ = 9 V)



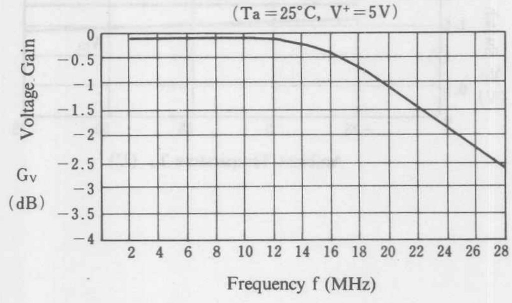
Voltage Gain vs. Operating Voltage

(Ta=25°C)



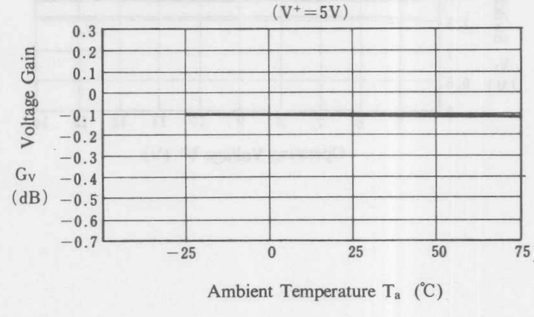
Voltage Gain vs. Frequency

(Ta=25°C, V^+=5V)



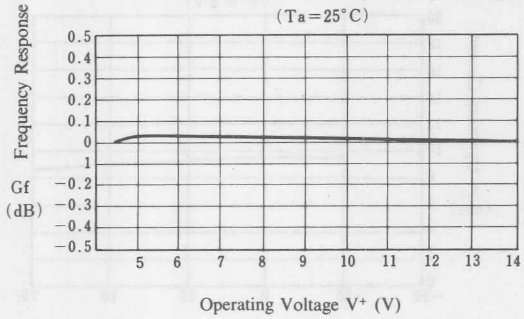
Voltage Gain vs. Ambient Temperature

(V^+=5V)

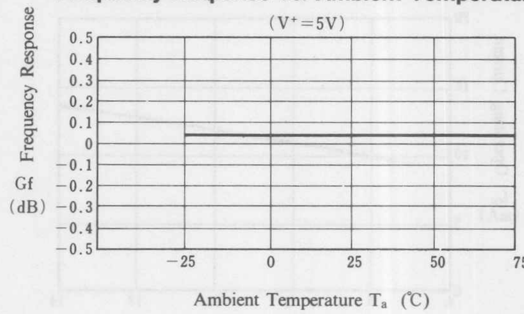


■ **TYPICAL CHARACTERISTICS** (Ta=+25℃)

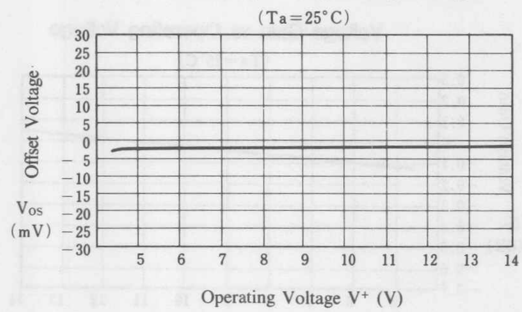
Frequency Response vs. Operating Voltage



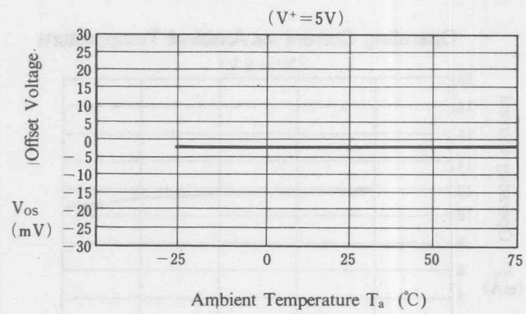
Frequency Response vs. Ambient Temperature



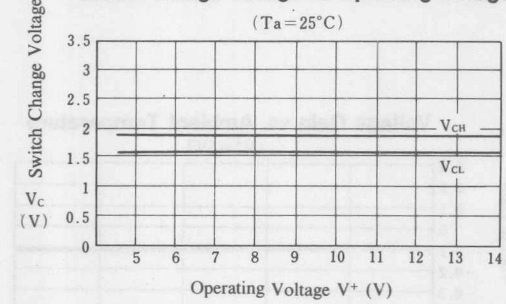
Offset Voltage vs. Operating Voltage



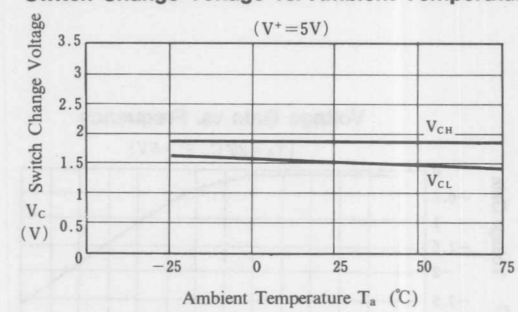
Offset Voltage vs. Ambient Temperature



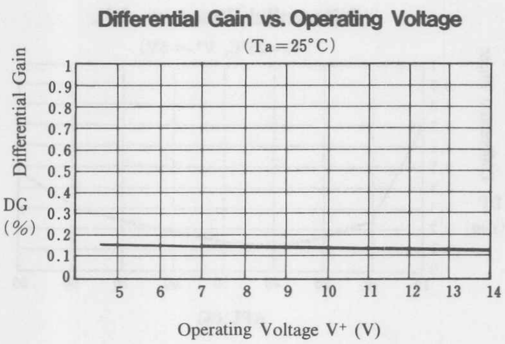
Switch Change Voltage vs. Operating Voltage

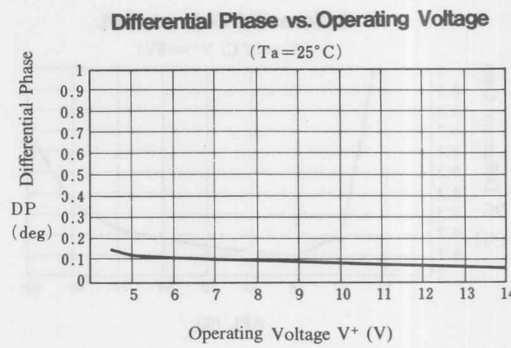


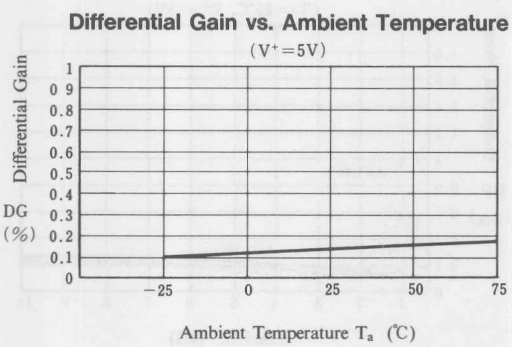
Switch Change Voltage vs. Ambient Temperature

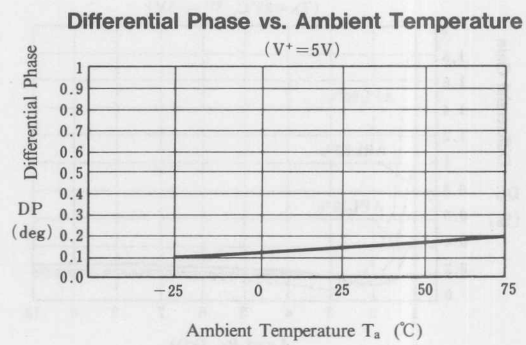


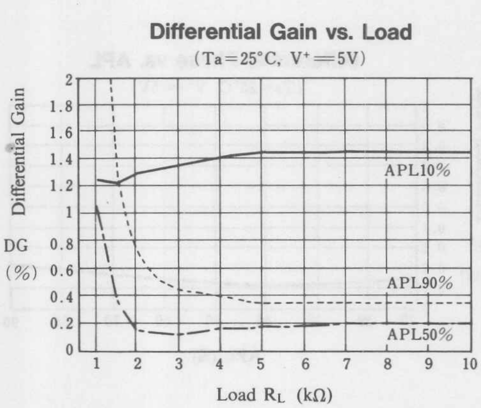
■ TYPICAL CHARACTERISTICS (Ta=+25℃)

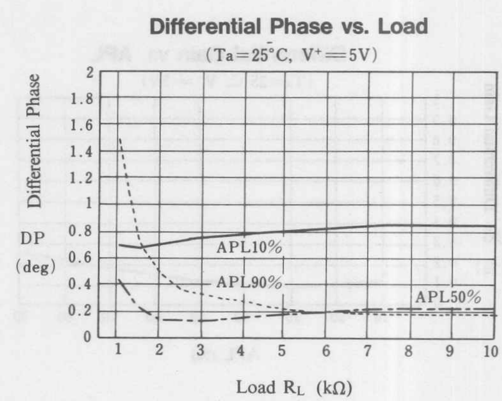








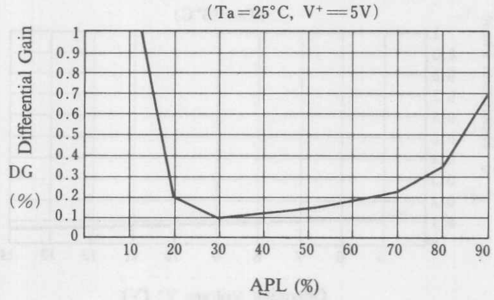




■ **TYPICAL CHARACTERISTICS** (Ta=+25℃)

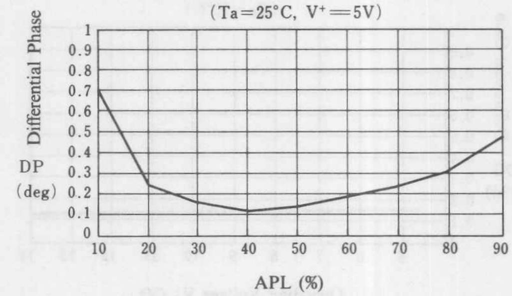
Differential Gain vs. APL

(Ta=25°C, V+=5V)



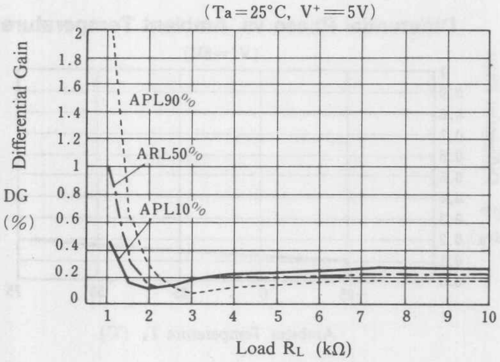
Differential Phase vs. APL

(Ta=25°C, V+=5V)



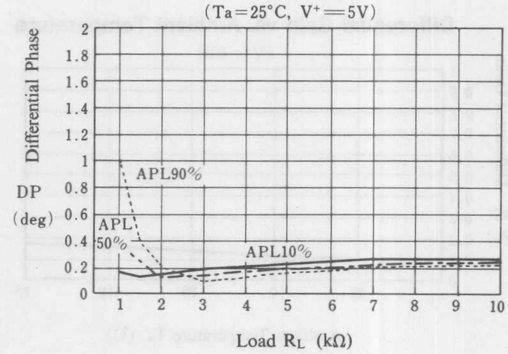
Differential Gain vs. Load

(Ta=25°C, V+=5V)



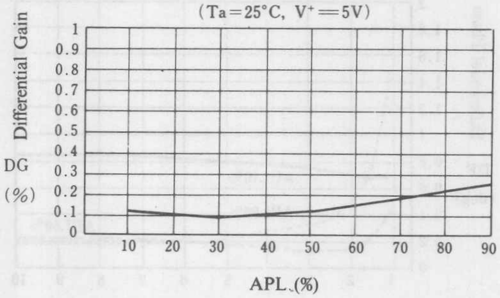
Differential Phase vs. Load

(Ta=25°C, V+=5V)



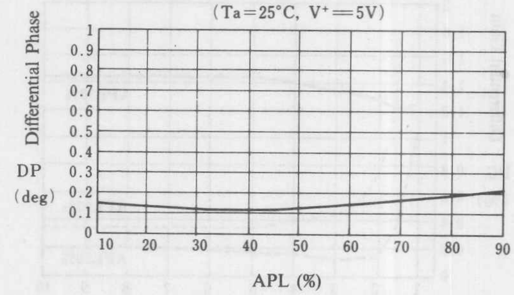
Differential Gain vs. APL

(Ta=25°C, V+=5V)



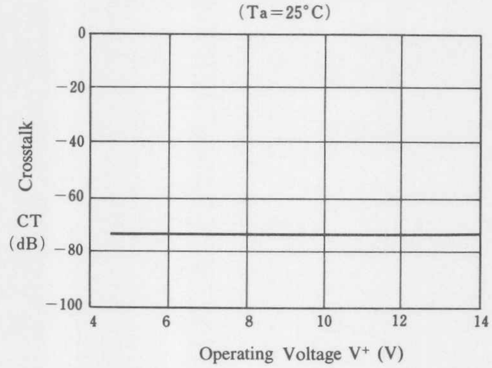
Differential Phase vs. APL

(Ta=25°C, V+=5V)

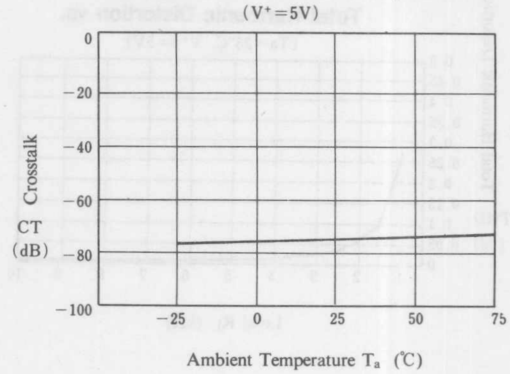


■ TYPICAL CHARACTERISTICS (Ta=+25℃)

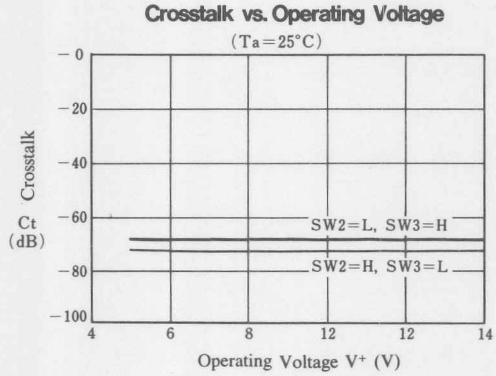
Crosstalk vs. Operating Voltage



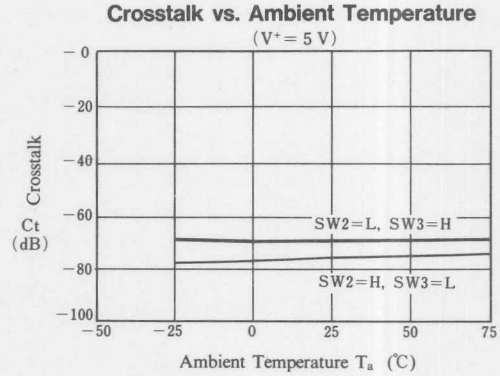
Crosstalk vs. Ambient Temperature



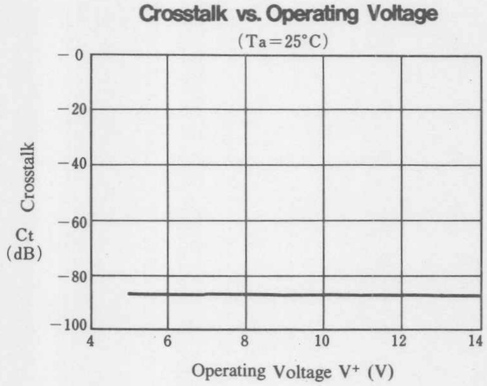
Crosstalk vs. Operating Voltage



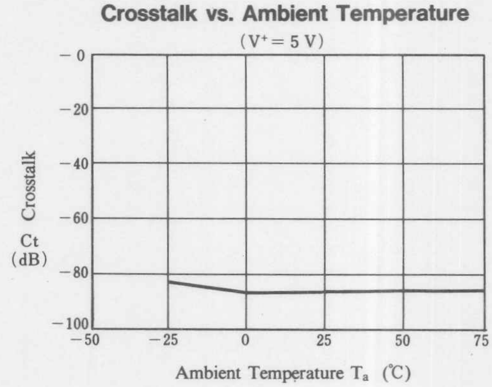
Crosstalk vs. Ambient Temperature



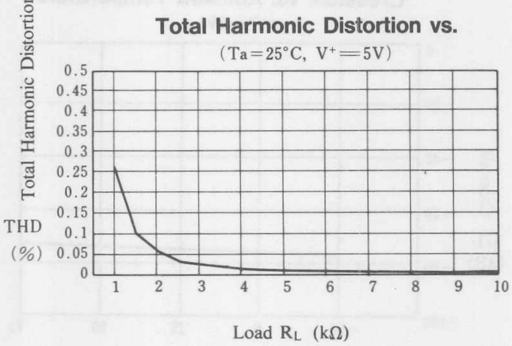
Crosstalk vs. Operating Voltage



Crosstalk vs. Ambient Temperature



■ **TYPICAL CHARACTERISTICS** (Ta=+25℃)



VIDEO SUPER INPOSER WITH Y-C MIXER

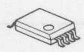
■ GENERAL DESCRIPTION

The NJM2509 is video super imposer, including Y/C mix circuit.

Y-signal input terminal have sink-chip clamp function and it is applied to fixed DC level of video signal.

Impose voltage is fixed internally to white level and black level, and includes 6dB amplifier.

■ PACKAGE OUTLINE



NJM2509V

■ FEATURES

- Operating Voltage (4.5~5.1V)
- Internal Y/C Mix Circuit
- Internal Clamp Circuit (Y Signal), Bias Circuit (C Signal)
- Impose voltage fixed internally to white level and black level.
- Internal 6dB AMP. (Input:0.5V_{P-P}, Output:1.0V_{PP})
- Package Outline SSOP8
- Bipolar Technology

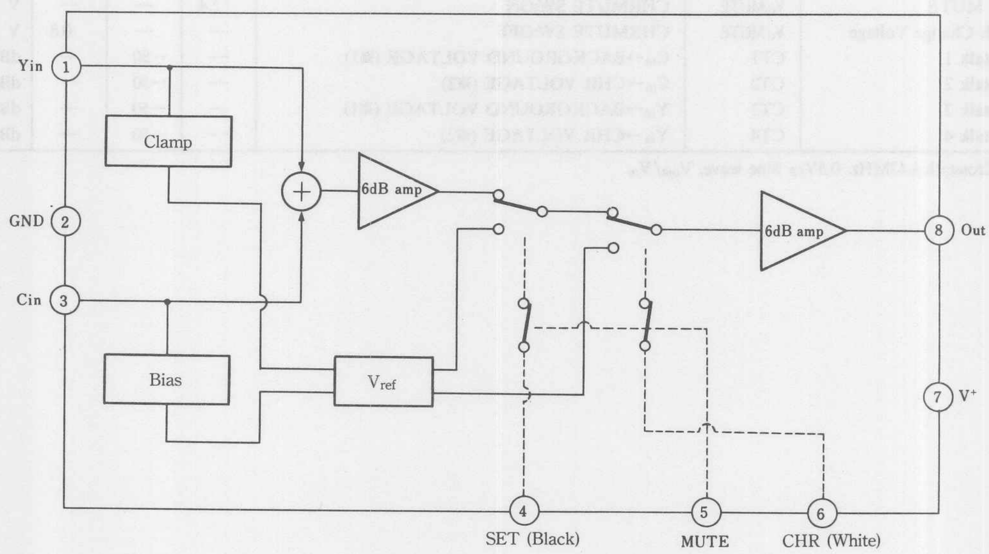
■ RECOMMENDED OPERATING CONDITION

- Operating Voltage V^+ 4.5~5.1V

■ APPLICATION

- Video Camera

■ BLOCK DIAGRAM



NJM2509V

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	7.0	V
Power Dissipation	P_D	250	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

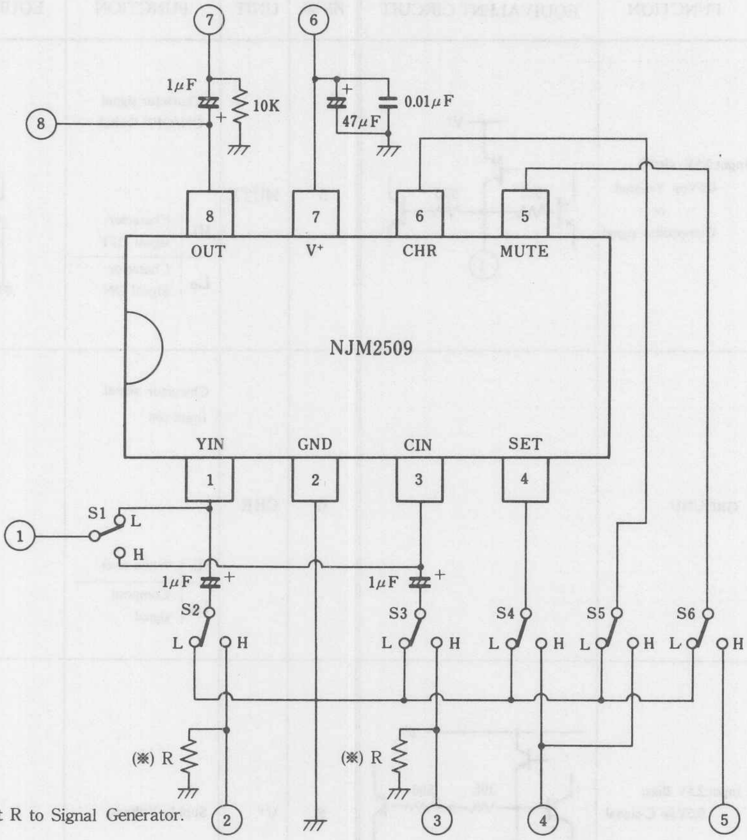
■ ELECTRICAL CHARACTERISTICS

(V^+=4.8V, Ta=25℃, R_L=10kΩ)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}		5.3	7.0	8.7	mA
Clamp Voltage	V_{cmp}		2.4	2.5	2.6	V
Bias Voltage	V_{bias}		2.4	2.5	2.6	V
Voltage Gain	G_V	V_{out}/V_{in} 100kHz, 0.5V_{P-P} Sine Wave	6.0	6.3	6.8	dB
Frequency Characteristic	G_l	0.5V_{P-P} Sine Wave v_0 (10MHz)/v_0 (100kHz)	−0.7	−0.2	+0.3	dB
Background Voltage	V_{set}	From Pedestal Level	5.0	15.0	20.0	IRE
CHR. VOLTAGE	V_{chr}	From Pedestal Level	65.0	75.0	85.0	IRE
Input Resistance	R_{in}	Input Cin	—	30	—	kΩ
Differential Gain	DG	0.5V_{P-P}, 10 STEP Stair wave	—	—	3.0	deg
Differential Phasa	DP	0.5V_{P-P}, 10 STEP Stair wave	—	—	3.0	%
BACKGROUND	V_{ch}	BACKGROUND SW:ON	2.4	—	—	V
Switch Change Voltage	V_{cl}	BACKGROUND SW:OFF	—	—	0.8	V
CHR MUTE	V_{ch}MUTE	CHRMUTE SW:ON	2.4	—	—	V
Switch Change Voltage	V_{cl} MUTE	CHRMUTE SW:OFF	—	—	0.8	V
Crosstalk 1	CT1	C_{in}→BACKGROUND VOLTAGE (※1)	—	−50	—	dB
Crosstalk 2	CT2	C_{in}→CHR VOLTAGE (※2)	—	−50	—	dB
Crosstalk 3	CT3	Y_{in}→BACKGROUND VOLTAGE (※1)	—	−50	—	dB
Crosstalk 4	CT4	Y_{in}→CHR VOLTAGE (※2)	—	−50	—	dB

※1. Crosstalk:4.43MHz. 0.5V_{PP} Sine wave, V_{out}/V_{in}

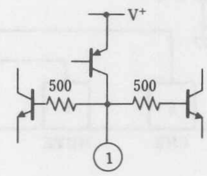
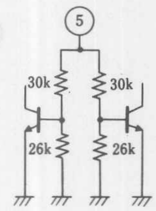
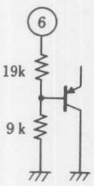
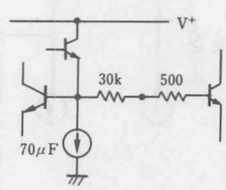
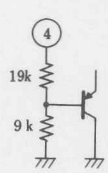
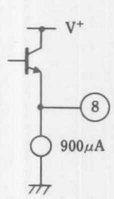
■ TEST CIRCUIT



(※):Adjust R to Signal Generator.

■ TERMINAL EXPLANATION

(V⁺=4.8V, Ta=25℃)

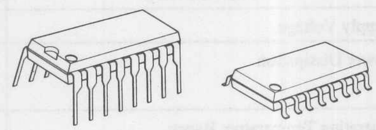
PIN NO.	UNIT	FUNCTION	EQUIVALENT CIRCUIT	PIN NO.	UNIT	FUNCTION	EQUIVALENT CIRCUIT
1	YIN	Input:2.5V clamp 0.5VPP Y-signal or Compozitto signal		5	MUTE	Ckaractor signal ON/OFF Switch Hi: Charactor signal OFF Lo: Charactor Signal ON	
2	GND	GROUND		6	CHR	Charactor signal Input pin Hi: White level Lo: Composit signal	
3	CIN	Input:2.5V Bias, 0.5VPP C-signal		7	V⁺	Supply Voltage	
4	SET	Charactor signal Input Pin Hi: Black level Lo: Composit signal		8	OUT	Output-1VPP Composit signal, Impose Voltage	

3-INPUT/2-INPUT VIDEO SWITCH

■ GENERAL DESCRIPTION

The NJM2513 is a switching IC for switching over from one audio or video input signal to another. Internalizing 3 input-1 output, and 2 input-1 output and then each set can be operated independently. Side of 2 input-1 output are "Clamp type", and they can be operated while setting DC level fixed in position of the video signal. It is a higher efficiency video switch, featuring the operating voltage 4.75 to 13V, the frequency feature 10MHz, and then the Crosstalk 75dB (at 4.43MHz).

■ PACKAGE OUTLINE



NJM2513D NJM2513M

■ FEATURES

- Operating Voltage (+4.75V～+13V)
- 3 Input-1 Output/2 Input-1 output
- Crosstalk 75dB(at 4.43MHz)
- Wide Bandwidth Frequency 10MHz(2V_{P-P} Input)
- Package Outline DIP16, DMP16
- Bipolar Technology

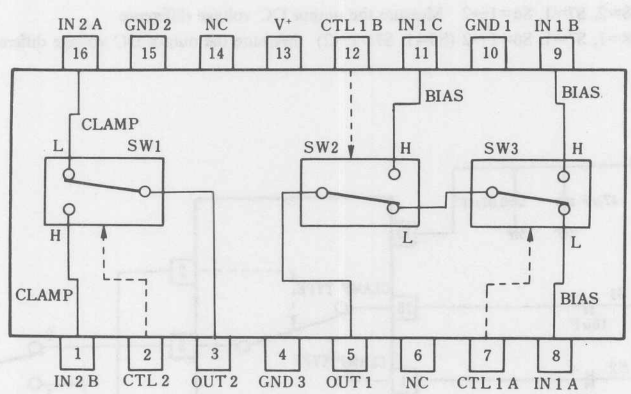
■ RECOMMENDED OPERATING CONDITION

- Operating Voltage V^+ 4.75～13.0V

■ APPLICATIONS

- VCR, Video Camera, AV-TV, Video Disk Player.

■ BLC DIAGRAM



NJM2513D
NJM2513M

■ MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	14	V
Power Dissipation	P_D	(DIP16) 700	mW
		(DMP16) 350	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

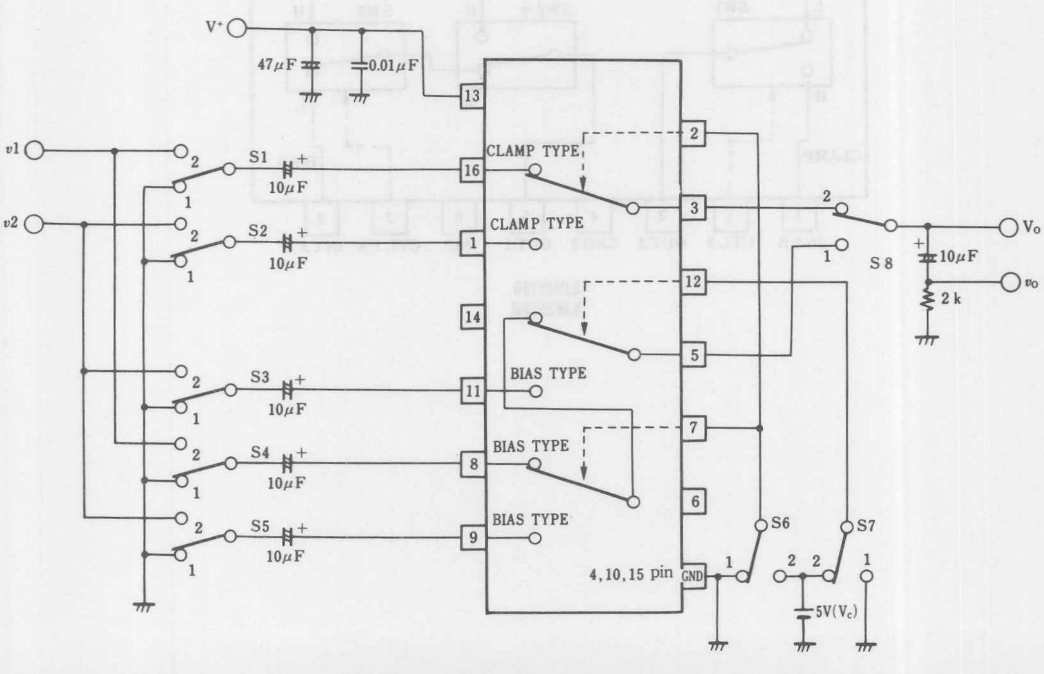
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	$I_{CC}1$	V^+=5V (Note1)	6.7	9.7	12.7	mA
Operating Current (2)	$I_{CC}2$	V^+=9V (Note1)	8.6	12.3	16.0	mA
Voltage Gain	G_V	V_I =100kHz, $2V_{P\text{-}P}$, V_O/V_I	−0.6	−0.1	+0.4	dB
Frequency Gain	G_F	V_I =$2V_{P\text{-}P}$, V_O(10MHz)/V_O(100kHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_I =$2V_{P\text{-}P}$, Standerd Staircase Signal	—	0.3	—	%
Differential Phasa	DP	V_I =$2V_{P\text{-}P}$, Standerd Staircase Signal	—	0.3	—	deg
OutPut offset Voltage (1)	$V_{OS}1$	(Note2)	−15	0	+15	mV
OutPut offset Voltage (2)	$V_{OS}2$	(Note3)	−25	0	+25	mV
Crosstalk	CT	V_I =$2V_{P\text{-}P}$, 4.43MHz, V_O/V_I	—	−75	—	dB
Switch Change Over Voltage	V_{CH}	All inside Switches ON	2.5	—	—	V
Switch Change Over Voltage	V_{CL}	All inside Switches OFF	—	—	1.0	V

(Note1) S1=S2=S3=S4=S5=S6=S7=1

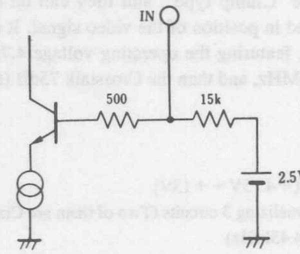
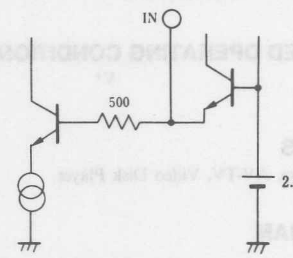
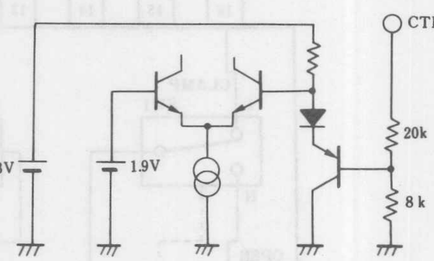
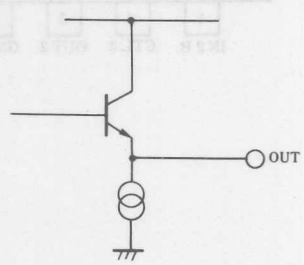
(Note2) S1=S2=S3=S4=S5=1, S8=2, S7=1, S6=1→2 Measure the output DC voltage difference

(Note3) S1=S2=S3=S4=S5=1, S8=1, S7=1, S6=1→2 (S6=1, S7=1→2) Measure the output DC voltage difference

■ TEST CIRCUIT



■ TERMINAL EXPLANATION

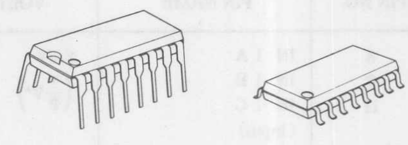
PIN NO.	PIN NAME	VOLTAGE	INSIDE EQUIVALENT CIRCUIT
8 9 11	IN 1 A IN 1 B IN 1 C 〔Input〕	2.5V $\left(\frac{1}{2}V^+\right)$	
16 1	IN 2 A IN 2 B 〔Input〕	1.5V $\left(\frac{3}{10}V^+\right)$	
7 12 2	CTL 1 A CTL 1 B CTL 2 〔Switching〕		
5	OUT 1 〔Output〕	1.8V $\left(\frac{1}{2}V^+-0.7\right)$	
3	OUT 2 〔Output〕	0.8V $\left(\frac{3}{10}V^+-0.7\right)$	
13	V^+	5 V	
15 4 10	GND 1 GND 2 GND 3		

3-INPUT/2-INPUT VIDEO SWITCH

■ GENERAL DESCRIPTION

The NJM2523 is a switching IC for switching over from one audio or video input signal to another. Internalizing 3 input-1 output, and 2 input-1 output and then each set can be operated independently. One of 2 input-1 output are Clamp type", and they can be operated while setting DC level fixed in position of the video signal. It is a higher efficiency video switch, featuring the operating voltage 4.75V to 13V, the frequency feature 10MHz, and then the Crosstalk 75dB (at 4.43MHz).

■ PACKAGE OUTLINE



NJM2523D NJM2523M

■ FEATURES

- Operating Voltage (+4.75V ~ +13V)
- Input-1 Output Internalizing 3 circuits (Two of them are Clamp type).
- Crosstalk 75dB(at 4.43MHz)
- Wide Bandwidth Frequency 10MHz(2V_{P-P} Input)
- Package Outline DIP16, DMP16.

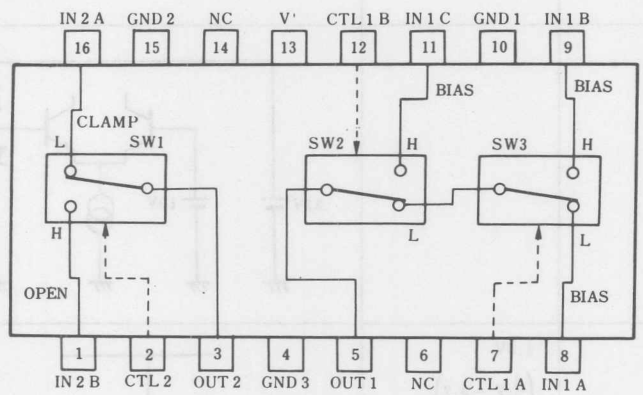
■ RECOMMENDED OPERATING CONDITION

- Operating Voltage V^+ 4.75~13.0V

■ APPLICATIONS

- VCR, Video Camera, AV-TV, Video Disk Player.

■ BLOCK DIAGRAM



NJM2523D
NJM2523M

■ MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	14	V
Power Dissipation	P_D	(DIP16) 700	mW
		(DMP16) 350	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

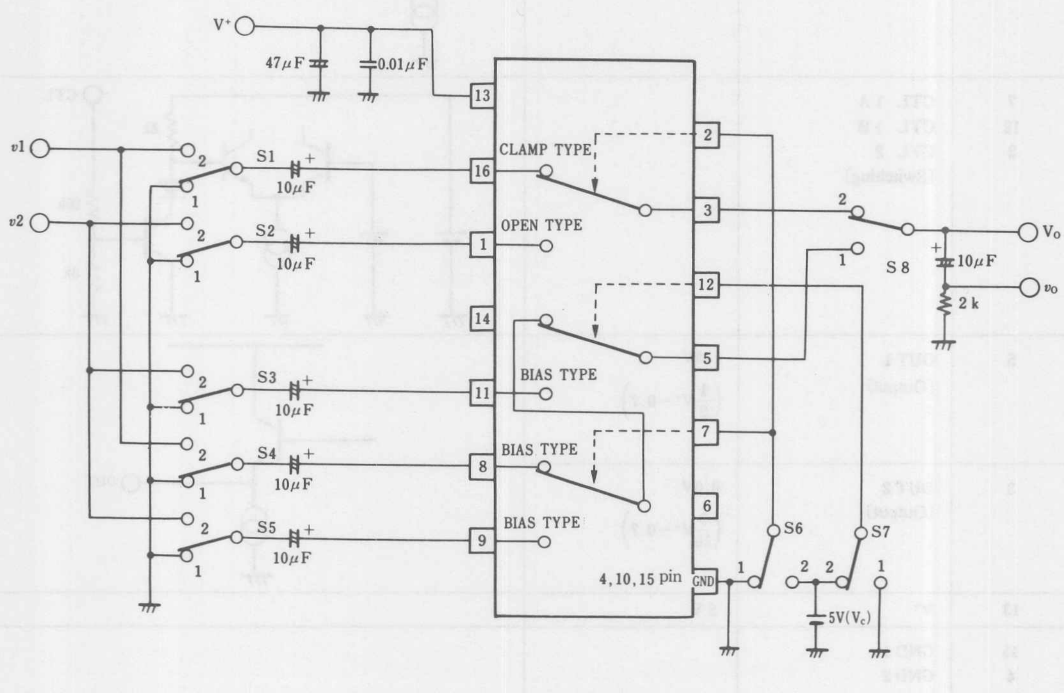
(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	$I_{CC}1$	V^+=5V (Note1)	6.7	9.7	12.7	mA
Operating Current (2)	$I_{CC}2$	V^+=9V (Note1)	8.6	12.3	16.0	mA
Voltage Gain	G_V	V_I =100kHz, $2V_{P-P}$, V_O/V_I	−0.6	−0.1	+0.4	dB
Frequency Gain	G_F 1	V_I =$2V_{P-P}$, V_O(10MHz)/V_O(100kHz)	−1.0	0	+1.0	dB
Differential Gain	DG	V_I =$2V_{P-P}$, Standerd Staircase Signal	—	0.3	—	%
Differential Phasa	DP	V_I =$2V_{P-P}$, Standerd Staircase Signal	—	0.3	—	deg
OutPut offset Voltage	$V_{OS}1$	(Note2)	−25	0	+25	mV
Crosstalk	CT	V_I =$2V_{P-P}$, 4.43MHz, V_O/V_I	—	−75	—	dB
Switch Change Over Voltage	V_{CH}	All inside Switches ON	2.5	—	—	V
Switch Change Over Voltage	V_{CL}	All inside Switches OFF	—	—	1.0	V

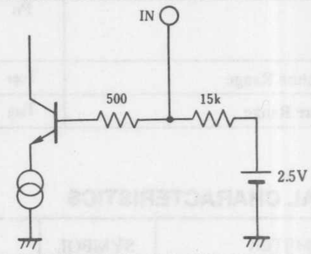
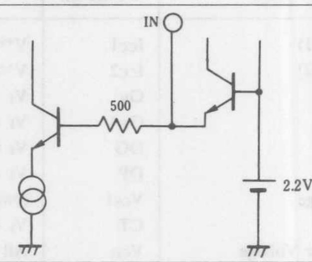
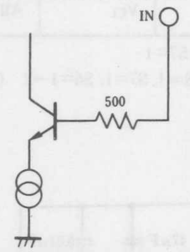
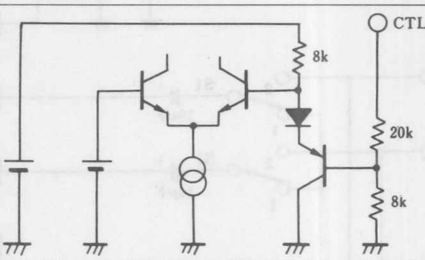
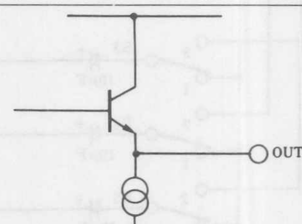
(Note1) S1=S2=S3=S4=S5=S6=S7=1

(Note2) S1=S2=S3=S4=S5=1, S8=1, S7=1, S6=1→2 (S6=1, S7=1→2) Measure the output DC voltage difference

■ TEST CIRCUIT



■ TERMINAL EXPLANATION

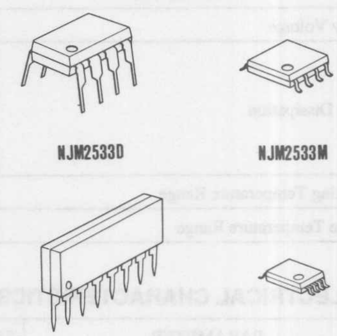
PIN NO.	PIN NAME	VOL	INSIDE EQUIVALENT CIRCUIT
8 9 11	IN 1 A IN 1 B IN 1 C 〔Input〕	2.5V $\left(\frac{1}{2}V^{+}\right)$	
16	IN 2 A 〔Input〕	1.5V $\left(\frac{3}{10}V^{+}\right)$	
1	IN 2 B 〔Input〕		
7 12 2	CTL 1 A CTL 1 B CTL 2 〔Switching〕		
5	OUT 1 〔Output〕	1.8V $\left(\frac{1}{2}V^{+}-0.7\right)$	
3	OUT 2 〔Output〕	0.8V $\left(\frac{3}{10}V^{+}-0.7\right)$	
13	V^{+}	5 V	
15 4 10	GND 1 GND 2 GND 3		

2-INPUT 1-OUTPUT VIDEO SWITCH

■ GENERAL DESCRIPTION

The NJM2533 is a video switch for VCR, TV, and others.
It contains two bias-type inputs and one buffer-type output.

■ PACKAGE OUTLINE



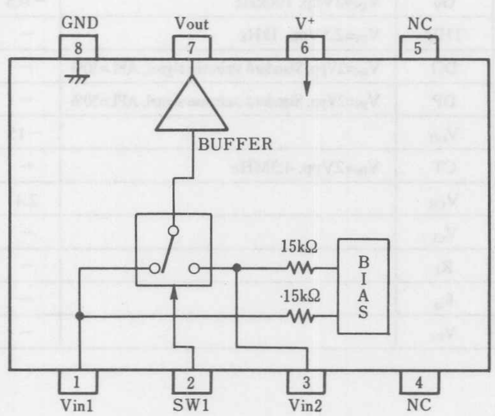
NJM2533D NJM2533M

NJM2533L NJM2533V

■ FEATURES

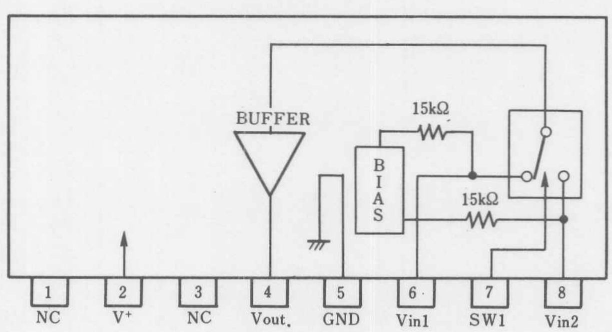
● Operating Voltage	(+4.75V ~ +13V)
● Low Supply Current	(MAX : 3.7mA)
● Crosstalk	(−70dB)
● 2-Input, 1-Output	
● Bipolar Technology	
● Package Outline	DIP8, DMP8, SIP8, SSOP8

■ PIN CONFIGURATION



PIN FUNCTION
1 : Vin1
2 : SW1
3 : Vin2
4 : NC
5 : NC
6 : V+
7 : V_{OUT}
8 : GND

NJM2533D
NJM2533M
NJM2533V



PIN FUNCTION
1 : NC
2 : V+
3 : NC
4 : V_{OUT}
5 : GND
6 : Vin1
7 : SW1
8 : Vin2

NJM2533L

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

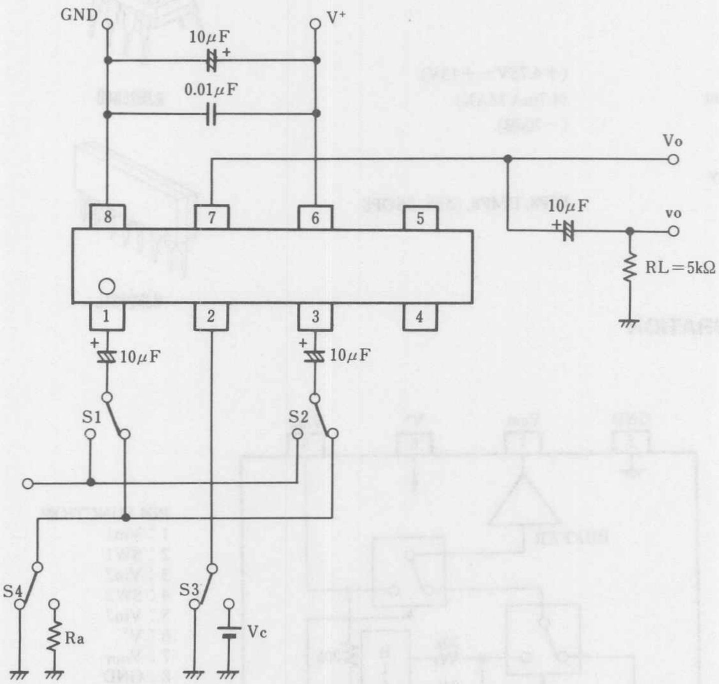
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+15	V
Power Dissipation	P_D	(DIP-8) 500 (DMP-8) 300 (SIP-8) 800 (SSOP-8) 250	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		+4.5	−	+13.0	V
Operating Current	I_{CC}		−	2.7	3.7	mA
Frequency Characteristics	Gf	V_{IN}=2Vpp, Vo=10MHz/100kHz	−1.0	0	+1.0	dB
Voltage Gain	G_V	V_{IN}=2Vpp, 100kHz	−0.5	0	+0.5	dB
Total Harmonic Distortion	THD	V_{IN}=2.5Vpp, 1kHz	−	0.05	0.1	%
Differential Gain	DG	V_{IN}=2Vpp, Standard staircase signal, APL=50%	−	0	3.0	%
Differential Phase	DP	V_{IN}=2Vpp, Standard staircase signal, APL=50%	−	0	3.0	deg
Output Offset Voltage	V_{off}		−15	0	+15	mV
Crosstalk	CT	V_{IN}=2Vpp, 4.3MHz	−	−70	−60	dB
Switching Voltage	V_{CH}		2.4	−	−	V
	V_{CL}		−	−	0.8	V
Input Impedance	R_I		−	30	−	kΩ
Output Impedance	R_o		−	25	−	Ω
Input Bias Voltage	V_{IN}		−	2.5	−	V

■ TEST CIRCUIT

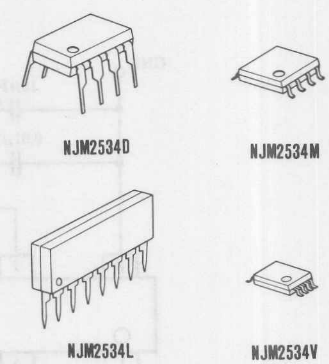


3-INPUT 1-OUTPUT VIDEO SWITCH

■ GENERAL DESCRIPTION

The NJM2534 is a video switch for VCR, TV and others.
It contains three bias-type inputs and one buffer-type output.

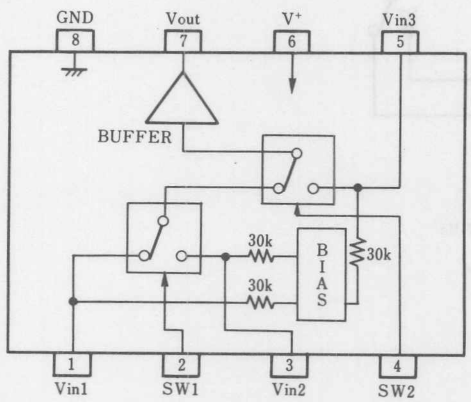
■ PACKAGE OUTLINE



■ FEATURES

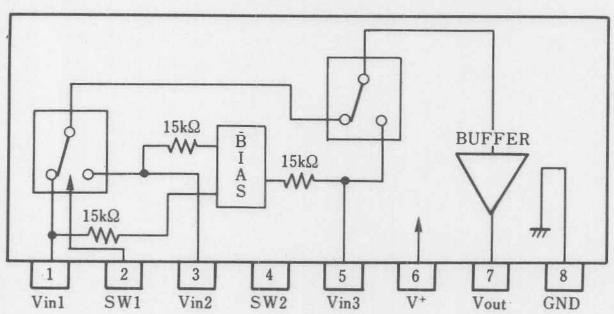
- Operating Voltage (+4.75V ~ +13V)
- Low Supply Current (4.7mA MAX)
- Crosstalk (−70dB)
- 3-Input, 1-Output
- Bipolar Technology
- Package Outline DIP8, DMP8, SIP8, SSOP8

■ PIN CONFIGURATION



PIN FUNCTION
1 : Vin1
2 : SW1
3 : Vin2
4 : SW2
5 : Vin3
6 : V+
7 : V_{OUT}
8 : GND

NJM2534D
NJM2534M
NJM2534V



PIN FUNCTION
1 : Vin1
2 : SW1
3 : Vin2
4 : SW2
5 : Vin3
6 : V+
7 : V_{OUT}
8 : GND

NJM2534L

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

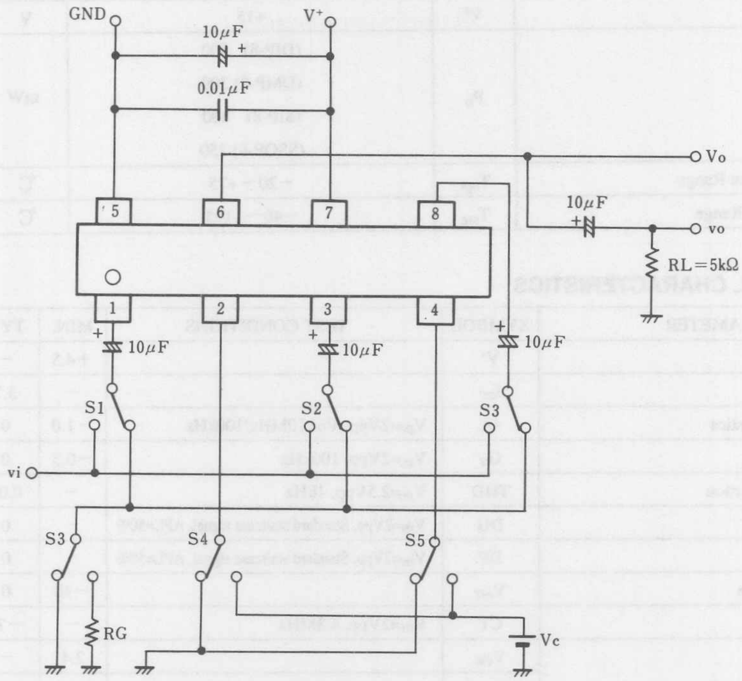
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+15	V
Power Dissipation	P_D	(DIP-8) 500 (DMP-8) 300 (SIP-8) 800 (SSOP-8) 250	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		+4.5	−	+13.0	V
Operating Current	I_{CC}		−	3.7	4.7	mA
Frequency Characteristics	Gf	V_{IN}=2Vpp, Vo=10MHz/100kHz	−1.0	0	+1.0	dB
Voltage Gain	G_V	V_{IN}=2Vpp, 100kHz	−0.5	0	+0.5	dB
Total Harmonic Distortion	THD	V_{IN}=2.5Vpp, 1kHz	−	0.05	0.1	%
Differential Gain	DG	V_{IN}=2Vpp, Standard staircase signal, APL=50%	−	0	3.0	%
Differential Phase	DP	V_{IN}=2Vpp, Standard staircase signal, APL=50%	−	0	3.0	deg
Output Offset Voltage	V_{off}		−30	0	+30	mV
Crosstalk	CT	V_{IN}=2Vpp, 4.3MHz	−	−70	−60	dB
Switching Voltage	V_{CH}		2.4	−	−	V
	V_{CL}		−	−	0.8	V
Input Impedance	R_I		−	30	−	kΩ
Output Impedance	R_o		−	25	−	Ω
Input Bias Voltage	V_{IN}		−	2.5	−	V

■ TEST CIRCUIT



3-INPUT 1-OUTPUT VIDEO SWITCH

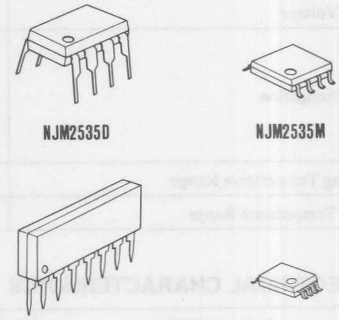
■ GENERAL DESCRIPTION

The NJM2535 is a video switch for VCR, TV and others.
It contains three cramp-type inputs and one buffer-type output.

■ FEATURES

- Operating Voltage (+4.75V～+13V)
- Low Supply Current (4.6mA MAX)
- Crosstalk (−70dB)
- 3-Input, 1-Output
- Bipolar Technology
- Package Outline DIP8, DMP8, SIP8, SSOP8

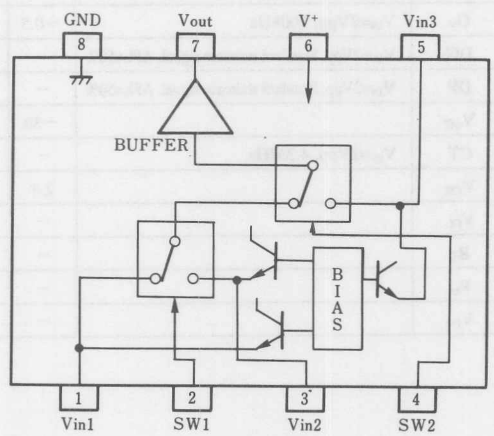
■ PACKAGE OUTLINE



NJM2535D NJM2535M

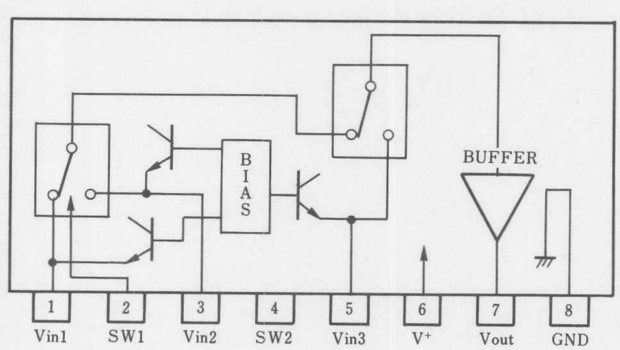
NJM2535L NJM2535V

■ PIN CONFIGURATION



PIN FUNCTION
1 : Vin1
2 : SW1
3 : Vin2
4 : SW2
5 : Vin3
6 : V+
7 : V_{OUT}
8 : GND

NJM2535D
NJM2535M
NJM2535V



PIN FUNCTION
1 : Vin1
2 : SW1
3 : Vin2
4 : SW2
5 : Vin3
6 : V+
7 : V_{OUT}
8 : GND

NJM2535L

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

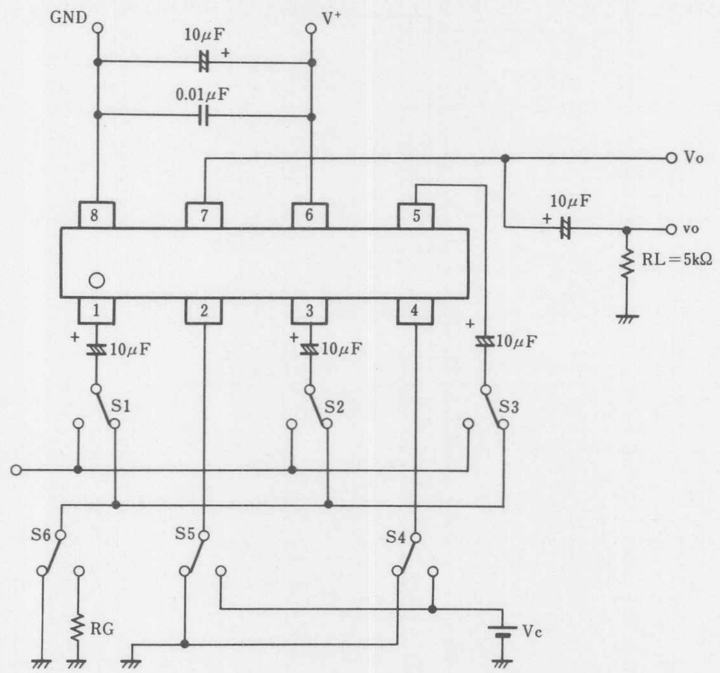
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+15	V
Power Dissipation	P_D	(DIP-8) 500 (DMP-8) 300 (SIP-8) 800 (SSOP-8) 250	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+		+4.5		+13.0	V
Supply Current	I_{CC}		−	3.6	4.6	mA
Frequency Characteristics	Gf	V_{IN}=2Vpp, Vo=10MHz/100kHz	−1.0	0	+1.0	dB
Voltage Gain	G_V	V_{IN}=2Vpp, 100kHz	−0.5	0	+0.5	dB
Differential Gain	DG	V_{IN}=2Vpp, Standard staircase signal, APL=50%	−	0	3.0	%
Differential Phase	DP	V_{IN}=2Vpp, Standard staircase signal, APL=50%	−	0	3.0	deg
Output Offset Voltage	V_{off}		−30	0	+30	mV
Crosstalk	CT	V_{IN}=2Vpp, 4.3MHz	−	−70	−60	dB
Switching Voltage	V_{CH}		2.4	−	−	V
	V_{CL}		−	−	0.8	V
Input Impedance	R_I		−	30	−	kΩ
Output Impedance	R_o		−	25	−	Ω
Input Bias Voltage	V_{IN}		−	2.5	−	V

■ TEST CIRCUIT



COMMUNICATION

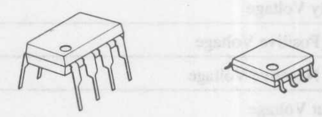
6

TONE DECODER/PHASE LOCKED LOOP

■ GENERAL DESCRIPTION

The NJM567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth cebter frequency, and output delay are independently determined by means of four external components.

■ PACKAGE OUTLINE

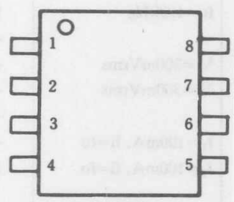


NJM567D NJM567M

■ FEATURES

- Operating Voltage (4.75V~9.0V)
- Wide frequency range (0.01Hz to 500kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14 percent)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Frequency adjustment over a 20 to 1 range with an external resistor
- Package Outline DIP8, DMP8
- Bipolar Technology

■ PIN CONFIGURATION

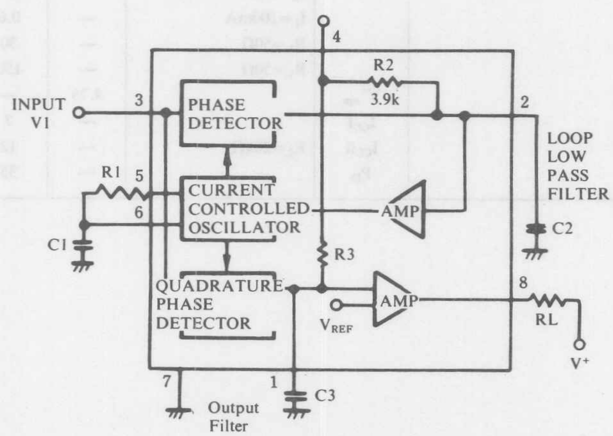


NJM567D
NJM567M

PIN FUNCTION

1	OUTPUT FILTER
2	LOW-PASS FILTER
3	INPUT
4	V+
5	TIMING R
6	TIMING CR
7	GROUND
8	OUTPUT

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	10	V
Input Positive Voltage	V_{IP}	$V^+ + 0.5$	V
Input Negative Voltage	V_{IN}	-10	Vdc
Output Voltage	V_8	15	Vdc
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
Operating Temperature Range	T_{opr}	$-20 \sim +75$	℃
Storage Temperature Range	T_{stg}	$-40 \sim +125$	℃

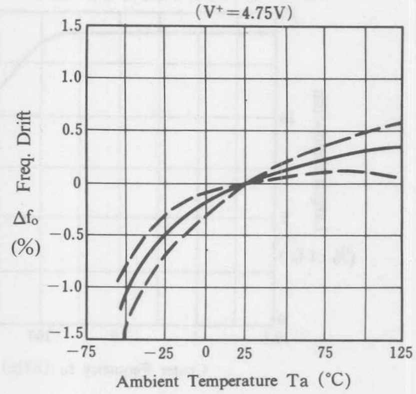
■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V^+=5.0V)

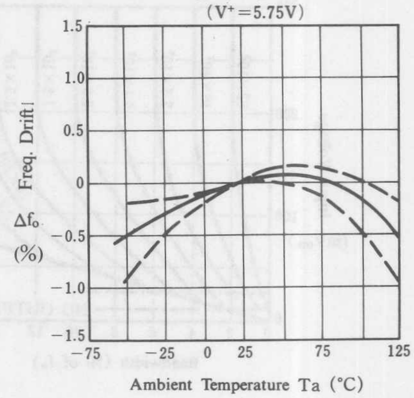
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Highest Center Frequency	f_{OH}		100	500	—	kHz
Center Frequency Stability	$\Delta fo/\Delta T$	$-20 \sim +75$°C	—	35±60	—	PPM/°C
Center Frequency Shift with Supply Voltage	$\Delta fo/\Delta V$	fo=100kHz	—	0.7	2	%/V
Largest Detection Bandwidth	B_{WM}	fo=100kHz	10	14	18	%×fo
Largest Detection Bandwidth Skew	B_{WS}		—	2	3	%×fo
Largest Detection Bandwidth Variation with Temperature	$\Delta B_W/\Delta T$	Vi=300mVrms	—	±0.1	—	%/°C
Largest Detection Bandwidth Variation with Supply Voltage	$\Delta B_W/\Delta V$	Vi=300mVrms	—	±2	—	%/V
Input Resistance	R_{IN}		—	20	—	kΩ
Smallest Detectable Input Voltage		I_L=100mA, fi=fo	—	20	25	mVrms
Largest No-Output Input Voltage		I_L=100mA, fi=fo	10	15	—	mVrms
Greatest Simultaneous Outband Signal to Inband Signal Ratio			—	+6	—	dB
Minimum Input Signal to Wideband Noise Ratio		B_n=140kHz	—	−6	—	dB
Fastest ON-OFF Cycling Rate			—	fo/20	—	
"1" Output Leakage Current			—	0.01	25	μA
"0" Output Voltage		I_L=30mA	—	0.2	0.4	V
		I_L=100mA	—	0.6	1.0	V
Output Fall Time		R_L=50Ω	—	30	—	ns
Output Rise Time		R_L=50Ω	—	150	—	ns
Operating Voltage	V^+_{opr}		4.75	—	9.0	V
Operating Current Quiescent	$I_{CC}I$		—	7	10	mA
Operating Current – Activated	$I_{CC}II$	R_L=20kΩ	—	12	15	mA
Quiescent Power Dissipation	P_D		—	35	—	mW

■ TYPICAL CHARACTERISTICS

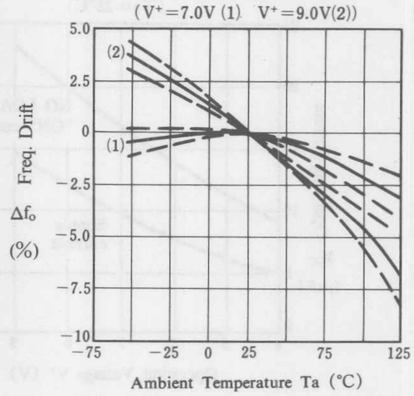
Frequency Drift
($V^+=4.75V$)



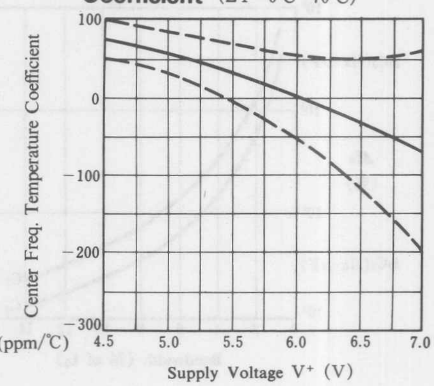
Frequency Drift
($V^+=5.75V$)



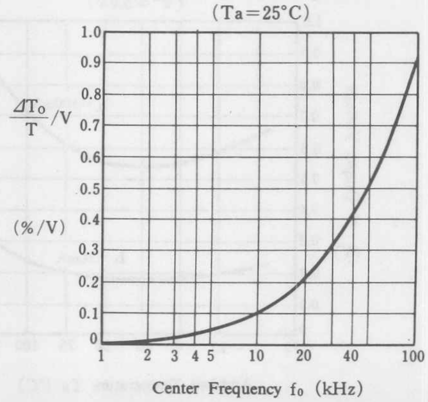
Frequency Drift
($V^+=7.0V$ (1) $V^+=9.0V$(2))



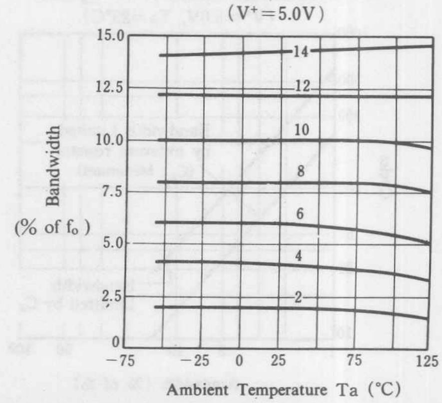
Center Frequency Temperature Coefficient ($\Delta T=0°C \sim 70°C$)



Center Frequency Shift
(Ta=25°C)

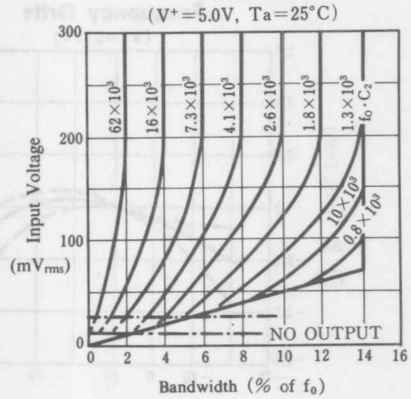


Detection Bandwidth
($V^+=5.0V$)

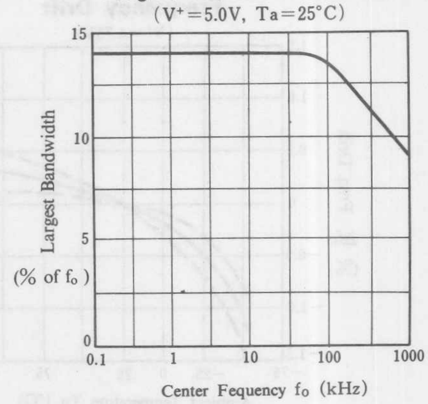


■ TYPICAL CHARACTERISTICS

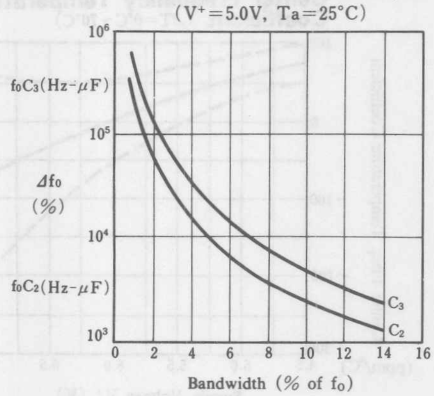
Bandwidth
(V^+=5.0V, Ta=25°C)



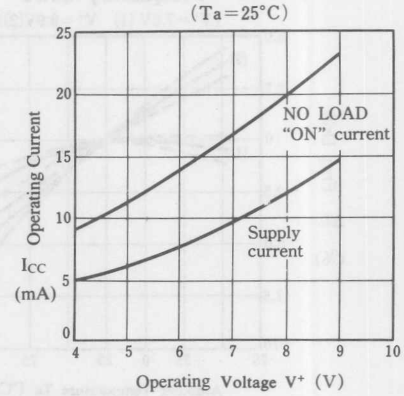
Largest Detection Bandwidth
(V^+=5.0V, Ta=25°C)



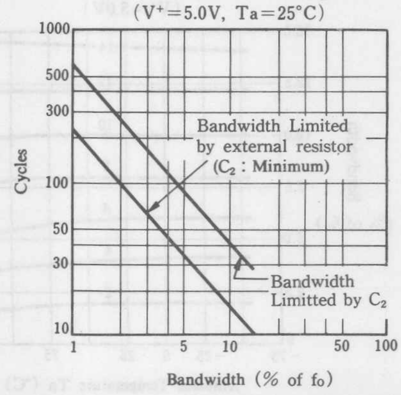
Detection Bandwidth vs. C2, C3
(V^+=5.0V, Ta=25°C)



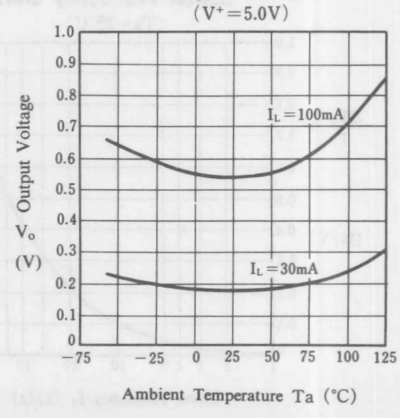
Operating Current
(Ta=25°C)



Greatest Number of Cycles
(V^+=5.0V, Ta=25°C)



Output Voltage
(V^+=5.0V)



■ DESIGN FORMULAS

$$f_o = \frac{1}{1.07\,R_1C_1} \quad (V_{IN} = 0mV)$$

$$BW \simeq 1070\sqrt{\frac{V_{IN}}{f_oC_2}} \text{ in \% of } f_o,\ V_{IN} \leqq 200mVrms$$

where V_{IN} : Input Voltage (Vrms)
C_2 : LPF Capacitor (μF)

■ PLL WORDS EXPLANATIONS

☆ **Center Frequency (f_o)**
The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

☆ **Detection Bandwidth (BW)**
The frequency range, centered about f_o, within which an input signal above the threshold voltage (typically 20mVrms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

☆ **Lock Range**
The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

☆ **Detection Band Skew**
A measure of how well the detection band is centered about the center frequency, f_o. The skew is defined as $(f_{max} + f_{min} - 2f_o)/2f_o$ where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

◎ **Operating Instructions**
Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

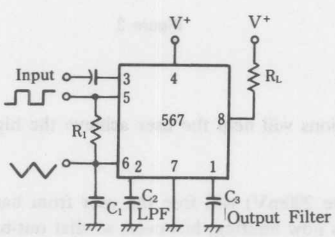


Figure 1

1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R_1C_1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.
2. Select the low pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of f_oC_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_oC_2 product (f_o (Hz), C_2 (μfd))
3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

◎ **Output Terminal** (Fig. 2)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_o with a slope of about 20mV per percent of frequency deviation. The average voltage at pin 1 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{be}) \approx (+V - 1.4V)$ having a dc average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of 1 volt peak-to-peak with an average dc level of +V2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

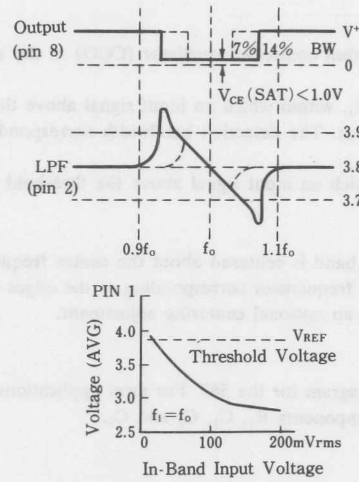


Figure 2

■ OPERATING PRECAUTINS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_o/3$, $f_o/5$, etc.
2. The 567 will lock onto signals near (2n + 1) f_o, and will give an output for signals near (4n + 1) f_o where n=0, 1, 2, etc. Thus, signals at 5f_o and 9f_o can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and outband signals is afforded in the low input level (below 200mVrms) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into an out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

◎ **Speed of Operation**

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away form the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o}\ \mu F$$

$$C_3 = \frac{260}{f_o}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

◎ **Optional Controls** (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

◎ **Sensitivity Adjustment** (Figure 3)

When operated as a very narrow band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for Lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most usefu when, to obtain maximum operating speed. C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

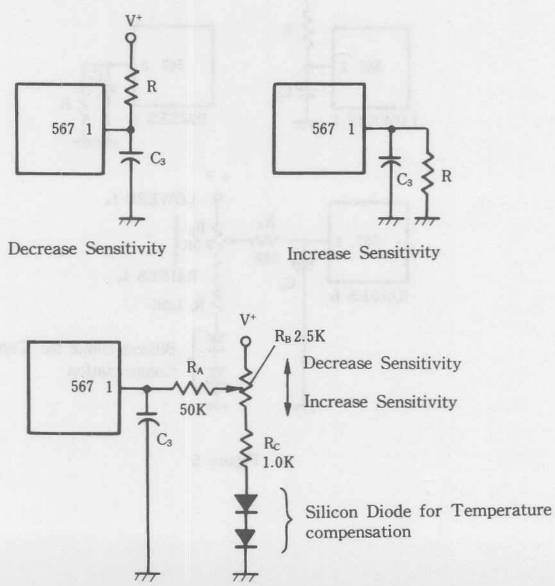


Figure 3

◎ **Chatter Prevention** (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

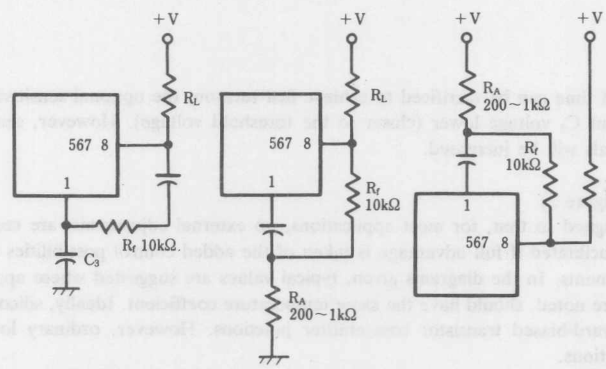


Figure 4

◎ **Detection Band Centering (or Skew) Adjustment** (Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

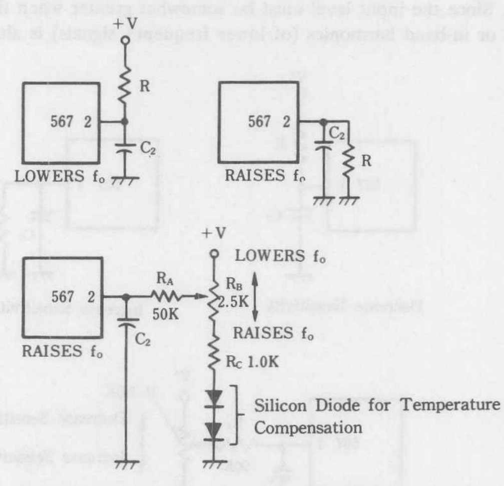


Figure 5

◎ **Alternate Method of Bandwidth Reduction** (Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve camping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

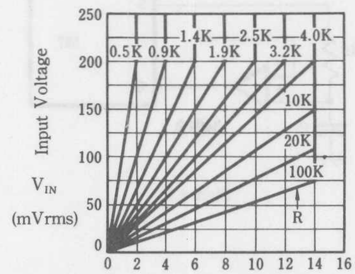
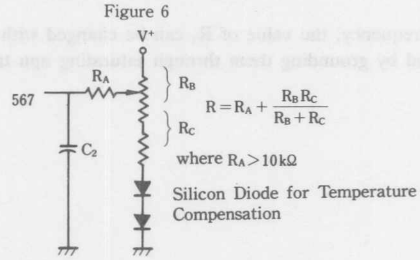


Figure 6



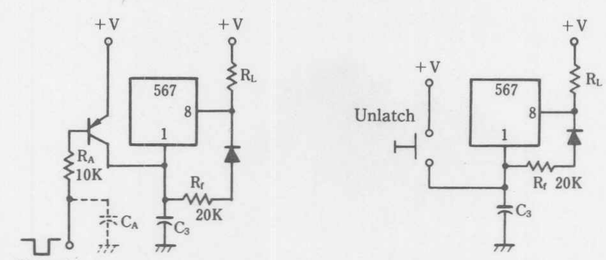
$$\frac{130}{f_o}\left(\frac{10K+R}{R}\right) < C_2 < \frac{1300}{f_o}\left(\frac{10K+R}{R}\right)$$

(note) Adjust control for symmetry of detection band edges about f_o.

◎ **Output Latching** (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

Output Latching



C_A prevents latch-up when power supply is turned on.

Figure 7

◎ **Reduction of C_1 Value** (Figure 8)

For precision very low-frequency applictions, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and lower value of C_1 for a given frequency.

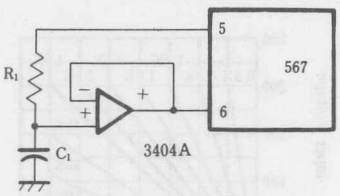


Figure 8

◎ **Programming**

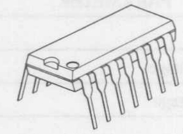
To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.

DOUBLE BALANCED MODULATOR/DEMODULATOR

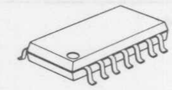
■ GENERAL DESCRIPTION

The NJM1496 is a double balanced modulator-demodulator which produces an output voltage proportional to the product of an input (signal) voltage and a switching (carrier) signal. Typical applications include suppressed carrier modulation, amplitude modulation, synchronous detection, FM or PM detection, broadband frequency doubling and chopping.

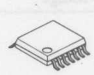
■ PACKAGE OUTLINE



NJM1496D



NJM1496M



NJM1496V

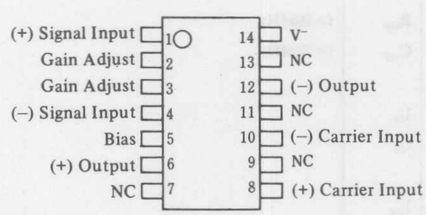
■ FEATURES

- Excellent carrier suppression
  65dB typical at 0.5MHz
  50 dB typical at 10MHz
- Adjustable gain and signal handling
- Fully balanced inputs and outputs
- High Common Mode Rejection 85dB Typ.
- Package Outline DIP14, DMP14, SSOP14
- Bipolar Technology

■ APPLICATION

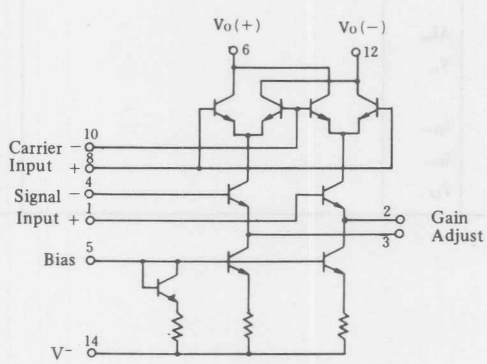
- Balanced Modulation
- Synchronous Detection
- FM Detection
- Phase Detection
- Sampling

■ PIN CONFIGURATION



NJM1496D
NJM1496M
NJM1496V

■ EQUIVALENT CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	RATINGS	UNIT
Applied Voltage	30(Applied Pins 6-8, 12-8, 6-10, 12-10, 10-1, 8-1, 10-4, 8-4, 2-5, 3-5)	V
Carrier Input Voltage	±5(Applied Pins 8-10)	V
Signal Input Voltage	$\pm(5+I_5 Re)$ (Applied Pins 1-4)	V
Input Signal	5	V
Bias Current (I_5)	10	mA
Power Dissipation	(DIP14) 570	mW
	(DMP14) 300	mW
	(SSOP14) 300	mW
Operating Temperature Range	−20～+75	℃
Storage Temperature Range	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

DC Characteristics (V^+=12V, V^-=−8V, I_5=1.0mA, R_L=3.9kΩ, Re=1.0kΩ, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Single-Ended Input Impedance						
Parallel Input Resistance	R_{ip}	Signal Port, f=5.0MHz	—	200	—	kΩ
Parallel Input Capacitance	C_{ip}	Signal Port, f=5.0MHz	—	2.0		pF
Single-Ended Output Impedance						
Parallel Output Resistance	R_{op}	f=10MHz	—	40	—	kΩ
Parallel Output Capacitance	C_{op}	f=10MHz	—	5.0	—	pF
Input Bias Current						
$I_{bs}=I_1+I_4/2$	I_{bs}		—	12	30	μA
$I_{bc}=I_8+I_{10}/2$	I_{bc}		—	12	30	μA
Input Offset Current						
$I_{ios}=I_1-I_4$	I_{ios}		—	0.7	7	μA
$I_{ioc}=I_8-I_{10}$	I_{ioc}		—	0.7	7	μA
Average Temperature Coefficient of Input Offset Current	ΔI_{io}		—	2.0	—	nA/°C
Output Offset Current (I_6-I_{12})	I_{oc}		—	15	80	μA
Average Temperature Coefficient of Output Offset Current	ΔI_{oc}		—	90	—	nA/°C
Output Voltage	V_o		—	8.0	—	V
Operating Current						
(I_6+I_{12})	I_{D+}		—	2.0	4.0	mA
I_{14}	I_{D-}		—	3.0	5.0	mA
DC Power Dissipation	P_D		—	33	—	mW

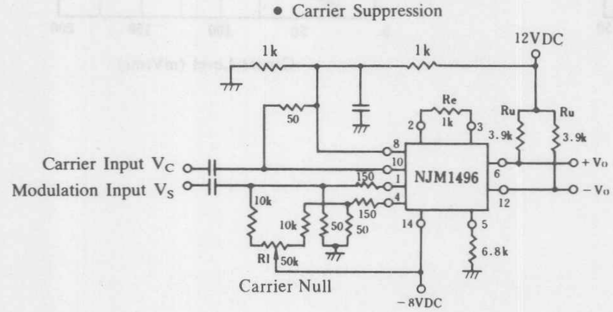
■ ELECTRICAL CHARACTERISTICS

AC Characteristics (V^+=12V, V^-=−8V, I_5=1.0mA, R_L=2.9kΩ, Re=1.0kΩ, Ta=25℃)

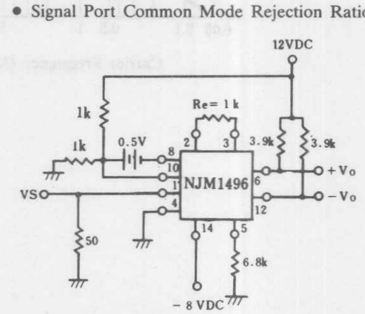
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Carrier Feedthrough		Vc= 60mVrms sine wave				
		offset adjusted				
	V_{CFT}	fc=1.0kHz	—	40	—	μVrms
	V_{CFT}	fc=10MHz	—	140	—	μVrms
		Vc= 300mVp-p square wave				
		fc=1.0kHz				
	V_{CFT}	offset adjusted	—	0.04	0.4	mVrms
	V_{CFT}	offset not adjusted	—	20	200	mVrms
Carrier Suppression		fs = 10kHz, 300mVrms sine wave				
		offset adjusted				
	V_{CS}	fc = 500kHz, 60mVrms sine wave	40	65	—	dB
	V_{CS}	fc = 10MHz, 60mVrms sine wave	—	50	—	dB
Transadmittance Bandwidth						
(R_L = 50Ω)		Vc= 60mVrms sine wave				
Carrier Input Port	BW 3dB	fs = 1.0kHz, 300mVrms sine wave	—	300	—	MHz
Signal Input Port	BW 3dB	Vs = 300mVrms sine wave		80		MHz
		|Vc|=0.5Vdc				
Voltage Gain, Signal Channel		Vs = 100mVrms fs=1.0kHz				
	AV_S	|Vc|=0.5Vdc	2.5	3.5	—	V/V
Signal Port Common Mode Input Voltage						
Range	CM_V	fs = 1.0kHz	—	5.0	—	Vp-p
Signal Port Common Mode Rejection Ratio	ACM	fs = 1.0kHz, |Vc|=0.5Vdc	—	−85	—	dB
Differential Output Swing Capability	DV_{out}		—	8.0	—	Vp-p

■ TEST CIRCUIT

- Carrier feedthrough
- Carrier Suppression



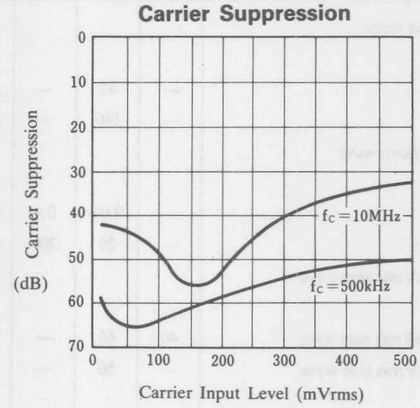
- Differential Output Swing Capability
- Signal Port Common Mode Rejection Ratio



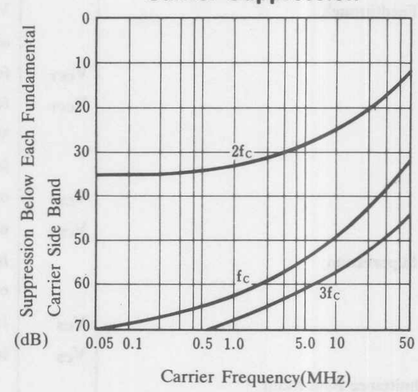
Connect a 100μF capacitor and a 3000pF capacitor in parallel to each other, if the capacitance is not specified.

■ TYPICAL CHARACTERISTICS

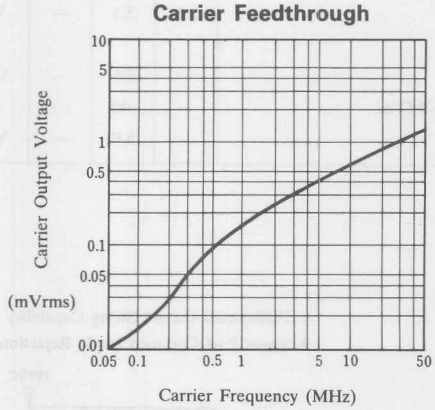
Carrier Suppression



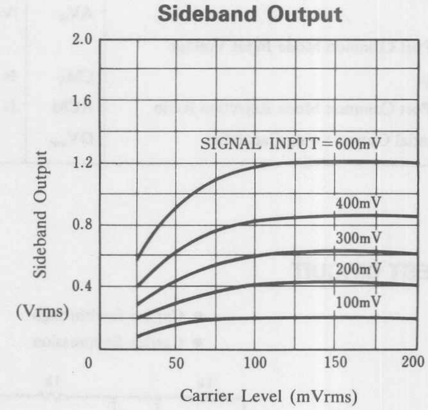
Carrier Suppression



Carrier Feedthrough

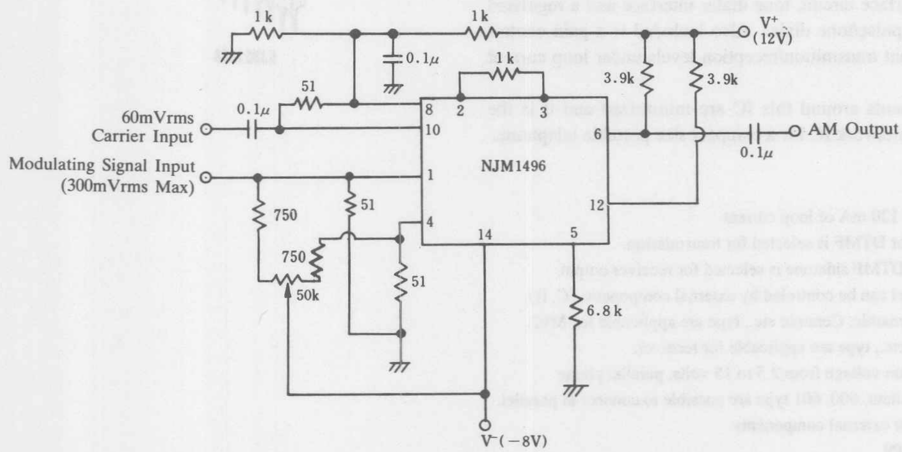


Sideband Output

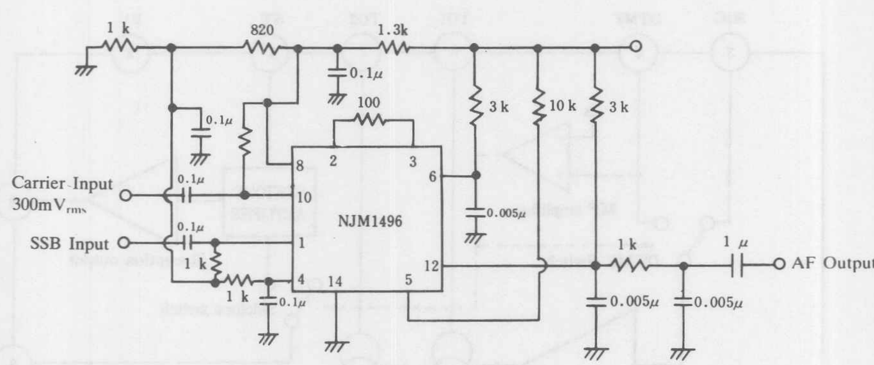


■ TYPICAL APPLICATIONS

AM Modulator Circuit



Product Detector (+12V DC Single Supply)



TELEPHONE SPEECH NETWORK IC

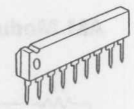
■ GENERAL DESCRIPTION

The NJM2105 is a Telephone Speech Network IC produced in a 9-pin single-in-line package which complies with foreign regulations such as FCC and DOC rules.

This IC incorporates adjustable transmit, receive and sidetone functions, a DC loop interface circuit, tone dialer interface and a regulated output voltage for a pulse/tone dialer. Also included is a gain control circuit to keep constant transmition/reception levels under loop current variations.

External components around this IC are minimized and it is the most suitable speech network IC for a compact size portable telephone.

■ PACKAGE OUTLINE

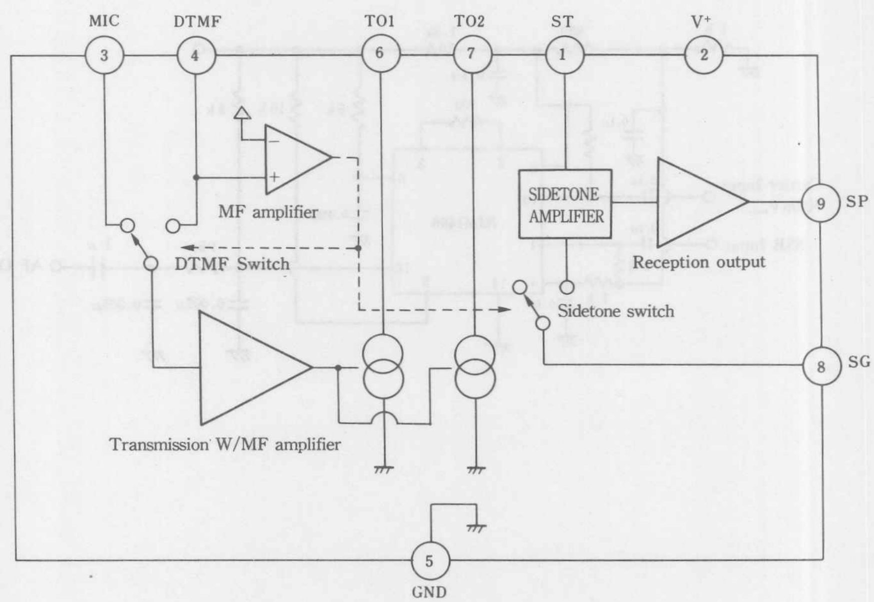


NJM2105S

■ FEATURES

- Operates with 20 to 120 mA of loop current
- Either voice signal or DTMF is selected for transmission.
- Either line input or DTMF sidetone is selected for receiver output.
- DTMF sidetone level can be controled by external components (C, R).
- ECM, Magnetic, Dynamic, Ceramic etc., type are applicable for MIC.
- Dynamic, Ceramic etc., type are applicable for receiver.
- Due to wide operation voltage from 2.5 to 15 volts, parallel phone performance is excellent, 600, 601 type are possible to connect in parallel.
- SIP-9 with minimum external components.
- Package Outline SIP9
- Bipolar Technology

■ BLOCK DIAGRAM



NJM2105S

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

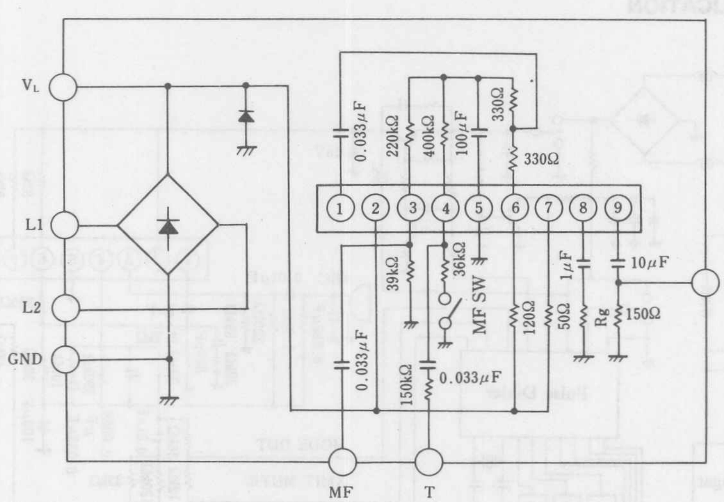
PARAMETER	SYMBOL	RATINGS	UNIT
Line voltage	V_L	20	V
Line current	I_L	300	mA
Power dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^{+}=5V, Ta=25℃)

PARAMETER	SYMBOL	FIG.	CONDITION	MIN.	TYP.	MAX.	UNIT
Line voltage	V_L	1	I_L =20mA	3.0	3.5	4.0	V
		1	I_L =120mA	10.5	11.5	13.5	V
Transmission amplifier gain	G_T	2	I_L =20mA	36.0	38.0	40.0	dB
		2	I_L =120mA	36.0	38.0	40.0	dB
Reception amplifier gain	G_R	4	I_L =20mA	−10.0	−8.0	−6.0	dB
		4	I_L =120mA	−10.0	−8.0	−6.0	dB
MF amplifier gain	G_{MF}	3	I_L =20mA	10.0	12.0	14.0	dB
		3	I_L =120mA	10.0	12.0	14.0	dB
Transmission Dynamic Range	D_T	2	Distortion 4% I_L =20mA	2.0	—	—	V_{P-P}
		2	Distortion 4% I_L =120mA	5.0	—	—	V_{P-P}
Reception Dynamic Range	D_R	4	Distortion 10% I_L =20mA	0.3	—	—	V_{P-P}
		4	Distortion 10% I_L =120mA	0.4	—	—	V_{P-P}
Receving Source Current	I_S	—	I_L =20～120mA	1.0	—	—	mA
Receiving output	V_{RO}	—	I_L =20～120mA	1.05	1.50	1.75	V

■ TEST CIRCUITS



■ TEST CIRCUITS

Fig. 1

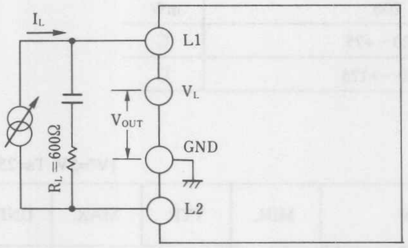


Fig. 2

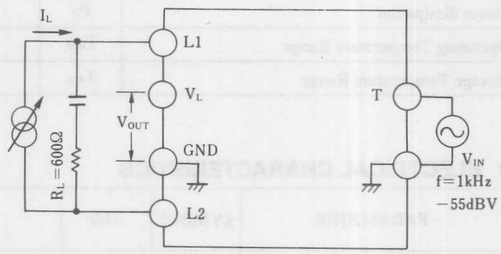


Fig. 3

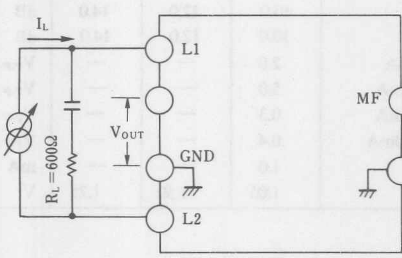
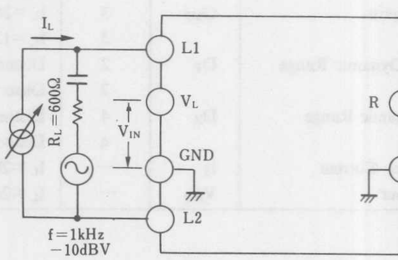
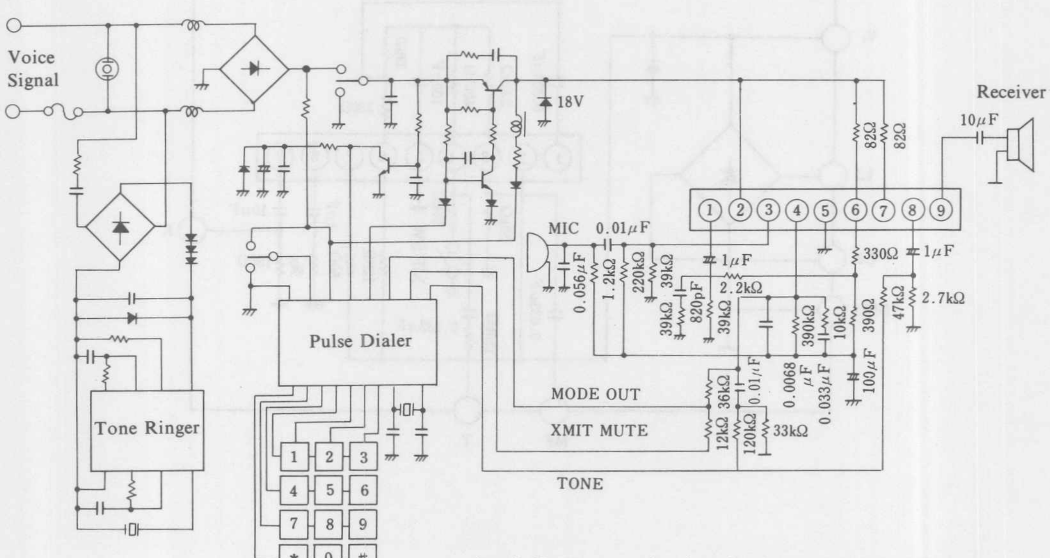


Fig. 4



■ TYPICAL APPLICATION

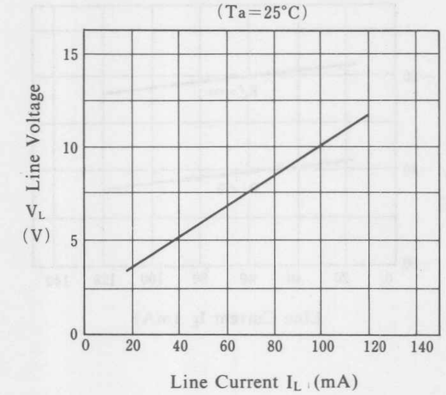


(note) Constant number is rating by case that use ECM and Dynamic Speaker.

■ TYPICAL CHARACTERISTICS

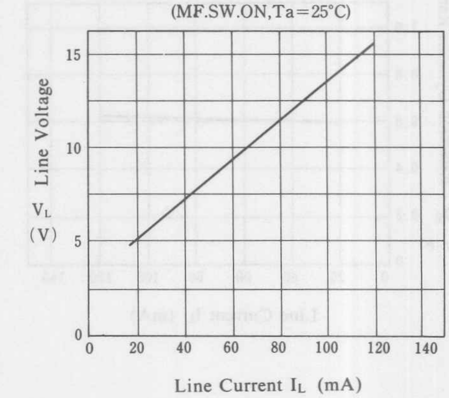
Line Voltage vs. Line Current

(Ta=25°C)



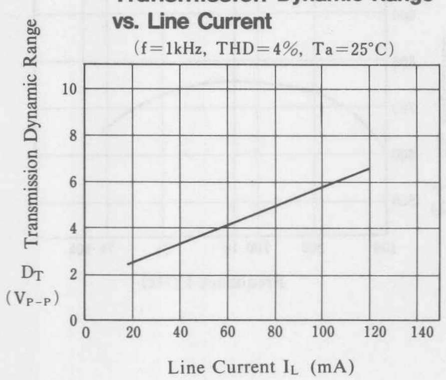
MF Line Voltage vs. Line Current

(MF.SW.ON,Ta=25°C)



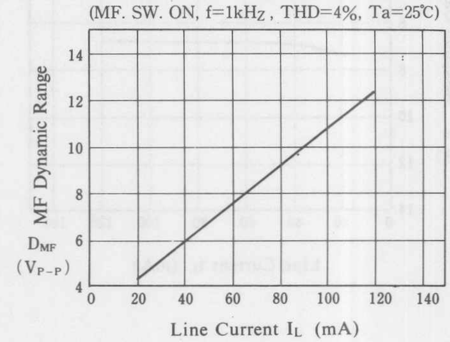
Transmission Dynamic Range vs. Line Current

(f=1kHz, THD=4%, Ta=25°C)



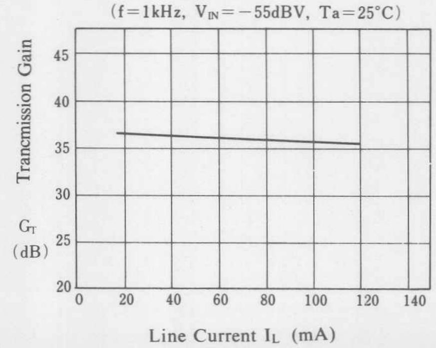
MF Dynamic Range vs. Line Current

(MF. SW. ON, f=1kHz, THD=4%, Ta=25℃)



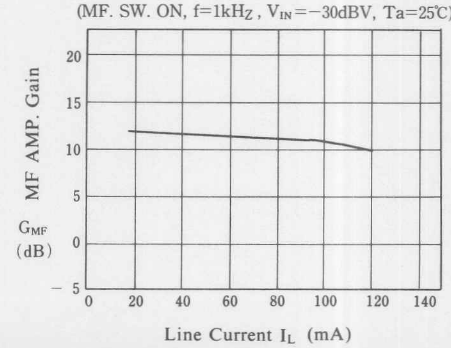
Transmission Gain vs. Line Current

(f=1kHz, V_{IN}=−55dBV, Ta=25°C)



MF AMP. Gain vs. Line Current

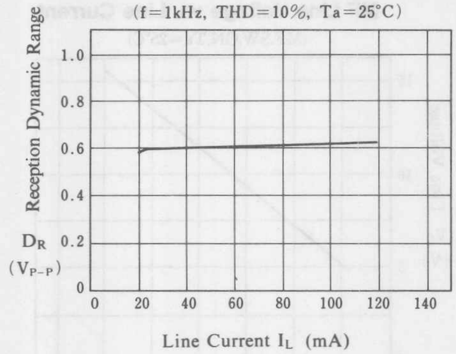
(MF. SW. ON, f=1kHz, V_{IN}=−30dBV, Ta=25℃)



■ TYPICAL CHARACTERISTICS

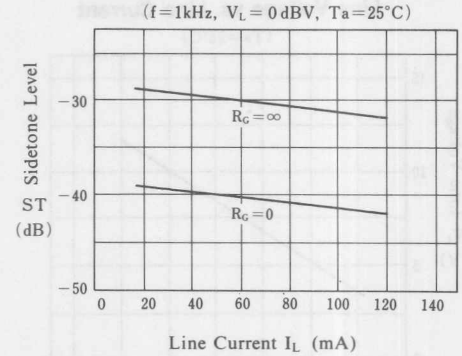
Reception Dynamic Range vs. Line Current

(f=1kHz, THD=10%, Ta=25°C)



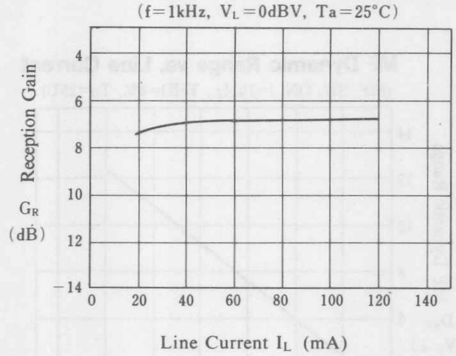
Sidetone Level vs. Line Current

(f=1kHz, V_L=0dBV, Ta=25°C)



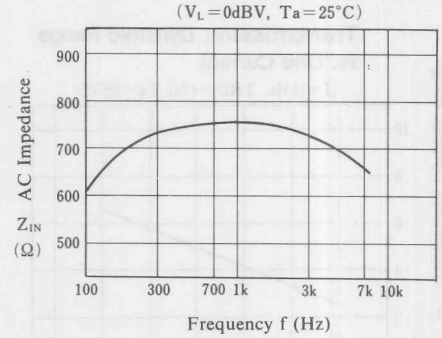
Reception Ganin vs. Line Current

(f=1kHz, V_L=0dBV, Ta=25°C)



AC Impedance vs. Ferequency

(V_L=0dBV, Ta=25°C)

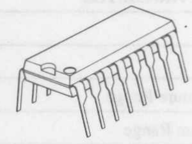


FULL BALANCED MIXER

■ GENERAL DESCRIPTION

The NJM2203D is a full balanced mixer integrated circuit for FM synthesizing tuner. The NJM2203D contains mixer, oscillator, buffer for oscillator output and IF amplifier circuits. By using this IC, RF circuit configuration is simplified and high reliability, stable operation, easy design and time saving adjustment are realized.

■ PACKAGE OUTLINE

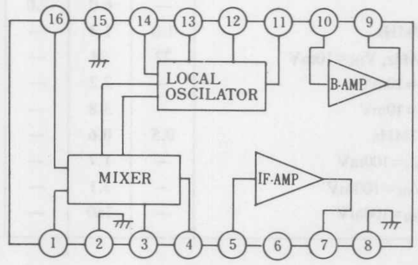


NJM2203D

■ FEATURES

- Minimum outer parts.
- Simplified circuit configuration
- Minimum frequency deviation with over input signal.
- Easy adjustment.
- Package Outline DIP16
- Bipolar Technology

■ BLOCK DIAGRAM

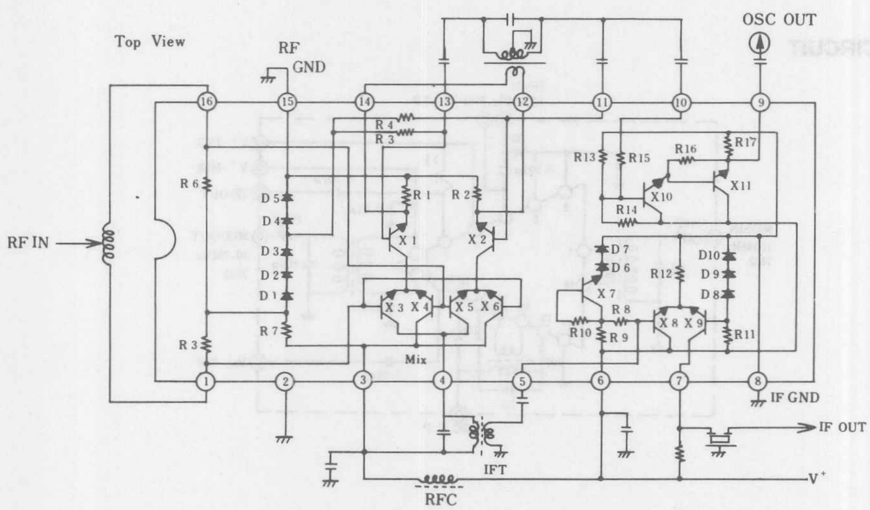


NJM2203D

PIN FUNCTION

1. RF INPUT1	9. OSC OUT
2. GND	10. OSC Buffer INPUT
3. V^+_M	11. OSC1
4. Mix OUT	12. OSC2
5. Mix INPUT	13. OSC3
6. V^+_A	14. OSC4
7. IF OUT	15. GND(RF)
8. GND(IF)	16. RF INPUT2

■ EQUIVALENT CIRCUIT



NJM2203D

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	18	V
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

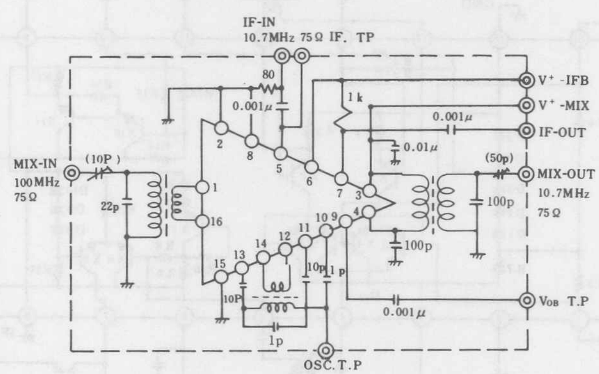
■ ELECTRICAL CHARACTERISTICS

(V^+=12V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current (MIX)	I_{CCM}	STC, no signal	2.5	3.2	3.8	mA
Supply Current (IF+B)	I_{CCA}	STC, no signal	8.8	11.0	13.2	mA
Conversion Power Gain (MIX)	P_G	STC, fosc=100MHz, Vin=1mV	21	24	27	dB
Noise Figure (MIX)	NF	STC	—	6.0	7.0	dB
Local Oscillater Voltage (OSC)	V_{OSC}	STC, fosc=110.7MHz	1.0	1.3	—	V
Voltage Gain (IF)	V_G	STC, f_{IF}=10.7MHz, V_{IN}=10mV	22	28	—	mV/mV
Input Resistance (IF)	$R_I(IN)$	f=10.7MHz, V_{IN}=10mV	—	3.2	—	kΩ
Input Capacitance (IF)	$C_I(IN)$	f=10.7MHz, V_{IN}=10mV	—	3.8	—	pF
Local Osc. Buffer Output (O)	V_{OB}	STC, f_{OSC}=110.7MHz	0.5	0.6	—	V
Input Resistance (O-Buf)	$R_O(IN)$	f=110.7MHz, V_{IN}=100mV	—	1.7	—	kΩ
Input Capacitance (O-Buf)	$C_O(IN)$	f=110.7MHz, V_{IN}=100mV	—	3.1	—	pF
Output Resistance (O-Buf)	$R_O(OUT)$	f=110.7MHz, V_{IN}=100mV	—	160	—	Ω

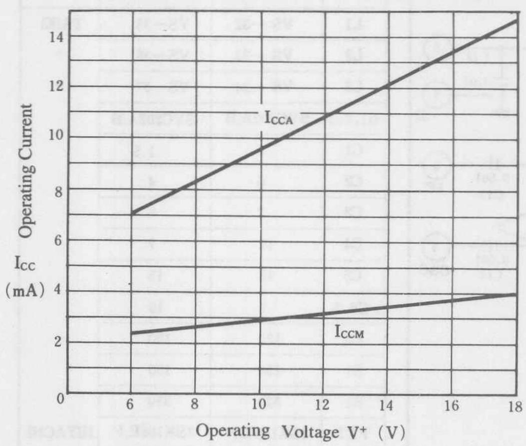
note: STC: Specified Test Circuit

■ TEST CIRCUIT

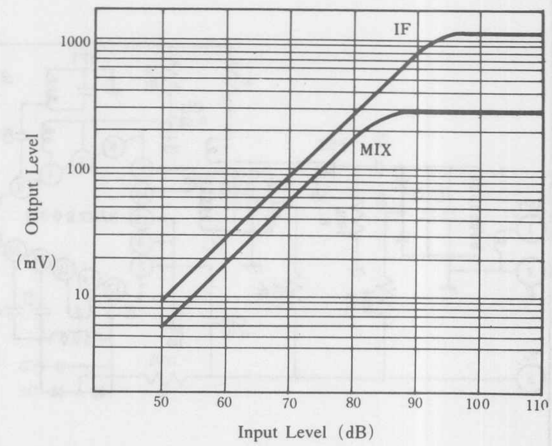


■ TYPICAL CHARACTERISTICS

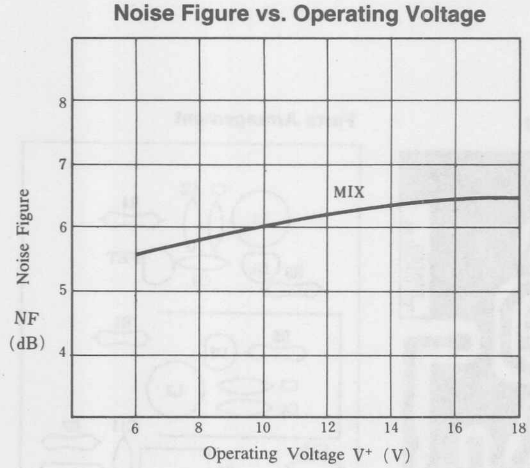
Operating Current vs. Supply Voltage



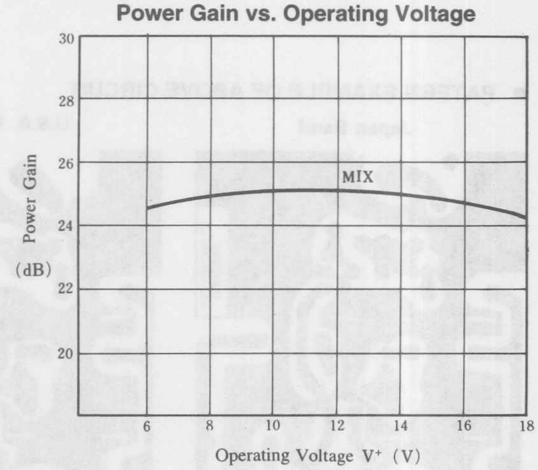
Output Level vs. Input Level



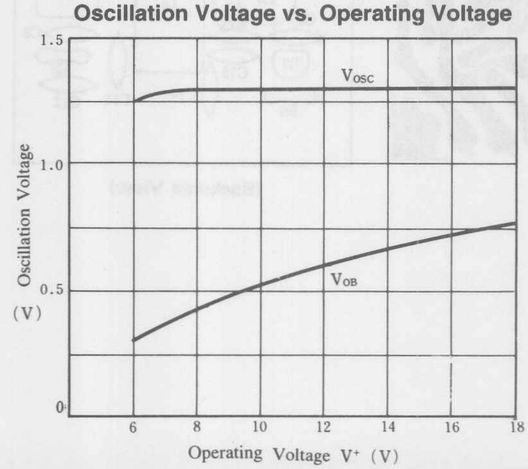
Noise Figure vs. Operating Voltage



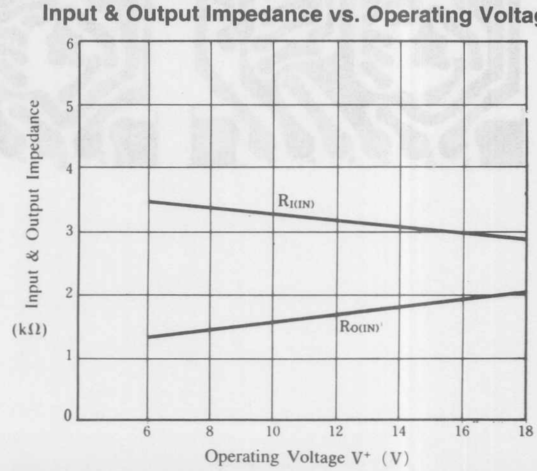
Power Gain vs. Operating Voltage



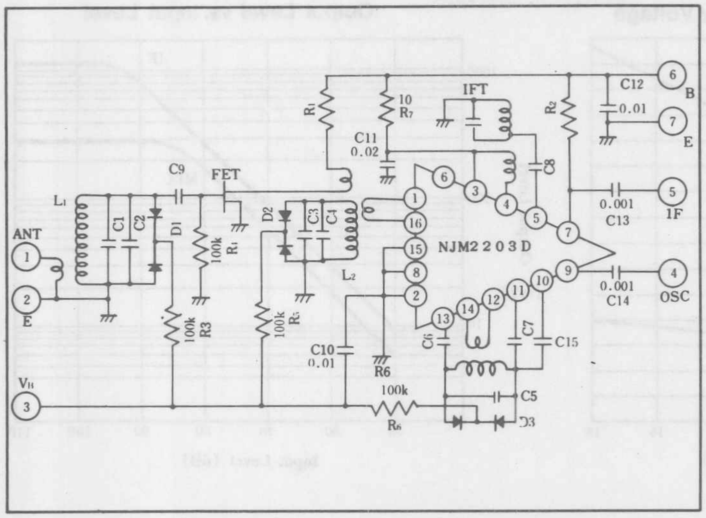
Oscillation Voltage vs. Operating Voltage



Input & Output Impedance vs. Operating Voltage



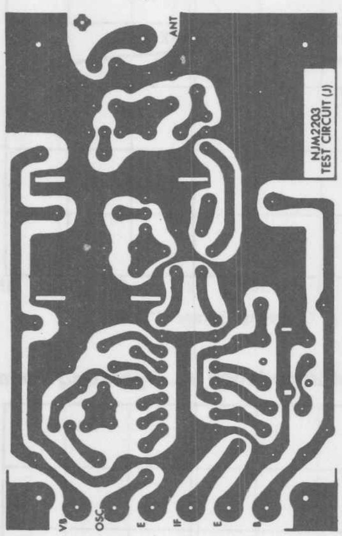
■ TYPICAL APPLICATION



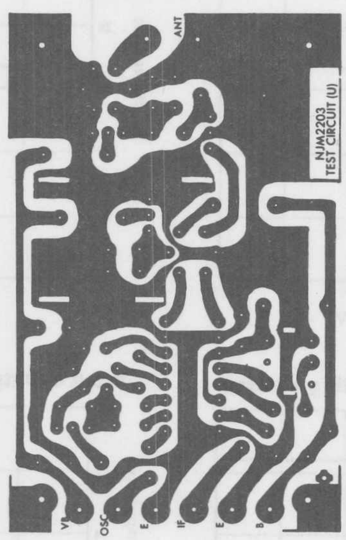
	76~90MHz	88~108MHz	
L1	VS −32	VS−35	TAIKI
L2	VS −33	VS−36	〃
L3	VS −34	VS−37	〃
D1,2,3	SVC202A,B	SVC202A,B	
C1	6	1.5	
C2	6	4	
C3	7	6	
C4	12	7	
C5	15	15	
C6,7	5	10	
C8	120	120	
R1	150	150	
R2	330	330	
FET	2SK168E,F	2SK168E,F	HITACHI
IFT	154FC−41921N		TOKO

■ PATERN EXAMPLE OF ABOVE CIRCUIT

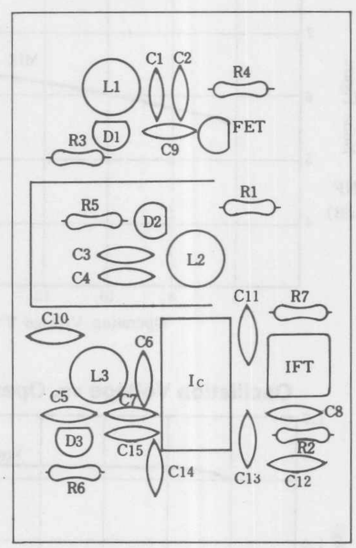
Japan Band



U.S.A. Band



Parts Arrangement



(Backside View)

LOG AMPLIFIER

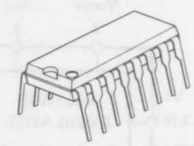
■ GENERAL DESCRIPTION

The NJM2204A is an integrated IF limitting amplifier which contains temperature compensated reference power supply, 6 stage differential limitting amplifier and 6 stage logarithmic suppression circuit.

Its voltage gain is 58dB and linearity is ±1dB within 50dB log dynamic range. The voltage gain and log dynamic range are enlarged by connecting multiple stages.

The NJM2204A is suitable to telecommunication equipment.

■ PACKAGE OUTLINE



NJM2204AD

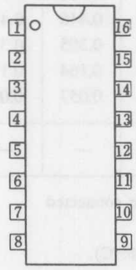
■ FEATURES

- Wide log dynamic range (50dB)
- Wide linearity range (±1dB)
- Large Voltage Gain (58dB)
- Wide stable operating supply voltage range (8～12V)
- Wide stable operating temperature range (−20～85℃)
- Package Outline DIP16
- Bipolar Technology

■ APPLICATION

- Cellular
- Personal wireless Radio
- Business wireless Radio
- Handy talky

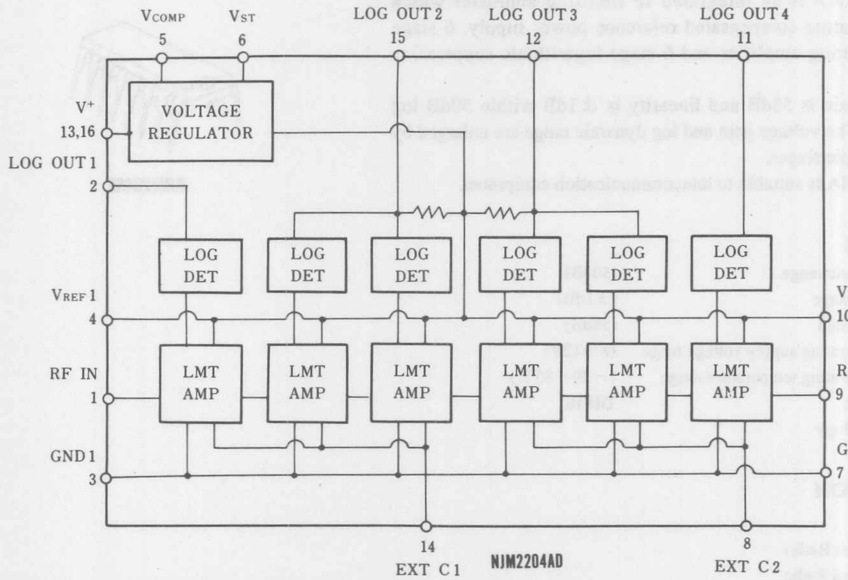
■ PIN CONFIGURATION



NJM2204AD

Pin No.	Pin Name	Function
1	RF IN	AC Signal Input (C-coupling)
2	LOG OUT 1	LOG Detector Output (from 1st stage)
3	GND 1	Ground 1
4	V_{REF} 1	Internal Reference Voltage 1
5	V_{COMP}	Compensation Input to Reference Voltage
6	V_{st}	Compensated Output of Reference Voltage
7	GND 2	Ground 2
8	EXT C2	Terminate with C
9	RF OUT	Limitted AC Output
10	V_{REF} 2	Internal Reference Voltage 2
11	LOG OUT 4	LOG Detector Output (from 6th stage)
12	LOG OUT 3	LOG Detector Output (from 4th and 5th stage)
13	V^+ 2	Supply Voltage Input 2
14	EXT C1	Terminate with C
15	LOG OUT 2	LOG Detector Output (from 2nd and 3rd stage)
16	V^+ 1	Supply Voltage Input 1

■ BLOCK DIAGRAM



■ LOG DETECTOR OUTPUT CHARACTERISTICS (EXAMPLE)

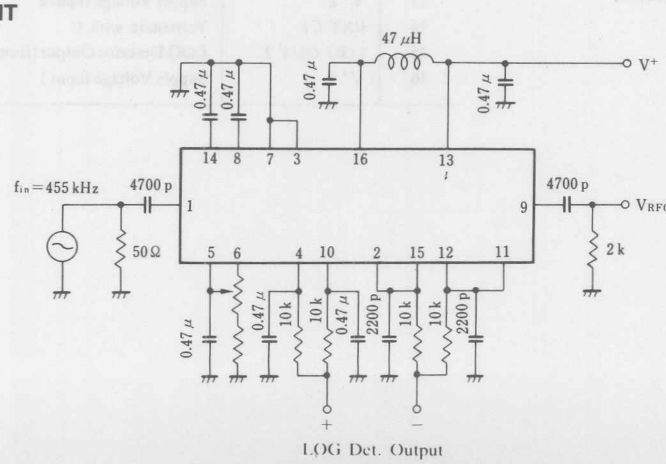
(Ta=25℃, V^+=9V, V_{REF}=6.0V)

PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Log Detector Output	f_{in}=455kHz, V_{in}=8dB (50Ω termination)	0.976	1.004	1.032	V
	f_{in}=455kHz, V_{in}=−2dB (50Ω termination)	0.868	0.896	0.924	V
	f_{in}=455kHz, V_{in}=−12dB (50Ω termination)	0.727	0.755	0.783	V
	f_{in}=455kHz, V_{in}=−22dB (50Ω termination)	0.586	0.614	0.642	V
	f_{in}=455kHz, V_{in}=−32dB (50Ω termination)	0.446	0.474	0.502	V
	f_{in}=455kHz, V_{in}=−42dB (50Ω termination)	0.305	0.333	0.361	V
	f_{in}=455kHz, V_{in}=−52dB (50Ω termination)	0.164	0.192	0.202	V
	f_{in}=455kHz, V_{in}=−62dB (50Ω termination)	0.057	0.085	0.113	V
Log Detector Linearity	Ta=−20°C~85°C, V_{in}=−2~−52dBm	—	—	±1	dB

* Log Detection Linearity: It is error between RF input level and ideal input level to straight line connected two detection output points of two input level (−2dBm, −52dBm).

* Temperature coefficient of Log detection output voltage: approximately 90μV/°C Typ. (−20~+85°C).

■ TEST CIRCUIT



■ RECOMMENDED OPERATING CONDITION

(Ta=−20~85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+	8.0	9.0	16.0	V
Output Load Impedance	B_{RFO}	1	2	—	kΩ
	B_{LOGO}	100	—	—	kΩ
Stabilized Voltage	V_{VR}	—	6.0	—	V

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+	−0.5~16.0	V
Input Voltage	V_{IN}	−0.5~V^+	V
Output Current	I_{LR}	5	mA
	I_{RFO}	2	mA
Operating Temperature	T_{opr}	−20~85	°C
Storage Temperature	T_{stg}	−55~125	°C

(note): The NJM2204A is produced by high frequency wafer process and so destructive voltage against surge pulse is lower than low frequency product.

■ ELECTRICAL CHARACTERISTICS

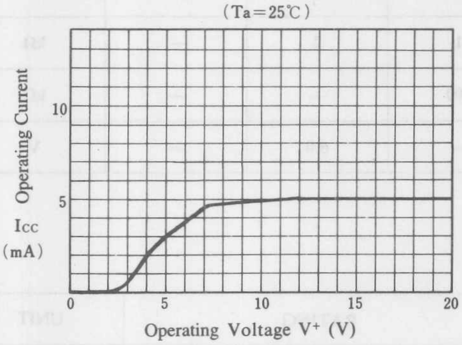
(Ta=25°C, V^+=9V, V_{REF}=6.0V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}		—	6	10.0	mA
Maximum Operating Frequency	f_{max}		0.5	3	—	MHz
Output Voltage Swing	V_{RFO}	Input: +8dBm (50Ω termination)	—	2.0	—	V_{P-P}
Log Detection Output	V_{LOG}	Input: +8dBm (50Ω termination)	—	1.0	—	V
Log Detection Linearity	L_{IN}	V_{in}=−2dBm~−52dBm (50Ω termination)	—	—	±1	dB
Limitter Amp Gain	G_V		60	—	—	dB

■ TYPICAL CHARACTERISTICS

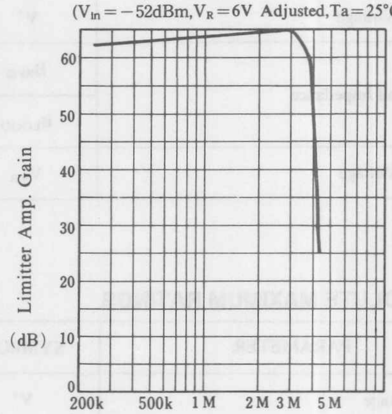
Operating Current vs. Operating Voltage

(Ta=25℃)



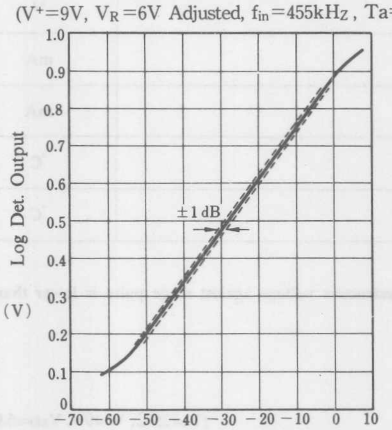
Limitter Amp Gain

($V_{in}=-52$dBm, $V_R=6$V Adjusted, Ta=25°C)



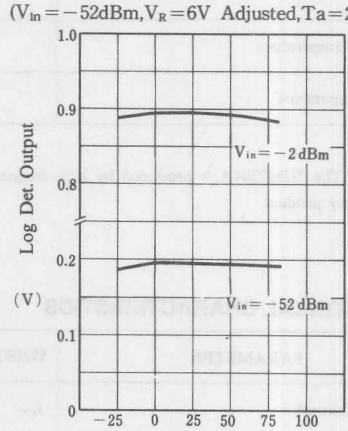
Log Detector Output

(V^+=9V, V_R=6V Adjusted, f_{in}=455kHz, Ta=25℃)



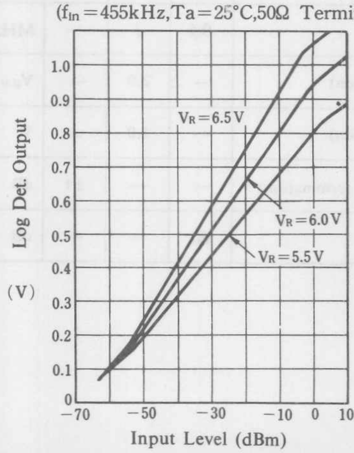
Log Detector Output

($V_{in}=-52$dBm, $V_R=6$V Adjusted, Ta=25°C)

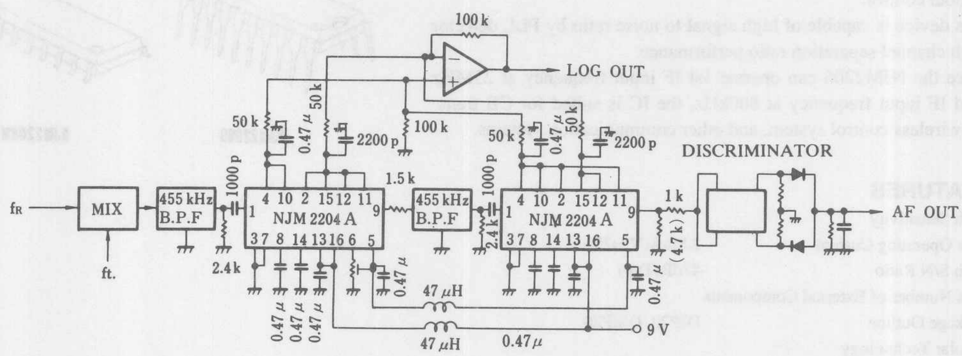


Log Detector Output V_R

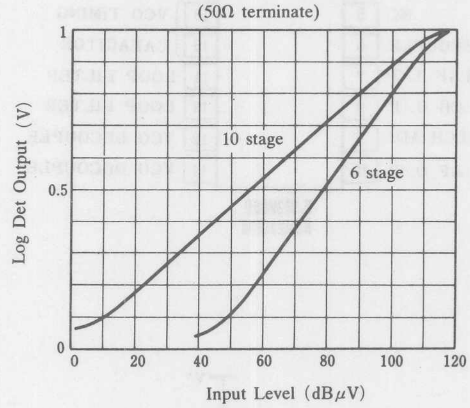
(f_{in}=455kHz, Ta=25°C, 50Ω Terminal)



■ **TYPICAL APPLICATION & CHARACTERISTICS** (10 synthesized stage)



Log Det Output Voltage



LOW POWER IF/AF PLL CIRCUIT FOR NARROW BAND FM RECEIVER

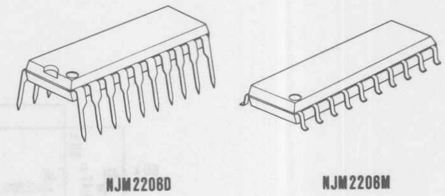
■ GENERAL DESCRIPTION

The NJM2206 is a low power IF/AF PLL circuit for narrowband FM receiver with single or double balanced mixer-IF amplifier and detector. Its low power characteristic is capable for battery operation and remote control.

This device is capable of high signal to noise ratio by PLL detector and high channel separation ratio performance.

Since the NJM2206 can operate 1st IF input frequency at 25MHz and 2nd IF input frequency at 800kHz, the IC is suited for CB transceiver, wireless control system, and other communication systems.

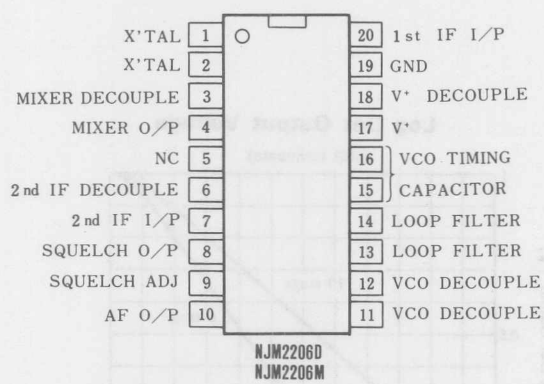
■ PACKAGE OUTLINE



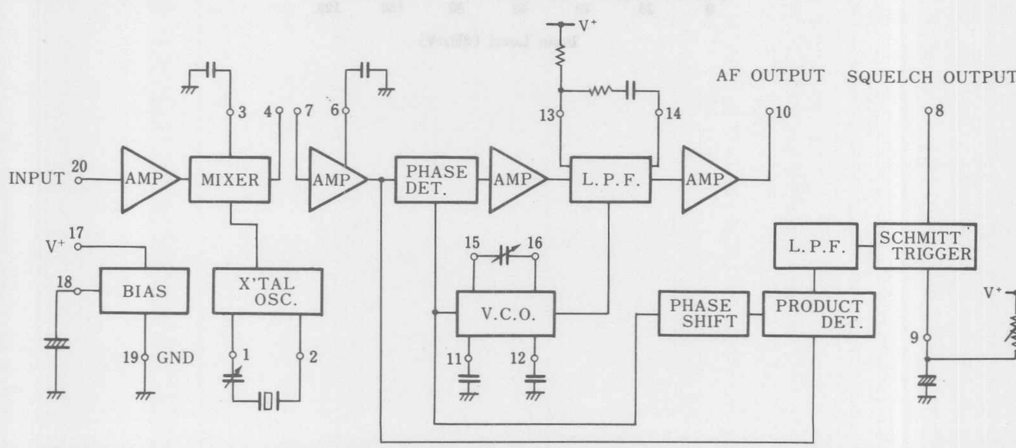
■ FEATURES

- High Sensitivity
- Low Operating Current 2.8mA(V^+=7V)
- High S/N Ratio 47dB(Typ)
- Less Number of External Components
- Package Outline DIP20, DMP20
- Bipolar Technology

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	10	V
Power Dissipation	P_D	(DIP20) 700	mW
		(DMP20) 350	mW
Operating Temperature Range	T_{opr}	−20～75	℃
Storage Temperature Range	T_{stg}	−40～125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V^+=7V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}		—	2.8	3.8	mA
1st IF Frequency Bandwidth	f_{B1}		—	25	—	MHz
1st IF Amp. Gain	G_{V1}		—	20	—	dB
Mixer Conversion Gain	g_{VM}		—	15	—	dB
2nd IF Amp. Gain	G_{VM}		—	60	—	dB
Input Singal Dynamic Range	V_{IDR}	for AF Output 1dB deviation	—	100	—	dB
Maximum Input Level	V_{IMAX}		0.2	—	—	Vrms
Input Sensitivity	S/N 1	At Input Level 10μVrms	20	—	—	dB
Signal to Noise Ratio	S/N 2	Input Level 1mVrms	40	45	—	dB
Total Harmonic Distortion	THD	Input Level 1mVrms	—	—	3	%
AF Output Level	V_O	Input Level 1mVrms	24	30	36	mVrms
AM Suppression Ratio	SUP_{AM}	for 30% AM at Input Level 100μVrms	—	30	—	dB
Squelch Low Level	V_{SL}	10μVrms Input	—	0.1	1.0	V
Squelch High Level	V_{SH}	0.5μVrms	5.0	6.4	—	V

The test conditions are as designated below, unless otherwise specified.

1st IF: 20.8MHz, 2nd IF: 455kHz, Modulation frequency: 1kHz
Frequency deviation: 3.5kHz
Test circuit diagram: See attached figure.
Ideal jigs shall be used.

■ DESCRIPTION OF OPERATION

[1] IF AMP, MIXER, and LOCAL OSC

(1) 1st IF Amp

Pin (20) is the signal input terminal. The 1st IF amplifier has the frequency characteristic shown in Graph 1 and the I/O characteristic shown in Graph 2. Also, Graph 3 shows the input impedance-to-frequency characteristic, while Graph 4 shows the input level-to S/N characteristic.

(2) Local OSC

This local OSC is composed by connecting a crystal oscillator and series capacitor across pins (1) and (2). The series capacitor is connected for finely adjusting the oscillation frequency and reducing the temperature drift.

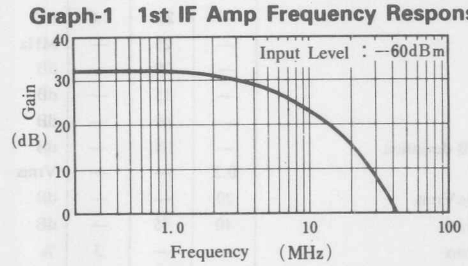
Graph 5 shows the oscillation frequency-to-power voltage and the oscillation level-to-power characteristic.

Graph 6 also shows a change of the oscillation frequency to the capacitance of the capacitor connected in series. For details, please contact the crystal oscillator maker.

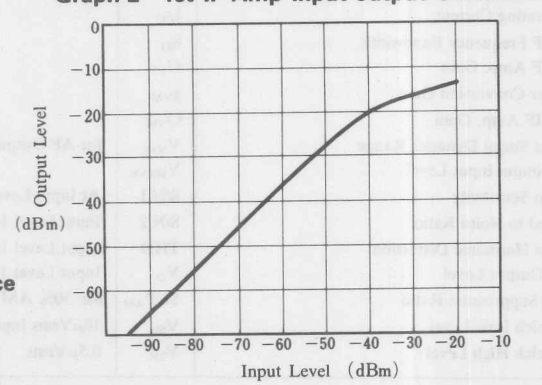
(3) Mixer

The mixer circuit produces the 2nd IF frequency by mixing the 1st IF Amp output and local OSC output signal with each other. A decoupling capacitor is connected to pin (3).

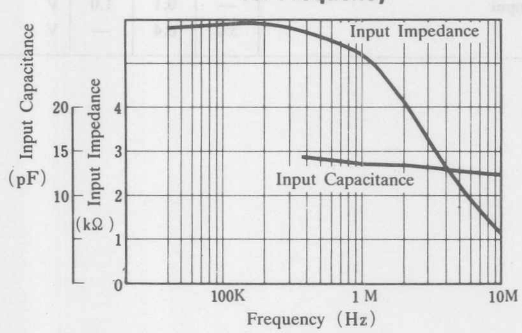
Graph-1 1st IF Amp Frequency Response



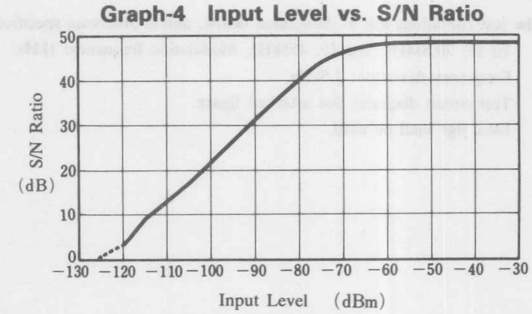
Graph-2 1st IF Amp Input-output Character



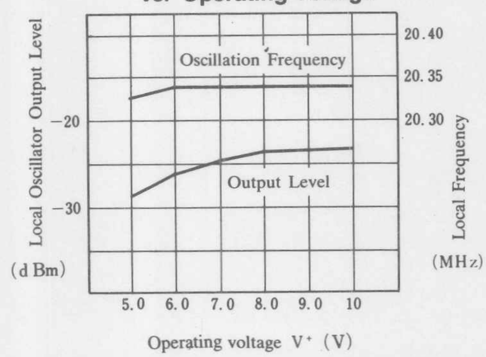
Graph-3 Input Impecance/Capacitance vs. Frequency



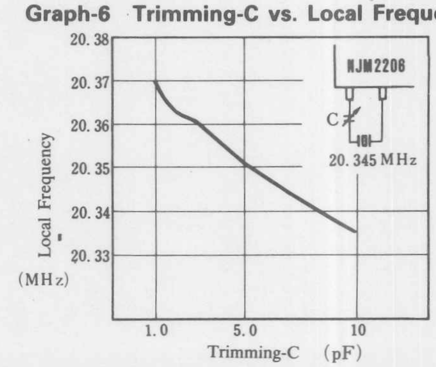
Graph-4 Input Level vs. S/N Ratio



Graph-5 Local Oscillator Output Level/Freq. vs. Operating Voltage



Graph-6 Trimming-C vs. Local Frequency



Note) It is depending on the crystal oscillator.

(4) Pin (4)–GND Capacitor

The capacitor to be connected across pin (4) and GND composes a low-pass filter as shown in Fig. 1.

The cutoff frequency $f_c = 1/2\pi CR$

This cutoff frequency f_c is set to be more than two times the 2nd IF frequency. This C is about 80pF maximum, and it can suppress higher harmonics components without affecting the 455kHz output.

This behaviour is shown in Graph 7.

(5) The capacitor across pins (4) and (7) serves as the coupling capacitor for the mix out and 2nd IF Amp stage. A ceramic filter is insertable instead of the coupling capacitor.

(6) The S/N ratio is changed by the capacitor across pin (6) and GND when the input level is low as shown in Graph 8. this is because the capacitor across pin (6) and GND serves as the decoupling capacitor in the 2nd IF Amp stage, so that the 2nd IF Amp gain is reduced when this capacitance of the capacitor decreases.

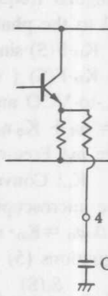
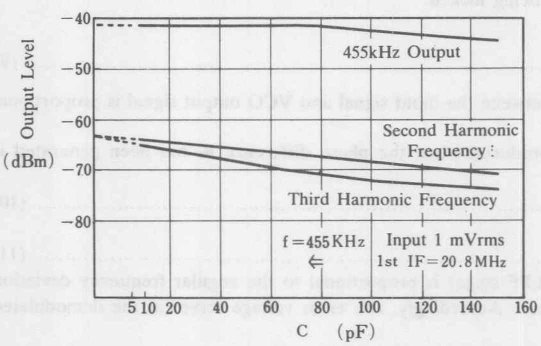
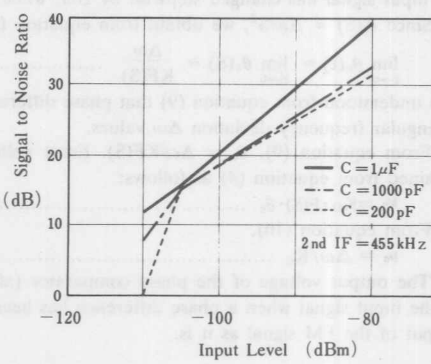


Fig. 1

Graph-7 Pin (4) Low-pass Filter C Value-higher Harmonics component



Graph-8 Change of Input Sensitivity by Pin (6) Decoupling Capacitor



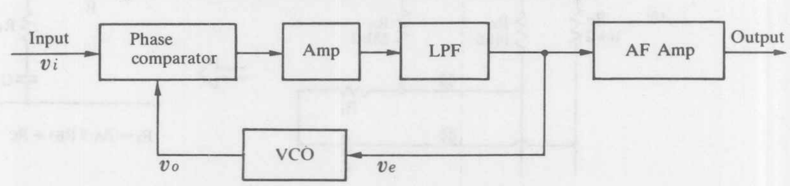
[2] Operation Principle of PLL Demodulation

(1) Operation principle of NJM2206 FM demodulator circuit

When FM is locked at the center frequency, the oscillation frequency of VCO follows frequency change of the FM input VCO oscillation frequency to the input signal frequency and, the control voltage becomes the demodulated output. VCOoscillation frequency to the input signal frequency and, the control voltage becomes the demodulated output.

The FM demodulation circuit of NJM2206 is constructed as shown in BLOCK DIAGRAM 2.

Fig. 2 PLL Demodulation Circuit Block Diagram



Assume v_i be the input signal voltage and v_o be the VCO signal voltage in Fig. 2.

$v_i = V_i \sin\{\omega_i t + \theta_i(t)\}$ .... (1)

$v_o = V_o \cos\{\omega_o t + \theta_o(t)\}$ .... (2)

From equations (1) and (2), signal voltage v_e after eliminating high-frequency components via the LPF is obtained by equation (3).

$v_e = K_D \cdot F(S) \cdot \sin\{(\omega_i - \omega_o)t + \theta_i(t) - \theta_o(t)\}$ .... (3)

Where F(S): Transfer function of LPF

K_D: Conversion gain of phase comparator

When the angular frequency of the input signal coincides with the angular frequency of the output signal, error voltage ν_e proportional to the phase differences is obtained as shown in equation (4).

$$\nu_e = K_D \cdot F(S) \cdot \sin\{\theta_i(t) - \theta_o(t)\}$$
$$\approx K_D \cdot F(S)\{\theta_i(t) - \theta_o(t)\} \quad \cdots\cdots (4)$$

Also, the ν_e-to-VCO angular frequency ω_o relation is represented by equation (5).

$$\omega_o = \omega_f + K_o \nu_e \quad \cdots\cdots (5)$$

where ω_f: Free-running angular frequency of VCO

K_o: Conversion gain of VCO

Since the microscopic change of the phase angle with time is given by the angular frequency change component $\Delta\omega_o$ we obtain; $\Delta\omega_o = K_o \cdot \nu_e = d\theta_o(t)/dt$ ……(6)

From equations (5) and (6), we obtain the PLL transfer function as shown in equation (7)

$$H(S) = \frac{\theta_o(S)}{\theta_i(S)} = \frac{KF(S)}{S+KF(S)} \quad \cdots\cdots (7)$$

where $K = K_o \cdot K_D$: Loop gain coefficient

Assume that $\theta_e(S) = \theta_i(S) - \theta_o(S)$, and we obtain equation (8) from equation (7);

$$\frac{\theta_e(S)}{\theta_i(S)} = \frac{S}{S+KF(S)} \quad \cdots\cdots (8)$$

Let's consider about the phase difference of the input signal and VCO output signal when the angular frequency of the input signal has changed stepwise by $\Delta\omega$, while PLL is being locked.

Since $\theta_i(S) = \Delta\omega/S^2$, we obtain from equation (8)

$$\lim_{t\to\infty} \theta_e(t) = \lim_{S\to 0} \theta_e(S) = \frac{\Delta\omega}{KF(S)} \quad \cdots\cdots (9)$$

It is understood from equation (9) that phase difference θ_e between the input signal and VCO output signal is proportional to angular frequency deviation $\Delta\omega$ values.

From equation (9), $\theta_e = \Delta\omega/KF(S)$. Error voltage ν_e produced when the phase difference θ_e has been generated is obtained from equation (4) as follows;

$$\nu_e = K_D \cdot F(S) \cdot \theta_e \quad \cdots\cdots (10)$$

From equation (10),

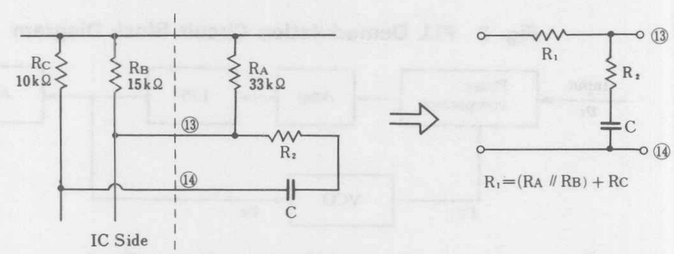
$$\nu_e = \Delta\omega/K_o \quad \cdots\cdots (11)$$

The output voltage of the phase comparator (after the LPF stage) is proportional to the angular frequency deviation of the input signal when a phase difference has been produced. Accordingly, this error voltage serves as the demodulated output of the FM signal as it is.

References: "Phase lock techniques" Floyed M Gardner
"Basis and application of PLL", Hideo Kadota

(2) Low-pass filter (LPF)

The LPF of NJM2206 is shown in Fig. 3.



$$\text{Transfer Function } F(S) = \frac{S\tau_2 + 1}{S(\tau_1 + \tau_2) + 1} \qquad \tau_1 = CR_1, \quad \tau_2 = CR_2$$

Fig. 3 NJM2206 LPF

The loop band is determined by this LPF, and it affects the maximum phase deviation capture range, maximum frequency response characteristic, or noise bandwidth. The PLL transfer function is obtained when the LPF shown in Fig. 2 is used.

$$H(S) = -\frac{S\omega_n\left(2\xi - \frac{\omega_n}{K}\right) + \omega_n}{S^2 + 2\xi\,\omega_n S + \omega_n}$$

$$\omega_n = \left(\frac{K}{\tau_1 + \tau_2}\right)^{1/2}\text{: Natural angular frequency}$$

$$\xi = \frac{1}{2}\left(\frac{K}{\tau_1 + \tau_2}\right)^{1/2}\left(\tau_2 + \frac{1}{K}\right)\text{: Dumping factor}$$

When $K \gg 1$, $\xi = \frac{1}{2}\omega_n \tau_2$

This filter is characterized that since the loop gain, and damping factor are adjustable separately, the narrow band is obtainable with high stability of PLL.

Exmaple of calculation of LPF constants

$K_o = 0.5f_o$: Conversion gain of VCO, f_o: free-running frequency

$K_D = 1.96$: Conversion gain of phase comparator x gain of amplifier

$K_oK_D = 0.98f_o$

$R_1 = 20k\Omega$

The above values are calculated from the design values of the NJM2206 circuit constants.

Assume that the maximum frequency deviation $\Delta f = 3.5kHz$, the modulation signal frequency $f_m = 1kHz$, $f_o = 455kHz$ and the maximum phase error $\phi_{e\,max}$ is obtained by;

$$\phi_{e\,max} = \frac{2\pi}{K_oK_D} \cdot \frac{\Delta f}{f_o} = 0.05$$

Assume that natural angular frequency $f_n = 10kHz$, and we obtain from Fig. 3;

$$\frac{\phi_e}{\frac{\Delta f}{f_n}} = 0.1$$

$$\phi_e = 0.1 \times \frac{\Delta f}{f_n} = 0.035$$

Accordingly, we obtain, assuming that $f_n = 10kHz$;

$$\tau_1 + \tau_2 = \frac{K_oK_Dfo}{(2\pi fn)^2} = 113\mu S$$

Damping factor $\xi = 0.707$,

$$\tau_2 = \frac{2\xi}{2\pi fn} = 22\mu S$$

$$\therefore \tau_1 = 91\mu S$$

From these values, we obtain C and R_2 as follows.

$C = \tau_1/R_1 = 4500pF$

$R_2 = \tau_2/C = 4.9k\Omega$

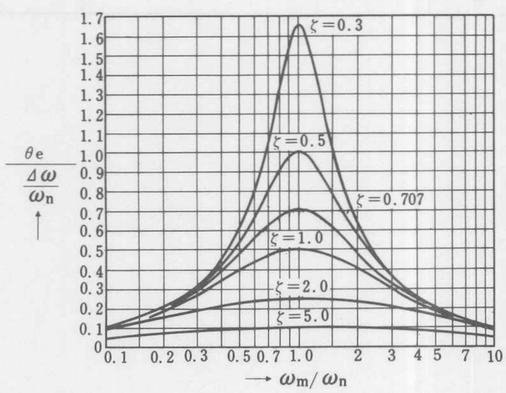


Fig. 4 Steady-state Phase Error by Sine Wave FM

(3) Effect of LPF constants on the detection characteristic of PLL demodulator circuit

Graphs 9, 10 and 11 show the input-to-output characteristic, modulation frequency-to-AF output characteristic, and frequency deviation-to-distortion factor characteristic when LPF constants were changed, respectively. Table 1 shows LPF constants in these cases.

- **Input-to-output characteristic (Graph 9)**

  The noise level from −100dBm to −70dBm is affected by the natural angular frequency and lock range. Since the input level, where the noise level suppression is started, is transient just before the PLL is locked, the noise level is affected by the damping factor and capture range.

- **Modulation frequency-to-AF output characteristic (Graph 10)**

  The band is demodulated from (1) and (2), and determined by the natural angular frequency. If this band is wide, the noise level increases.

- **Frequency deviation-to-distortion factor characteristic (Graph 11)**

  The maximum frequency deviation is determined by the natural angular frequency.

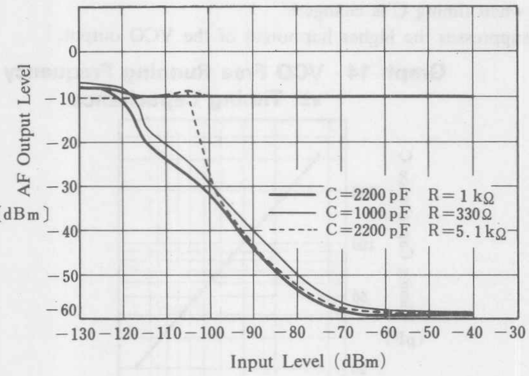
- **LPF constants, the capture range, and lock range (Graph 12)**

  Graph 12 shows the capture range and lock range when LPF constants were changed. From this graph and the input-to-output characteristic shown in Graph 9, it is understood that the noise level is changed by the lock range.

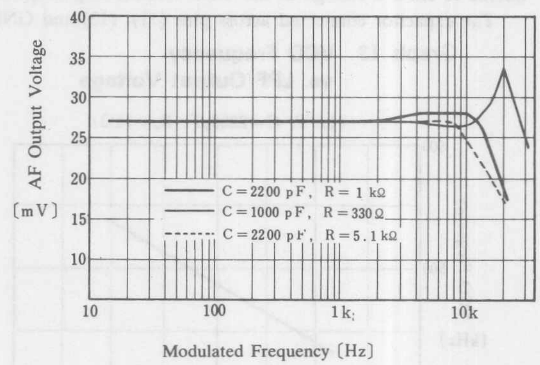
Table-1

①	C=2200pF, R_2=1kΩ	f_n=15.6kHz, ξ=0.1
②	C=1000pF, R_2=330Ω	f_n=23.6kHz, ξ=0.02
③	C=2200pF, R_2=5.1kΩ	f_n=14.3kHz, ξ=0.5

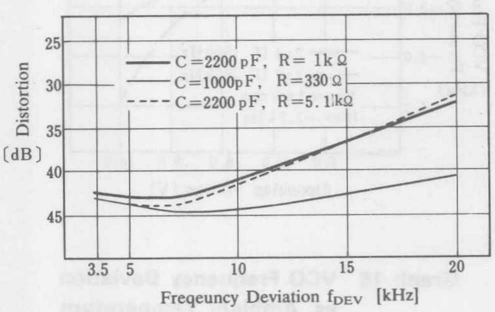
Graph 9 Input-output Characteristic



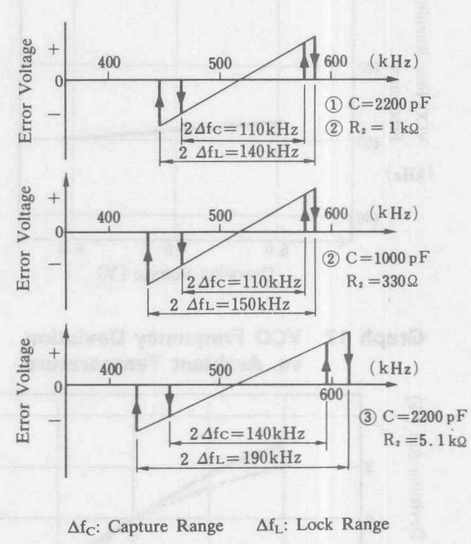
Graph 10 Modulated Frequency vs. A.F. Output Voltage



Graph 11 Frequency Deviation vs. Distortion



Graph 12 LPF Constance, Capture Range, Lock Range



(5) VCO

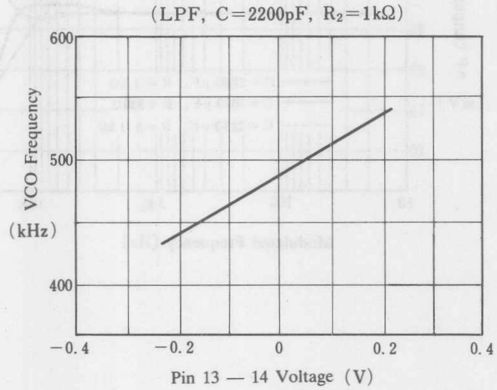
Graph 13 shows the VCO oscillation frequency-to-LPF output voltage characteristic. The LPF output voltage (voltage across pins (13) — (14)) becomes the VCO control voltage.

As shown in Graph 13, this relation is linear, and its gradient is determined by the VCO converstion gain.

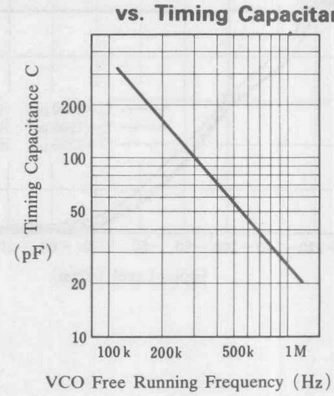
Also, the linearity range is closely related to the lock range. Graph 14 shows the VCO free-running-to-timing C characteristic to show a change of the VCO free-running frequency when timing C is changed.

The capacitor connected across pins (11), (12) and GND suppresses the higher harmonics of the VCO output.

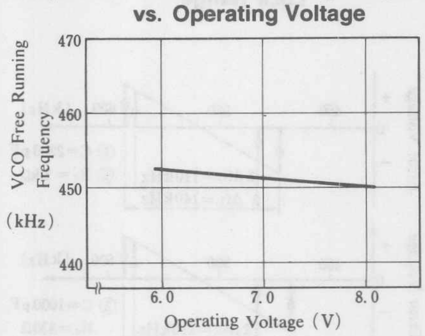
Graph 13 VCO Frequency vs. LPF Output Voltage



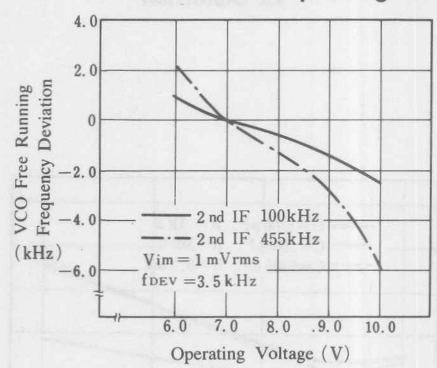
Graph 14 VCO Free Running Frequency vs. Timing Capacitance



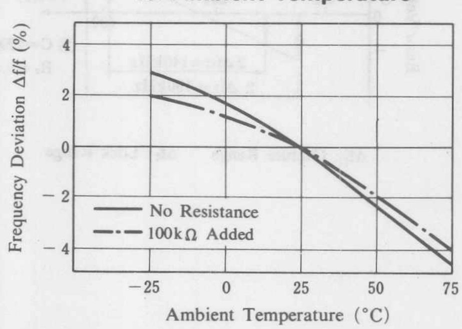
Graph 15 VCO Free Running Frequency vs. Operating Voltage



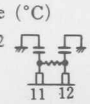
Graph 16 VCO Free Running Frequency Deviation vs. Operating Voltage



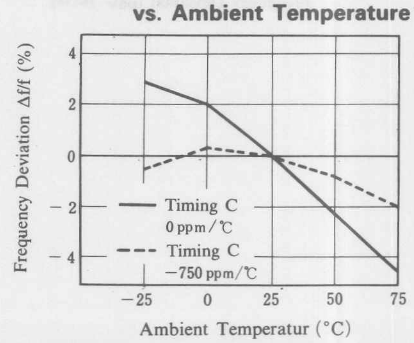
Graph 17 VCO Frequency Deviation vs. Ambient Temperature



Connection Resistance between pin 1 and 12
Use timing Capacitance at 0 ppm/°C



Graph 18 VCO Frequency Deviation vs. Ambient Temperature



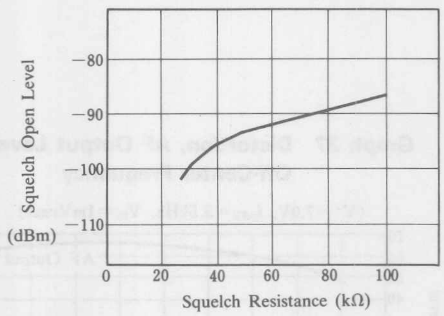
[3] Squelch Circuit Function

The squelch sensitivity is adjustable by the resistance value R connected between pin (9) and V^+. Graph 19 shows the relation between resistance R and squelch release level. As shown in graph 20, the squelch sensitivity corresponding to the S/N ratio required for mute function is adjustable by resistance R. Graph 21 shows the power voltage-to-squelch release level characteristic. Also, the squelch attack time is adjustable by the capacitor connected across pin (9) and GND. This characteristic is obtained by changing the gradient of the squelch level from a high level to a low level by using an external capacitor.

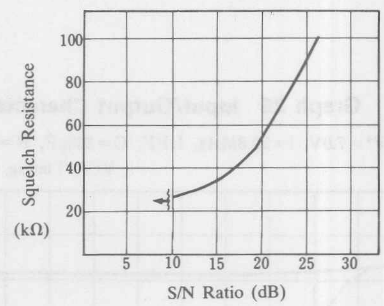
(Note) Squelch release level: Input signal level when the squelch level (pin (8) DC potential) changes from the high level to low level.

The VCO timing C is adjustable by maximizing the DC voltage of pin (9) when an 1mVrms non-modulated signal input is applied.

Graph 19 Squelch Open Level vs. Squelch Resistance

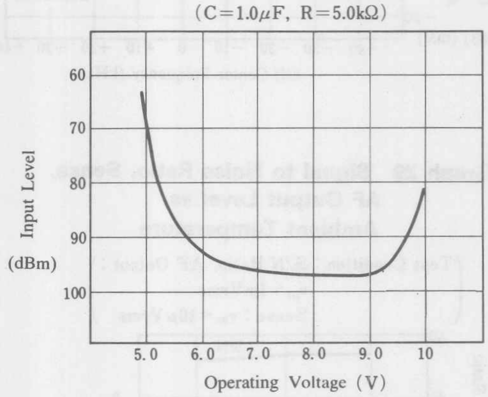


Graph 20 Squelch Sensitivity Characteristics

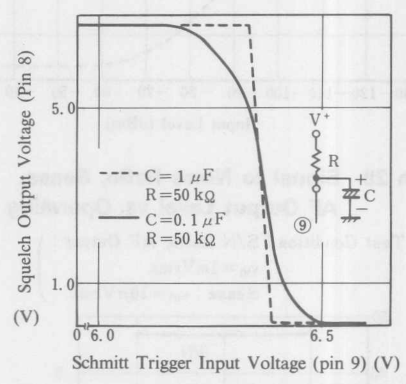


Graph 21 Squelch Open Level vs. Operating Voltage

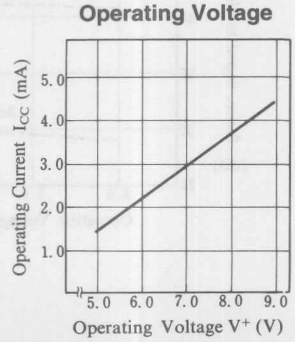
(C=1.0μF, R=5.0kΩ)



Graph 22 Squelch Input/Output Characteristics



Graph 23 Operating Current vs. Operating Voltage



[4] NJM2206 overall characteristics

(1) DC characteristic

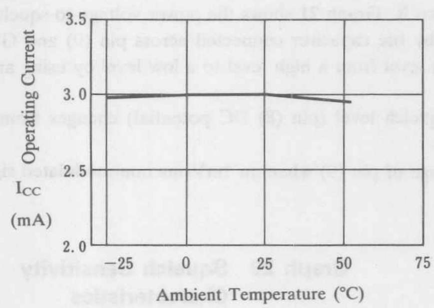
Graph 23 shows the power voltage-to-current consumption characteristic, while graph 24 shows the ambient temperature-to-current consumption characteristic.

(2) AC characteristic

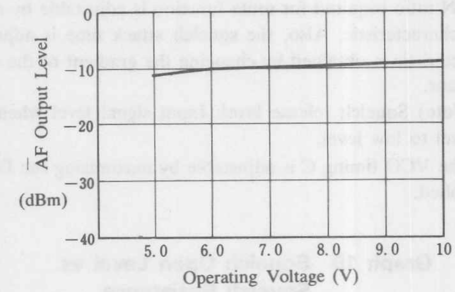
Graph 25 shows the power voltage-to-output level characteristic. As shown from this graph, this IC is characterized with small change of the AF output level against power fluctuations.

Also, the input/output characteristic is shown in graph 26. Graph 28 and 29 show the S/N ratio, sense, and AF output level-to-power voltage characteristic and the S/N ratio, sense, and AF output level-to-ambient temperature characteristic, respectively.

Graph 24 Operating Current vs. Ambient Temperature

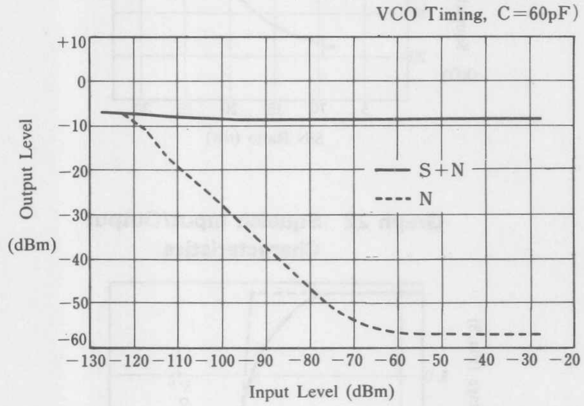


Graph 25 AF Output Level vs. Operating Voltage



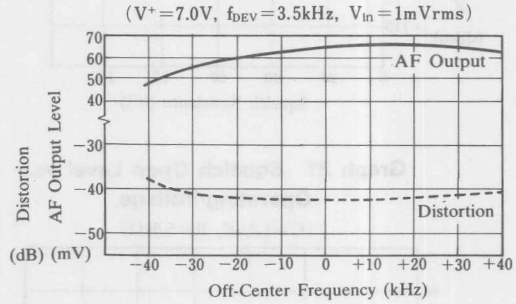
Graph 26 Input/Output Characteristics

(V^+=7.0V, f=20.8MHz, LPF, C=200pF, R=1kΩ, VCO Timing, C=60pF)



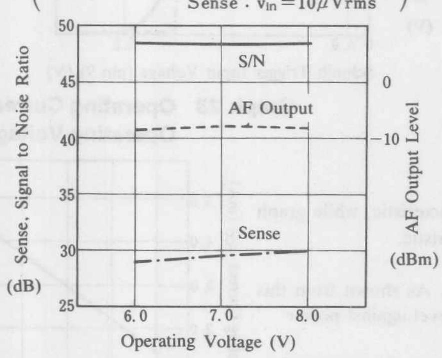
Graph 27 Distortion, AF Output Level vs. Off-Center Frequency

(V^+=7.0V, f_{DEV}=3.5kHz, V_{in}=1mVrms)



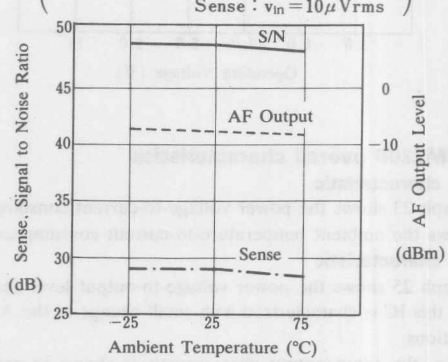
Graph 28 Signal to Noise Ratio, Sense, AF Output Level vs. Operating Voltage

(Test Condition : S/N Ratio, AF Output : v_{in}=1mVrms
Sense : v_{in}=10μVrms)

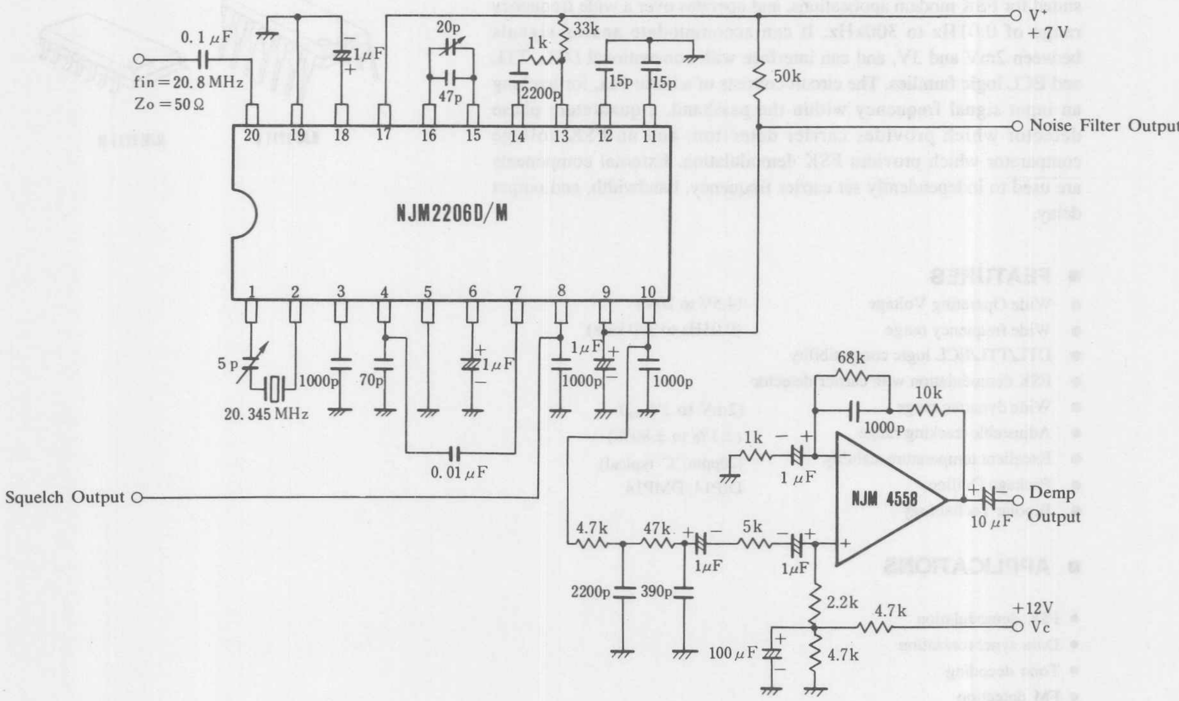


Graph 29 Signal to Noise Ratio, Sense, AF Output Level vs. Ambient Temperature

(Test Condition : S/N Ratio, AF Output : v_{in}=1mVrms
Sense : v_{in}=10μVrms)



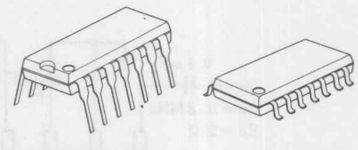
■ TEST CIRCUIT



■ GENERAL DESCRIPTION

The NJM2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications, and operates over a wide frequency range of 0.01Hz to 300kHz. It can accommodate analog signals between 2mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal frequency within the passband, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set carrier frequency, bandwidth, and output delay.

■ PACKAGE OUTLINE



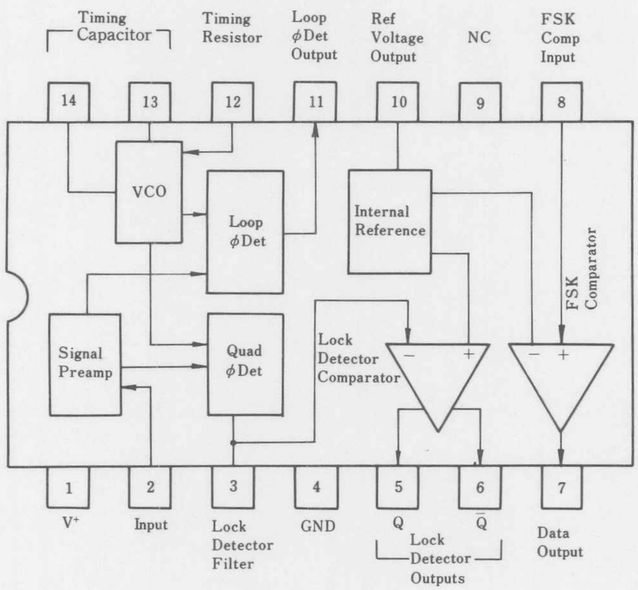
■ FEATURES

- Wide Operating Voltage (4.5V to 20V)
- Wide frequency range (0.01Hz to 300 kHz)
- DTL/TTL/ECL logic compatibility
- FSK demodulation with carrier-detector
- Wide dynamic range (2mV to $3V_{rms}$)
- Adjustable tracking range (±1% to ±80%)
- Excellent temperature stability (20ppm/°C typical)
- Package Outline DIP14, DMP14
- Bipolar Technology

■ APPLICATIONS

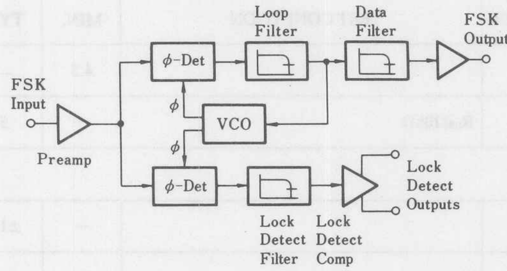
- FSK demodulation
- Data synchronization
- Tone decoding
- FM detection
- Carrier detection

■ PIN CONFIGURATION



NJM2211D
NJM2211M

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	20	V
Input Signal Level	V_{IN}	3	V_{rms}
Power Dissipation	P_D	(DIP14) 700	mW
		(DMP14) 300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

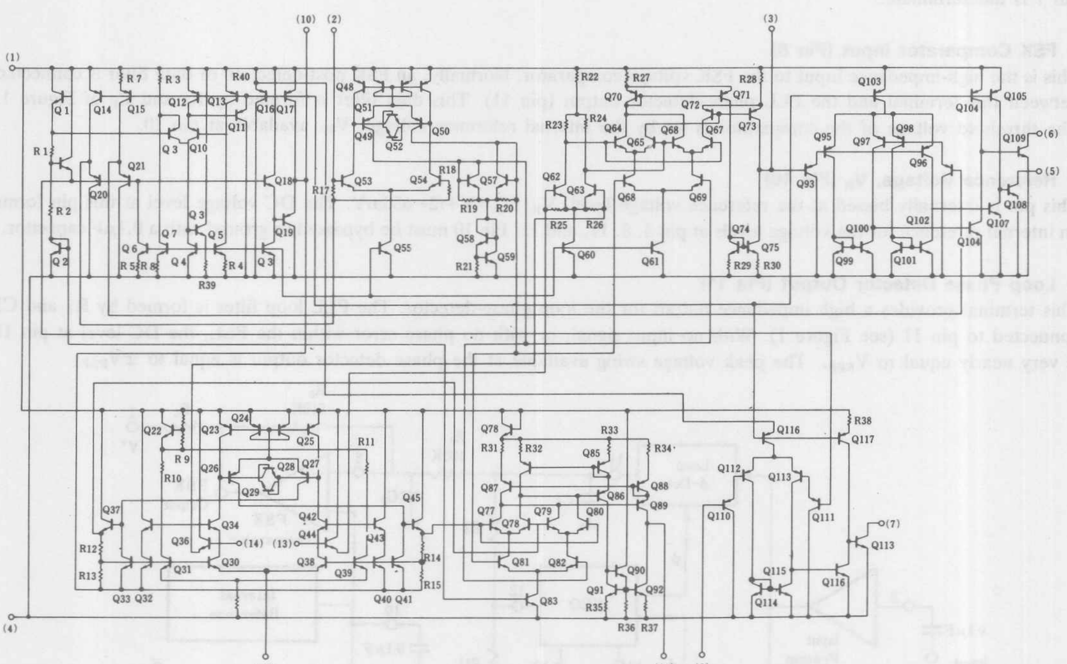
■ ELECTRICAL CHARACTERISTICS

($V^+=+12V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		4.5	—	20	V
Operating Current	I_{CC}	$R_0 \geqq 10k\Omega$	—	5	11	mA
Oscillator						
Frequency Accuracy	Δf_0		—	±1.0	—	%
Frequency Stability Temp. Coefficient	$\Delta f_0/\Delta T$	$R_1=\infty$	—	±20	—	ppm/℃
Power Supply Rejection	PSRR	$V^+=12\pm1V$ $V^+=5\pm0.5V$	—	±0.05 ±0.2	±1.5	%/V %/V
Upper Frequency Limit	$f_{0\,MAX}$	$R_0=8.2k\Omega$, $C_0=400pF$	—	300	—	kHz
Lowest Operating Frequency	$f_{0\,MIN}$	$R_0=2M\Omega$, $C_0=50\mu F$	—	0.01	—	Hz
Timing Resistor						
Timing Resistor	R_0	Operating Range	5	—	2000	kΩ
		Recommended Range	15	—	100	kΩ
Loop Phase Detector						
Peak Output Current	I_0	Meas. at pin 11	±100	±200	±300	μA
Output Offset Current	I_{OS}		—	±2.0	—	μA
Output Impedance	Z_0		—	1.0	—	MΩ
Maximum Voltage Swing	V_{OM}	Ref. to pin 10	±4.0	±5.0	—	V
Quadrature Phase Detector						
Peak Output Current	I_0	Meas. at Pin 3	—	150	—	μA
Output Impedance			—	1.0	—	MΩ
Maximum Voltage Swing			—	11	—	V_{p-p}
Input Preamp						
Input Impedance	R_{IN}	Meas. at Pin 2	—	20	—	kΩ
Input Signal Voltage Required to Cause Limiting	V_{IN}		—	2	—	mV_{rms}

Voltage Comparator						
Input Impedance	R_{IN}	Measure at Pin 3 & 8	—	2		MΩ
Input Bias Current	I_B			100		nA
Voltage Gain	G_V	R_L=5.1kΩ		70		dB
Output Voltage Low	V_{SAT}	5, 6, 7_{PIN} I_C=3mA	—	0.3	1.0	V
Output Leakage Current	I_{LEAK}	V_0=12V	—	0.01	11	μA
Internal Reference						
Output Voltage	V_{REF}	Measure at Pin 10	4.75	5.30	5.85	V
Output Impedance	Z_0		—	100	—	Ω

■ EQUIVALENT CIRCUIT



■ CIRCUIT FUNCTION

• Singal Input (Pin 2)

The input signal is AC coupled to this terminal. The internal impedance at pin 2 is 20kΩ. Recommended input signal leveles in the range of $10mV_{rms}$ to $3V_{rms}$.

• Quadrature Phase Detector Output (Pin 3)

This is the high-impedance output of the quadrature phase detector, and is internally connected to the input of lock-detect voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 1) to eliminate chatter at the lock-detect outputs. If this tone-detect section is not used, pin 3 can be left open circuited.

• Lock-Detect Output, Q (Pin 5)

The output at pin 5 is at a "high" state when the PLL is out of lock and goes to a "low" or conducting state when the PLL is locked. It is an open collector type output and required a pull-up resistor, R_L, to V^+ for proper operation. In the "low" state it can sink up to 5mA of load current.

• Lock-Detect Complement, Q (Pin 6)

The output at pin 6 is the logic complement of the lock-detect output at pin 5. This output is also an open collector type stage which can sink 5mA of load current in the low or "on" state.

• FSK Data Output (Pin 7)

This output is an open collector logic stage which requres a pull-up resistor, R_L, to V^+ for proper operation. It can sink 5mA of load current. When decoding FSK signals the FSK data output will switch to a "high" or off state for low input frequency, and will switch to a "low" or on state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

• FSK Comparator Input (Pin 8)

This is the high-impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase-detector output (pin 11). This data filter is formed by R_F and C_F of Figure 1. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at pin 10.

• Reference Voltage, V_R (Pin 10)

This pin is internally biased at the reference voltage level, V_R; $V_R=V+/2-650mV$. The DC voltage level at this pin forms an internal reference for the voltage levels at pin 3, 8, 11, and 12. Pin 10 must be bypassed to ground with a $0.1\mu F$ capacitor.

• Loop Phase Detector Output (Pin 11)

This terminal provides a high impedance output for the loop phase-detector. The PLL loop filter is formed by R1 and C1 connected to pin 11 (see Figure 1). With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_{REF}. The peak voltage swing available at the phase detector output is equal to $\pm V_{REF}$.

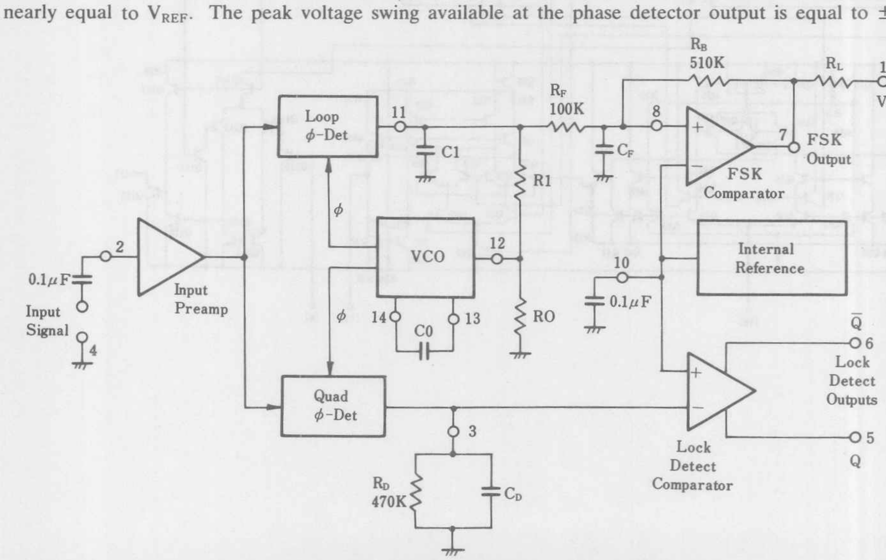


Figure 1 FSK & Tone Detection

- **VCO Control Input (Pin 12)**

VCO free-running frequency is determined by external timing resistor, R0, connected from this terminal to ground. The VCO free-running frequency, f_0, is given by:

$$f_0(\mathrm{Hz}) = \frac{1}{R0C0}$$

where C0 is the timing capacitor across pins 13 and 14. For optimum temperature stability R0 must be in the range of 10kΩ to 100kΩ (see Typical Electrical Characteristics).
This terminal is a low impedance point, and is internally biased at a DC level equal to V_R. The maximum timing current drawn from pin 12 must be limited to ≦3mA for proper operation of the circuit.

- **VCO Timing Capacitor (Pins 13 and 14)**

VCO frequency is inversely proportional to the external timing capacitor, C0, connected across these terminals. C0 must be non-polarized, and in the range of 200pF to 10μF.

- **VCO Frequncy Adjustment**

VCO can be fine tuned by connecting a potentiometer, R_X, in series with R0 at pin 12 (see Figure 2)

- **VCO Free-Running Frequency, F_0**

The NJM2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase-detector sections of the circuit. However, for setup or adjustment purposes, the VCO free-running frequency can be measured at pin 3 (with C_D disconnected) with no input and also pin 2 shorted to pin 10.

■ DESIGN EQUATIONS

See Figure 1 for Definitions of Components.

1. VCO Center Frequency, f_0:

$$f_0(\mathrm{Hz}) = \frac{1}{R0C0}$$

2. Internal Reference Voltage, V_R (measured at pin 10):

$$V_R = \left(\frac{+V_s}{2}\right) - 650\mathrm{mV}$$

3. Loop Lowpass Filter Time Constant, τ:

$$\tau = R1C1$$

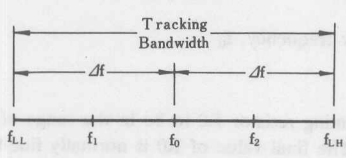
4. Loop Damping, ζ:

$$\zeta = \left(\sqrt{\frac{C0}{C1}}\right)\left(\frac{1}{4}\right)$$

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$:

$$\Delta f/f_0 = R0/R1$$

$\Delta f/f_0 = R0/R1$



6. FSK Date Filter Time Constant, τ_F:

$$\tau_F = R_F C_F$$

7. Loop Phase Detector Conversion Gain, K_ϕ:
(K$_\phi$ is the differential DC voltage across pins 10 and 11, per unit of phase error at phase-detector input):

$$K\phi\ (\text{in volts per radian}) = \frac{(-2)(V_{REF})}{\pi}$$

8. VCO conversion Gain, K0, is the amount of change in VCO frequency per unit of DC voltage change at pin 11:

$$K0\ (\text{in Hertz per volt}) = \frac{-1}{C0R1V_{REF}}$$

9. Total Loop Gain K_T:

$$K_T\ (\text{in radians per second per volt}) = 2\pi K\phi K0 = 4/C0R1$$

10. Peak Phase-Detector Current, I_A:

$$I_A(\mathrm{mA}) = \frac{V_{REF}}{25}$$

■ APPLICATIONS

FSK Decoding

Figure 2 shows the basic circuit connection for FSK decoding. With reference to Figures 1 and 2, the functions of external components are defined as follows: R0 and C0 set the PLL center frequency. R1 sets the system bandwidth, and C1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one pole post-detection filter for the FSK data output. The resistor R_B (=510kΩ) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.
Recommended component values for some of the most commonly used FSK bauds are given in Table 1.

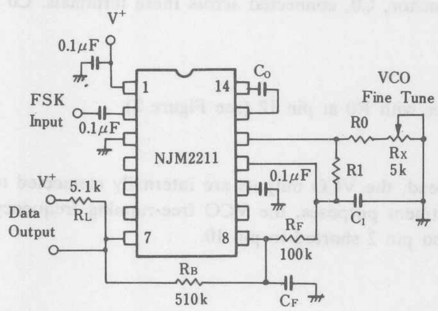


Figure 2 FSK Decoding

Table 1. Recommended Value for FSK

(Ref. Fig. 2)

FSK Band	Component Values
300 Band	C0=0.039μF C_F=0.005μF
F_1=1070Hz	C1=0.01μF R0=18kΩ
f_2=1270Hz	R1=100kΩ
300 Band	C0=0.022μF C_F=0.005μF
f_1=2025Hz	C1=0.0047μF R0=18kΩ
f_2=2225Hz	R1=200kΩ
1200 Band	C0=0.027μF C_F=0.0022μF
f_1=1200Hz	C1=0.01μF R0=18kΩ
f_2=2200Hz	R1=30kΩ

Design Instructions

The circuit of Figure 2 can be tailored for any FSK decoding application by the choice of five key circuit components; R0, R1, C0, C1 and C_F. For a given set of FSK mark and space frequencies, f_1 and f_2, these parameters can be calculated as follows:

1. Calculate PLL center frequency, f_0
   $$f_0 = \frac{f_1 + f_2}{2}$$
2. Choose a value of timing resistor R0 to be in the range of 10kΩ to 100kΩ. This choice is arbitary. The recommended value is R0≅20kΩ. The final value of R0 is normally fine-tuned with the series potentiometer, R_X.
3. Calculate value of C0 from Design Equation No. 1 or from Typical Performance Characteristics:
   $C0 = 1/R0f_0$
4. Calculate R1 to give a Δf equal to the mark-space deviation:
   $R1 = R0[f_0/(f_1 - f_2)]$
5. Calculate C1 to set loop damping. (See Design Equation No. 4.)
   Normally, $\zeta \approx 1/2$ is recommended
   Then: $C1 = C0/4$ for $\zeta = 1/2$
6. Calculate Data Filter Capacitance, C_F:
   For R_F=100kΩ. R_B=510kΩ, the recommended value of C_F is:
   $$C_F(\text{in } \mu F) = \frac{3}{\text{Band Rate}}$$

Note: All calculated component values except R0 can be rounded off to the nearest standard value, and R0 can be varied to fine-tune center frequency through a series potentiometer, R_X (see Figure 2).

Design Example

75 Band FSK demodulator with mark/space frequencies of 1110/1170Hz:

Step 1: Calculate f_0:
$f_0=(1110+1170)(1/2)=1140\text{Hz}$

Step 2: Choose R0=20kΩ (18kΩ fixed resistor in series with 5kΩ potentiometer)

Step 3: Calculate C0 from V_{CO} Frequency vs. Timing Capacitor: $C0=0.044\mu F$

Step 4: Calculate R1: $R1=R0(1140/60)=380k\Omega$

Step 5: Calculate C1: $C1=C0/4=0.011\mu F$

Note: All values except R0 can be rounded off to nearest standard value.

FSK Decoding With Carrier Detect

The lock-detect section of the NJM2211 can be used as a carrier detect option for FSK decoding. The recommended circuit connection for this application is shown in Figure 3. The open-collector lock-detect output, pin 6, is shorted to the data output (pin 7). Thus, the data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL, and the pin 6 output goes "high" to enable the data output.

The Minimum value of the lock-detect filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta f_c$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C1. For most applications, $\Delta f_c<\Delta f/2$. For $R_D=470k\Omega$, the approximate minimum value of C_D can be determined by:

$C_D\ (\mu F)\geqq 16/\text{capture range in Hz}$

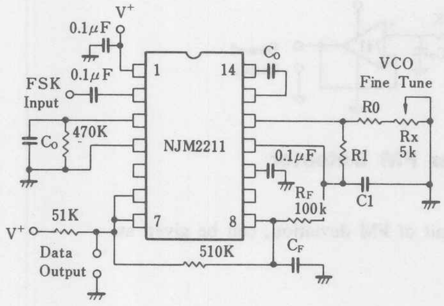
With values of C_D that are too small, chatter can be observed on the lock-detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock-detect output.

Tone Detection

Figure 4 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs becomes reversed for the duration of the input tone. Each logic output can sink 5mA of load current.

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2} as shown in Figure 4.

With reference to Figure 1 and 4, the function of the external circuit components can be explained as follows: R0 and C0 set VCO center frequency, R1 sets the detection bandwidth, C1 sets the lowpass-loop filter time constant and the loop damping factor, and R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.



(Data Output is "low" when no carrier is present)

Figure 3. FSK Demodulation with Carrier Detect Capability

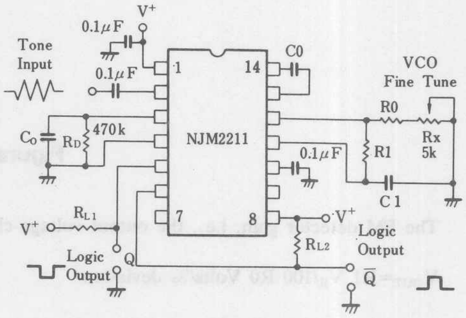


Figure 4. Tone Detection

Design Instructions

The circuit of Figure 4 can be optimized for any tone-detection application by the choice of five key circuit components: R0, R1 C0, C1, and C_D. For a given input tone frequency, f_S, these parameters are calculated as follows:

1. Choose R0 to be in the range of 15kΩ to 100kΩ. This choice is arbitrary.
2. Calculate C0 to set center frequency, f_0 equal to f_S: $C0=1/R0f_S$.
3. Calculate R1 to set bandwidth $\pm\Delta f$ (see Design Equation No. 5): $R1=R0\ (f_0/\Delta f)$

Note: The total detection bandwidth covers the frequency range of $f_0=\Delta f$.

4. Calculate value of C1 for a given loop damping factor:
   $C1=C0/16\zeta^2$
   Normally $\zeta\approx1/2$ is optimum for most tone-detector applications, giving C1=0.25 C0.
   Increasing C1 improves the out-of-band signal rejection, but increases the PLL capture time.
5. Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with R_D=470kΩ, C_D must be:
   $C_D\ (\mu F)\geqslant$ (16/capture range in Hz)
   Increasing C_D slows the logic output response time.

Design Examples

Tone detector with a detection band of 1kHz±20Hz:

Step 1: Choose R0=20kΩ (18kΩ in series with 5kΩ potentiometer).
Step 2: Choose C0 for f_0=1kHz: C0=0.05μF.
Step 3: Calculate R1: R1=(R0) (1000/20)=1MΩ.
Step 4: Calculate C1: for $\zeta=1/2$, C1=0.25μF, C0=0.013μF.
Step 5: Calculate C_D: C_D=16/38=0.42μF.
Step 6: Fine tune the center frequency with the 5kΩ potentiometer, R_X.

Linear FM Detection

The NJM2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for the application is shown in Figure 5. The demodulated output is taken from the loop phase detector output (Pin 11), through a post detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 5.

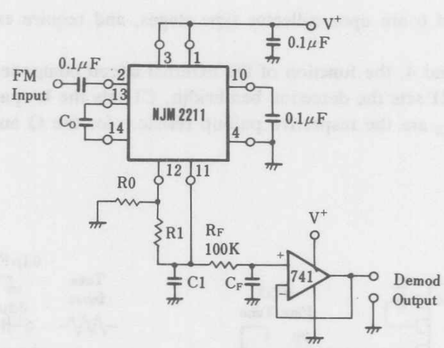


Figure 5. Linear FM Detector

The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

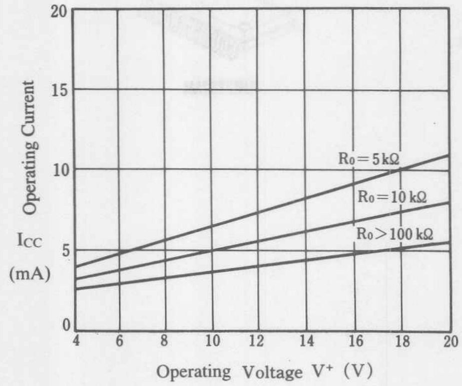
$V_{OUT}=R1\ V_R/100\ R0$ Volts/% deviation

where V_R is the internal reference voltage. For the choice of external components R1, R0, C_D, C1 and C_F, see the section on Design Equations.

■ TYPICAL CHARACTERISTICS

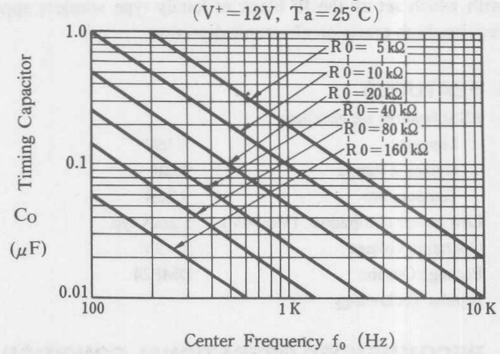
Operating Current

(Ta=25°C)



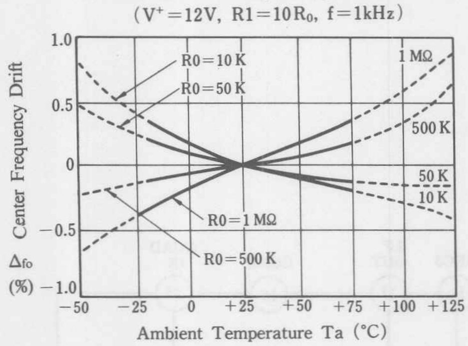
VCO Frequensy

(V+=12V, Ta=25°C)



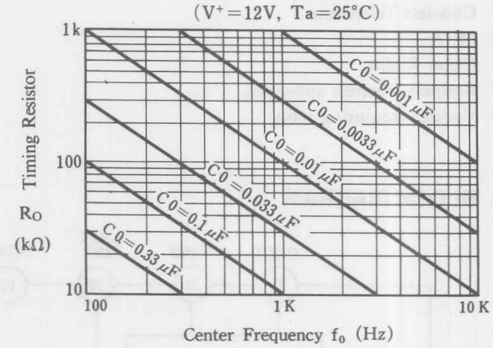
Center Frequency Drift

(V+=12V, R1=10R0, f=1kHz)



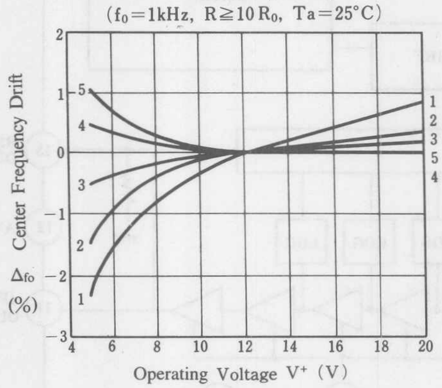
VCO Frequency

(V+=12V, Ta=25°C)



Center Frequency

(f0=1kHz, R≧10R0, Ta=25°C)



Curve	R0
1	5K
2	10K
3	30K
4	100K
5	300K

FM IF WITH LOG AMPLIFIER

■ CONNECTION DIAGRAM

The NJM2232A is high precision FM IF IC with log amplifier, designed to be used for handy type wireless apparatus.

The NJM2232A includes in one chip of IC, at each block, the mixer, local oscillator limitter, log amplifier, FM detector, and so on, with which set up the IF block of handy type wireless apparatus that requires high precision electronic detection.

■ FEATURES

- RSSI features are excellent
  - Linearity ±1dB
  - Dynamic Range 90dB
  - Temperature ±2dB
- Low power dissipation (V_{CC}=6V) 5.2mA typ.
- Operating voltage 5~9V
- Package Outline DMP24
- Bipolar Technology

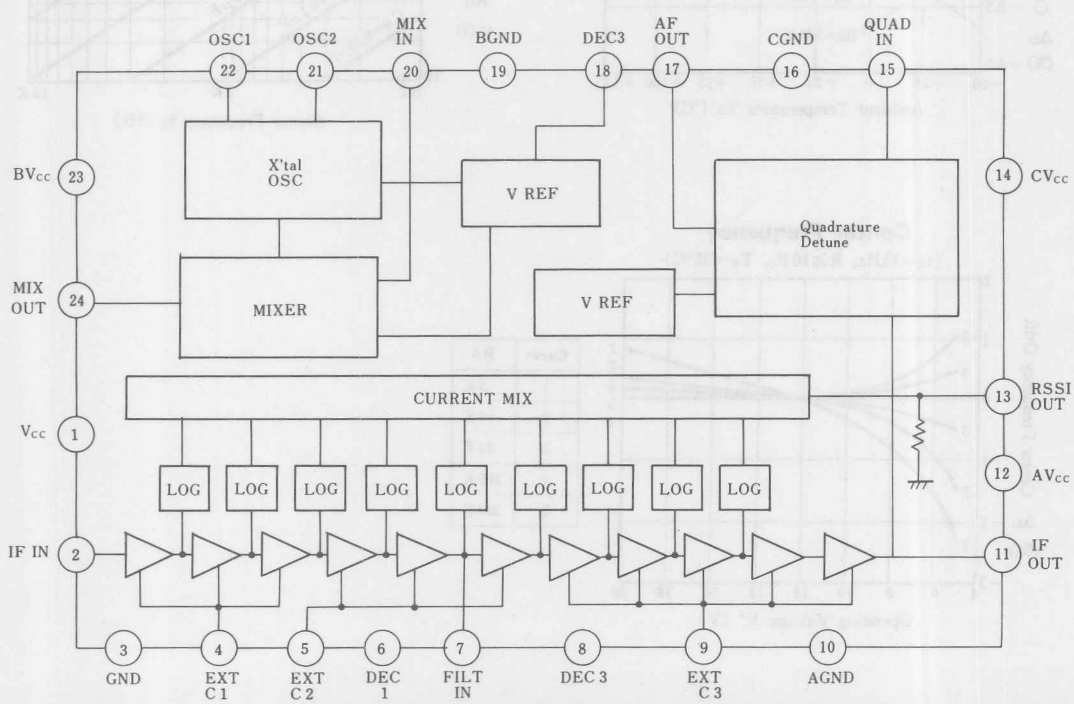
■ RECOMMENDED OPERATIONAL CONDITION

- Operating Voltage V^+ 5.0~9.0V

■ APPLICATION

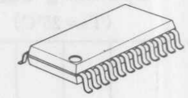
- Automobile telephone
- Codeless Telephone
- MCA
- Celler Radio
- Business Wireless apparatus
- Various measuring units

■ BLOCK DIAGRAM



NJM2232AM

■ PACKAGE OUTLINE



NJM2232AM

■ TERMINAL EXPLANATION

PIN	SYMBOL	Function
1	V_{CC}	Supply Voltage Input of IF-AMP1,RSSI and Reference
2	IF IN	IF-AMP1(Limitter Amp.) Signal Input.
3	GND	Ground of IF-AMP1,RSSI and Reference
4	EXT. C1	Capacitor Connection Terminal1(Limitter Amp. AC Decoupling)
5	EXT. C2	Capacitor Connection Terminal2 (Limitter Amp. AC Decoupling)
6	DEC 1	Reference Decoupling Capacitor1
7	FILT IN	Filter Input between IF-AMP1 and IF-AMP2
8	DEC 2	Reference Decoupling Capacitor2
9	EXT. C3	Capacitor Connection Terminal3 (Limitter Amp. AC Decoupling)
10	AGND	Ground of IF-AMP2 and RSSI
11	IF OUT	IF-AMP2(Limitter Amp.) Signal Output
12	AV_{CC}	Supply Voltage Input of IF-AMP2 and RSSI
13	RSSI	RSSI Input
14	CV_{CC}	FM-DISCRI Supply Voltage Input
15	QUAD IN	Quadrature Detector Input
16	CGND	FM-DISCRI Ground
17	AF OUT	Audio Signal Output
18	DEC 3	Reference Decoupling Capacitor3
19	BGND	Mixer Ground
20	MIX IN	Mixer Signal Input
21	OSC 2	Crystal Oscillator Terminal2
22	OSC 1	Crystal Oscillator Terminal1
23	BV_{CC}	Mixer Supply Voltage Input
24	MIX OUT	Mixer Signal Output

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	12	V
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=6V, Ta=25℃)

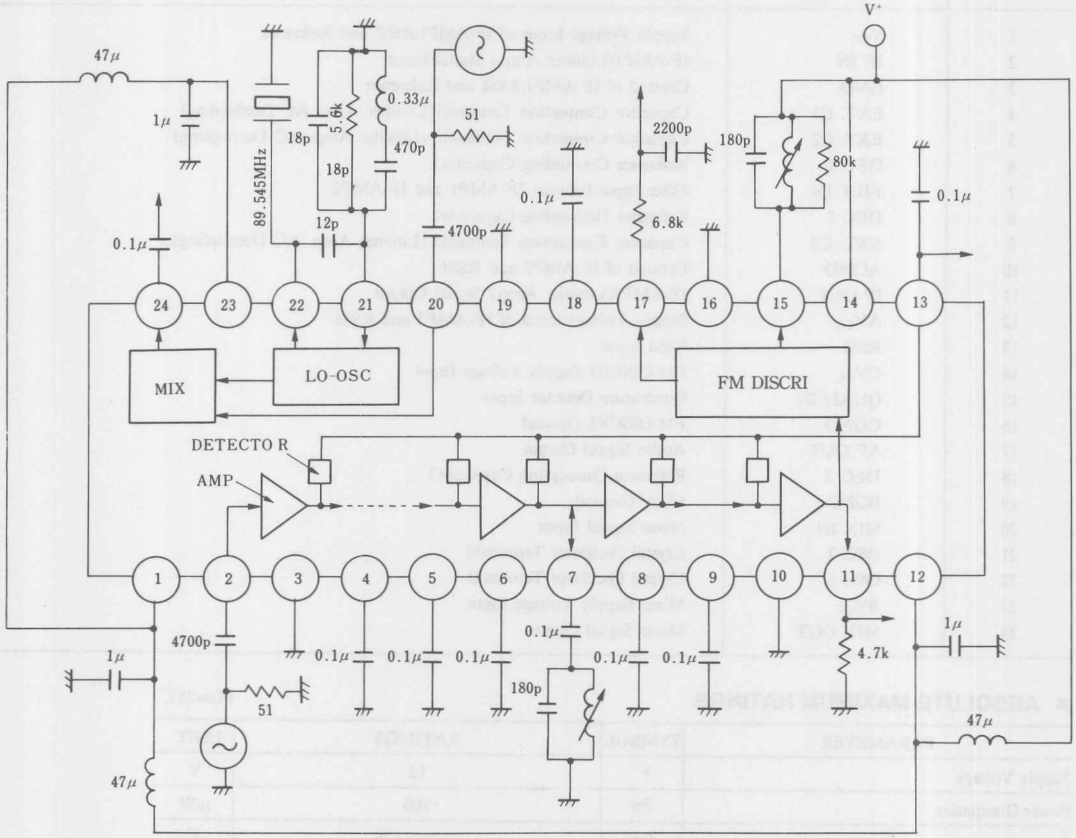
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	11, 21, 22pin, no loading	—	5.2	8.5	mA
Mixer Voltage Gain	G_{MIX}	f_{IN}=90MHz, −40dBm	18	20	22	dB
RSSI Output Voltage (1)	V_{L1}	f_{IN}=455kHz, −90dBm	0.135	—	0.405	V
RSSI Output Voltage (2)	V_{L2}	f_{IN}=455kHz, −80dBm	0.41	—	0.71	V
RSSI Output Voltage (3)	V_{L3}	f_{IN}=455kHz, 0dBm	2.56	—	2.94	V
RSSI Linearity	V_{LIN}	(Note 1)	−1	0	1	dB
RSSI Dynamic Range	DR	(Note 1)	90	—	—	dB
IF Output Voltage	V_{IF}	f_{IN}=455kHz, −50dBm	1.2	1.4	1.6	V
Audio Output Voltage	V_{OUT}	Standard Modulation Signal (Note 2)	150	200	250	mV
Total Harmonic Distortion	THD	Standard Modulation Signal (Note 2)	—	—	1	%
S/N Ratio	S/N	Standard Modulation Signal (Note 2)	40	—	—	dB
AMRR	AMR	Standard Modulation Signal (Note 3)	30	—	—	dB

(Note 1) RSSI Linearity has 10 measuring points (−90,−80~0dBm) from where getting the ideal linearity by way of mini square method, and that each 10 measured spots should stay on within the range of ± 1 dB that can be obtained during the process of the measurement. Also in the process of the measurement, RSSI dynamic range 90 dB can be obtained at the same time.

(Note 2) f_{IN}=455kHz, −20dBm, f_{MOD}=1kHz, f_{DEV}=3kHz

(Note 3) f_{IN}=455kHz, −20dBm, f_{MOD}=1KhZ, AM 30%MOD

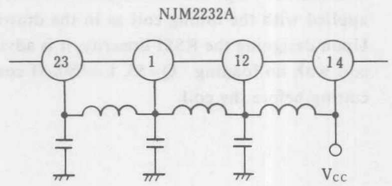
■ TEST CIRCUIT



Adjustable Coil:L-5K4-R(Mitsumi)

■ TERMINAL EXPLANATION

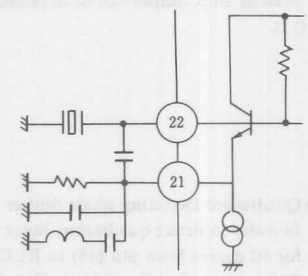
(1) Supply Voltage
The supply voltage is to be delivered at each block, such as limitter Amplifier block ((1), (12) Pin), Mixer block (23) pin , FM Discrimination block (14) pin and so on. When applying the voltage, proceed it supplying from the latter block to front in order of the block structure. When the mixer block and FM block are not required the IC is not operation, no functioning as long as the power supply is off.



⟨Supply Voltage⟩

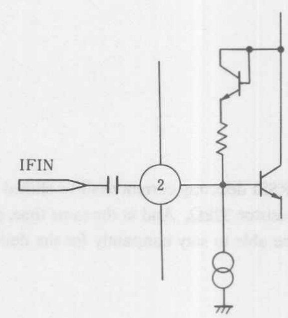
(2) Mixer Input
Mixer input impedance (20) pin is designed to be set at 1.5kΩ (standard) on voltage. It is advisable to input after DC cutting, for desired matched circuit.

(3) Oscillator
As far as the local oscillator input goes, there are 2 methods as shown below.
1. Input after setting the crystal oscillating circuit, on (21), (22) pins.
2. Connect (21) pin directly on supply voltage, and then input the external local oscillator output directly to pin 22.



⟨Oscillator⟩

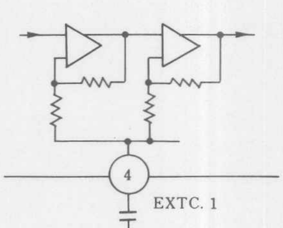
(4) Filter (to be used between Mixer and Limitter Amp.)
Mixer output impedance (24) pin is 2 kΩ (standard), Limitter Amp. Impedance (2) pin is 18kΩ (standard) are desired.
Input harmonizing to the filter to be used for adequate matched circuit.



⟨Limitter Amp. Input⟩

(5) Limitter Amp. Input
Limitter amp. impedance is designed to be 18kΩ (standard). Be sure to input after DC cutting.

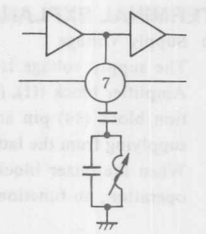
(6) Decoupling Capacitance
(4), (5), (9) pins capacitor are AC decoupling capacitor, Which are set as a part of amplifier feed back circuit of Limitter amp. block. Please apply about 0.1μF capacitance.



⟨Decoupling Capacitor⟩

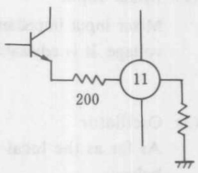
(7) Reference Capacitor
(6), (8), (18) pins capacitor are AC decoupling capacitor which are to be connected to the internal reference. Please apply about 0.1μF capacitance.

(8) Limitter Amp. Inter Section Filter
The limitter amp, the inter section filter is composed of the resonator applied with the tuning coil as in the drawing.
Upon designing the RSSI linearity, it is advisable to apply the resonator coil with no loading Q=55, L=680μH condition, and so proceed DC cutting before the coil.



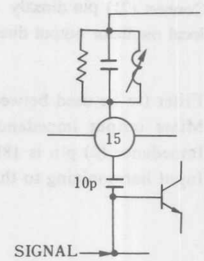
⟨Inter Section Filter⟩

(9) Limitter Amplifier
As shown in the drawing, the limitter amp. is the open emitter, and the limitter amp. output can be obtained by putting adequate resistor to pin (11).



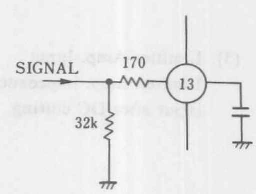
⟨Limitter Amp. Output⟩

(10) Quadrature Detecting phase Shifter
In order to detect quadrature, input the signal that has shifted the phase for 90 degree from pin (15) to RLC paralleled resonator.
The resistor value should be decided to obtain the desired audio output.



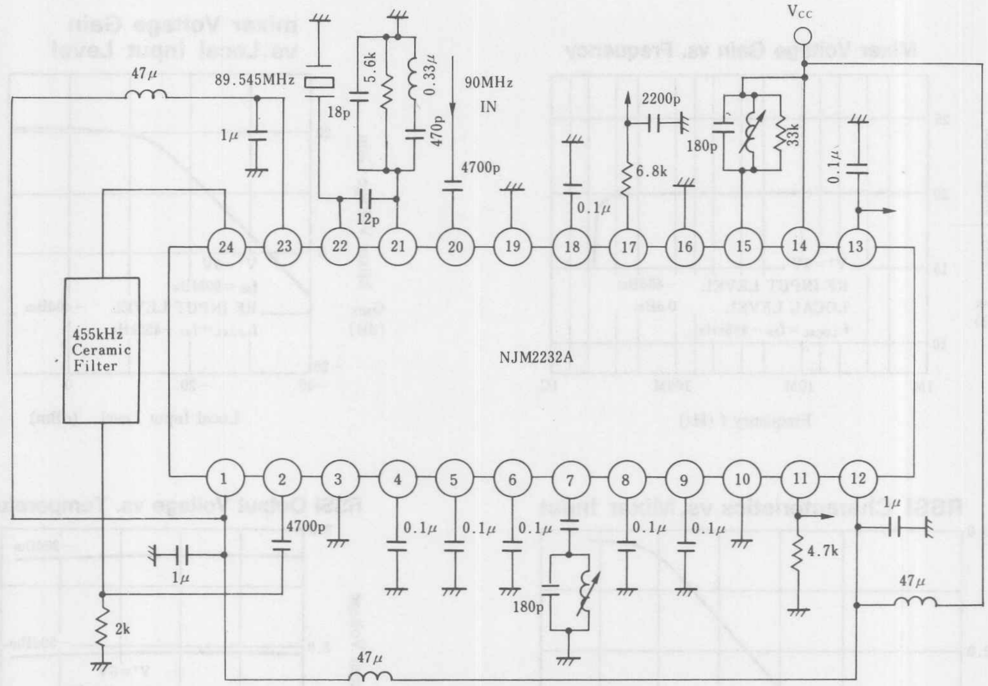
⟨Phase Shifter⟩

(11) RSSI detecting current shall be shifted from current into voltage by the internal resistor 32kΩ, And at the same time, please put the external capacitor value to be able to stay constantly for the desired time.



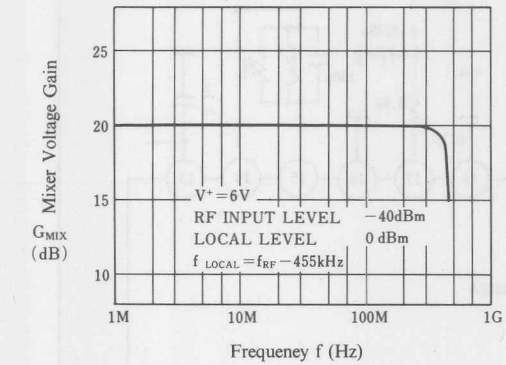
⟨RSSI Output⟩

■ TYPICAL APPLICATION

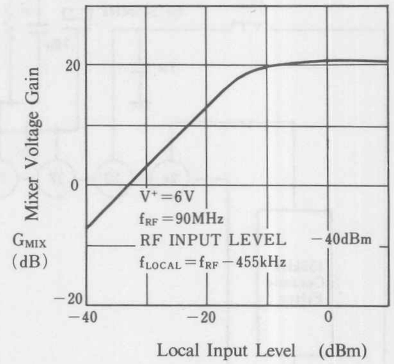


■ TYPICAL CHARACTERISTICS

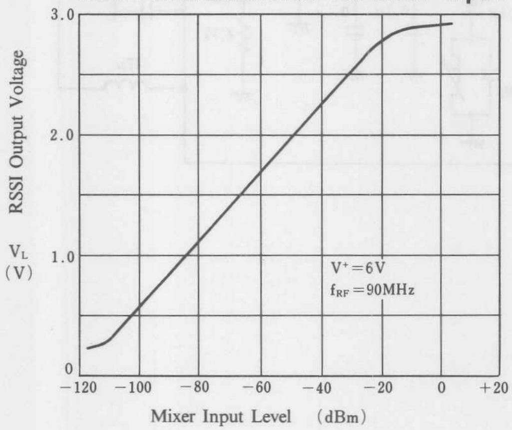
Mixer Voltage Gain vs. Frequency



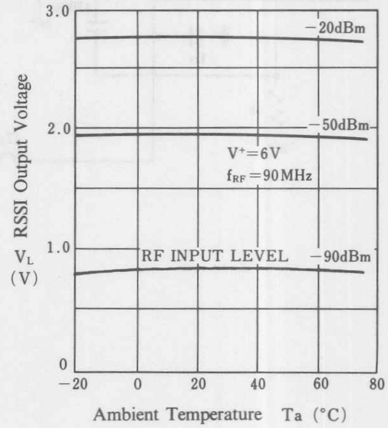
mixer Voltage Gain vs. Local Input Level



RSSI Characteristics vs. Mixer Input



RSSI Output Voltage vs. Temperature

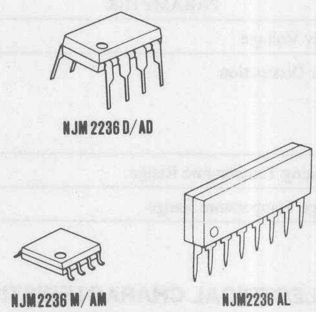


FM FRONT-END

■ GENERAL DESCRIPTION

The NJM2236 is designed for FM front end application, which is suitable to portable radio, radio cassette, clock radio and TV with FM radio. Comparing with conventional types, supply voltage dependence,overload characteristics and spurious radiation characteristics are improved.

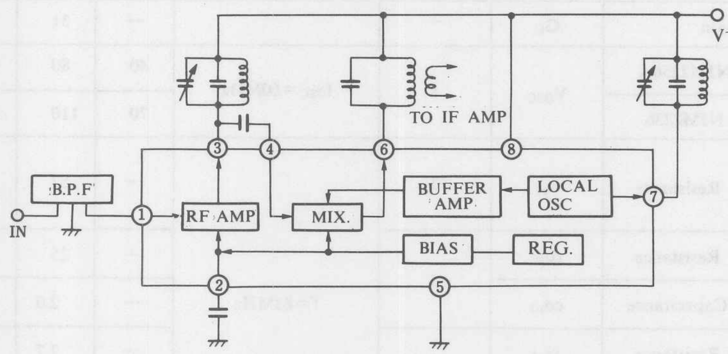
■ PACKAGE OUTLINE



■ FEATURES

- Wide Operating Voltage (1.6～6.0V)
- Excellent Supply Voltage Dependence of Local Oscillator
- Improved Intermoduration Characteristics by Duble Balanced Mixer Circuit
- Low Spurious Radiation
- Build-In Clamping Diode for the Mixer Output
- Local Oscillator Voltage : NJM2236A (Typ.80mV)
  : NJM2236 (Typ.110mV)
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

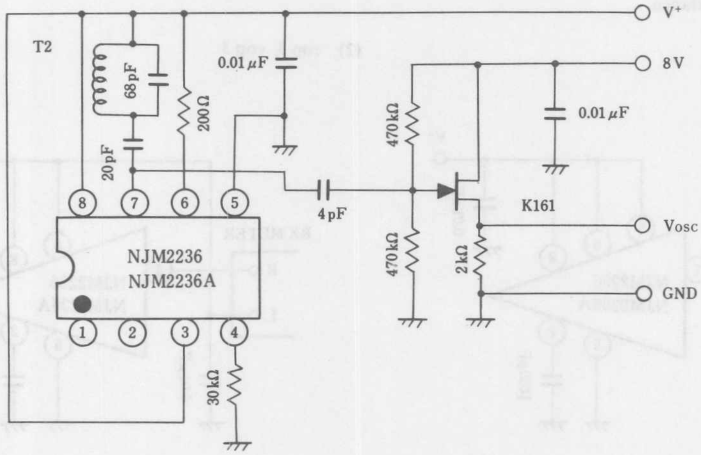
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
		(DIP8) 800	mW
Operating Temperature Range	T_{opr}	−20~75	℃
Storage Temperature Range	T_{stg}	−40~125	℃

■ ELECTRICAL CHARACTERISTICS

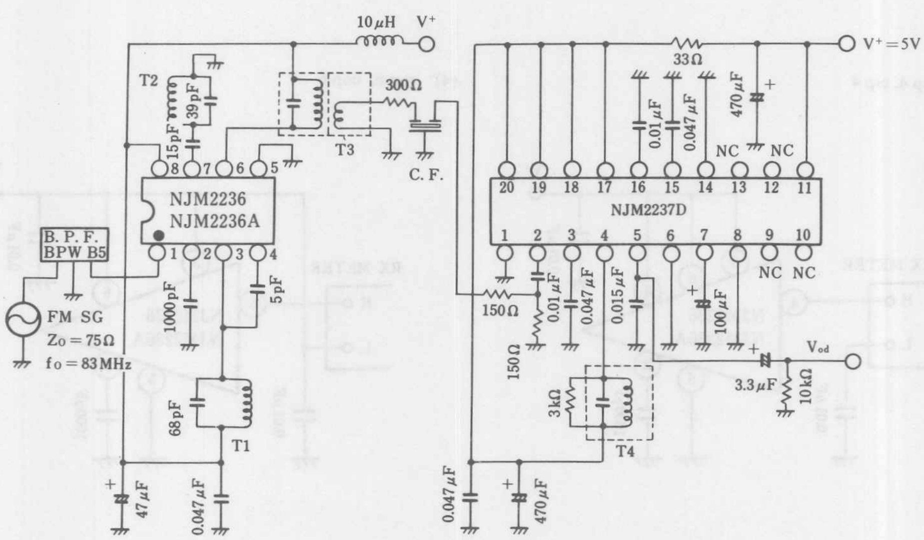
(V^+ =5V, [M-Type V^+ =3V], f=83MHz, fm=1kHz. △f=22.5kHz dev., Ta=25℃)

CHARACTERISTICS		SYMBOLS	CIRCUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Current		I_{CC}	2	$V_{IN}=0$	—	5.2	8.0	mA
−3dB Limiting Sensitivity		$V_{IN}(lim)$	2		—	3.0	7.0	dBμ
Quiescent Sensitivity		Q_S	2		—	11.0	—	dBμ
Conversion Gain		G_C	—		—	31	—	dB
Local OSC Voltage	NJM2236A	V_{OSC}	1	$f_{OSC}=60MHz$	40	80	120	mVrms
	NJM2236				70	110	180	mVrms
1 Pin Parallel Input Impedance	Resistance	r_{ip1}	3	f=83MHz	—	57	—	Ω
3 Pin Parallel Output Impedance	Resistance	ro_{p3}	3		—	25	—	kΩ
	Capacitance	co_{p3}			—	2.0	—	pF
4 Pin Parallel Input Impedance	Resistance	ri_{p4}	3		—	2.7	—	kΩ
	Capacitance	ci_{p4}			—	3.3	—	pF
6 Pin Parallel Output Impedance	Resistance	ro_{p6}	3	f=10.7MHz	—	100	—	kΩ
	Capacitance	co_{p6}			—	4.8	—	pF
Local OSC Stop Voltage		Vstop	1		—	0.9	1.3	V

■ TEST CIRCUIT 1



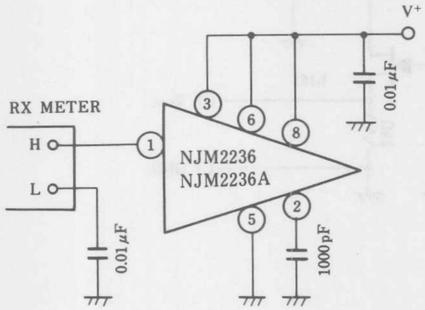
■ TEST CIRCUIT 2



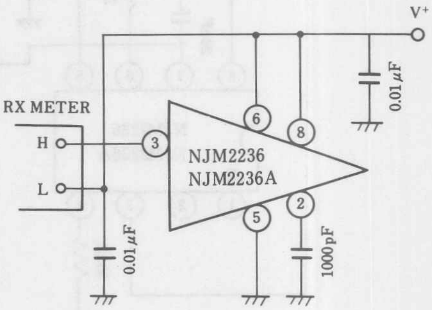
■ TEST CIRCUIT 3

Input, Output Impedance

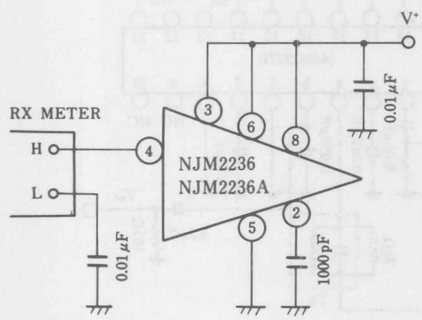
(1) rip 1



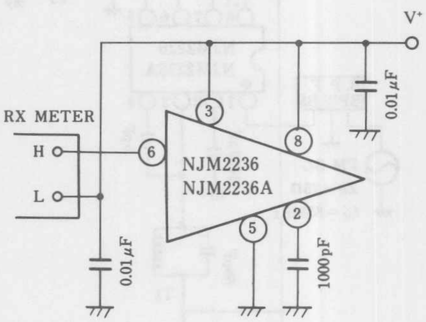
(2) rop 3, cop 3



(3) rip 4, cip 4

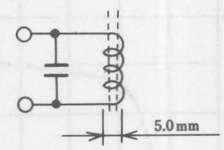
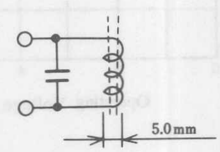
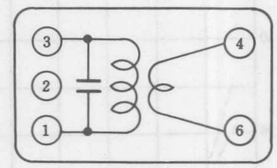
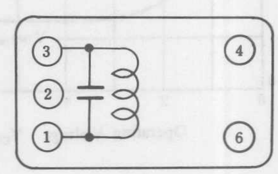


(4) rop 6, cop 6



■ TEST CIRCUIT COIL DATA

(Japan Band for 76.0MHz to 108.0MHz)

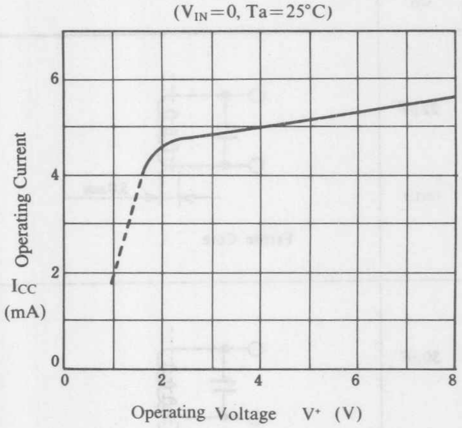
COIL	fo	Qo	TURNS	Co	
T 1 RF Coil	100MHz	100	0.7mmϕ $2\frac{1}{4}$ (Japan Band) SUMIDA 0295−057	22pF (ext.)	 Ferrite Core
T 2 osc Coil	100MHz	100	0.7mmϕ $2\frac{1}{2}$ (Japan Band) SUMIDA 0295−056	30pF (ext.)	 Ferrite Core
T 3 FM IFT Coil	10.7MHz	①−③ 90	①−③ 11T ④−⑥ 2T Wire : 0.12mmϕ UEW SUMIDA 2153−414−041	①−③ 82pF	 Bottom View
T 4 FM DET Coil	10.7MHz	①−③ 100	①−③ 10T Wire : 0.12mmϕ UEW SUMIDA 2153−4095−331	①−③ 150pF	 Bottom View

- Band Pass Filter (B. P. F.) : SOSHIN ELECTRIC Co., LTD. ···BPWB5
- Tuning Capacitor : ALPS ELECTRIC Co., LTD. ···VCB41E101

■ TYPICAL CHARACTERISTICS

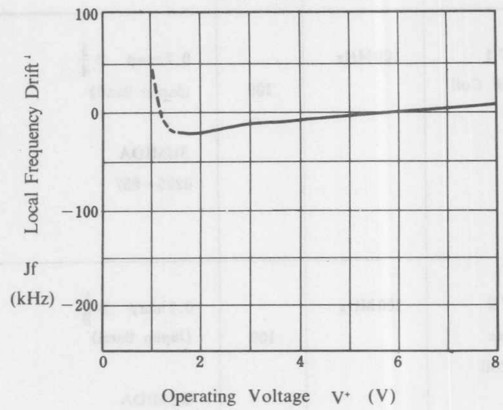
Operating Current vs. Operating Voltage

($V_{IN}=0$, Ta=25°C)



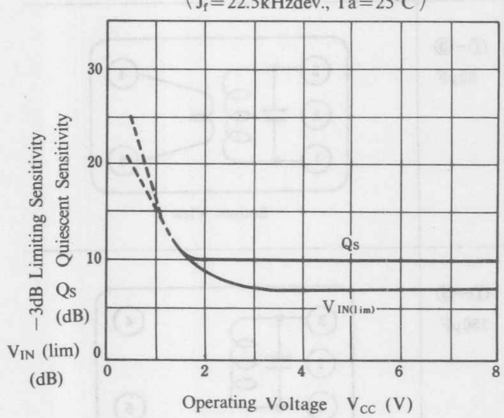
Local Frequency Drift vs. Operating Voltage

($V_{IN}=0$, Ta=25°C)



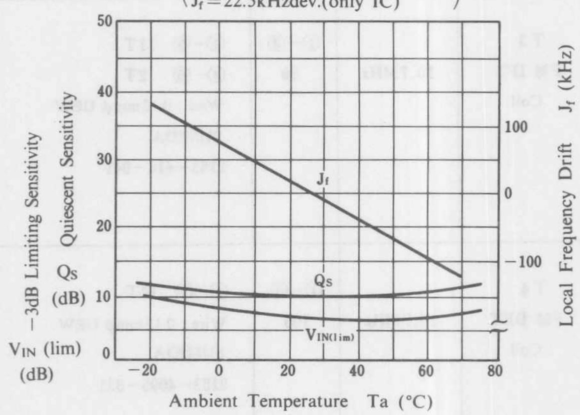
V_{IN}(lim), Q_S vs. V_{CC}

(f=63MHz, f_m=1kHz, J_f=22.5kHzdev., Ta=25°C)



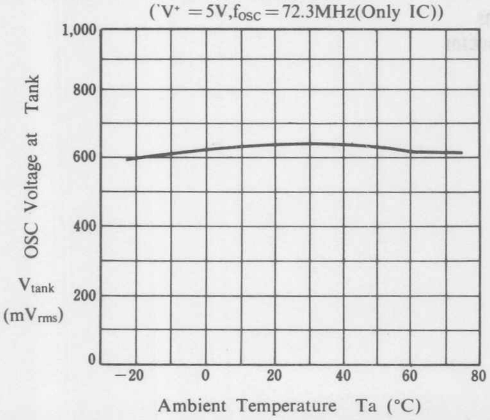
V_{IN}(lim), Q_S, J_f vs. T_a

(V^+=5V, f=83MHz, f_m=1kHz, J_f=22.5kHzdev.(only IC))



V_{tank} vs. T_a

(V^+=5V, f_{osc}=72.3MHz(Only IC))



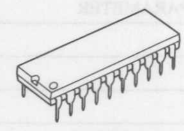
AM/FM RADIO

■ GENERAL DESCRIPTION

The NJM2237 is monolithic integrated circuit in a 20-lead dual in-line plastic package designed for use in 3-6V protable AM/FM radio receivers.

The functions incorporated are AM RF amplifier, AM mixer, FM/AM IF amplifier, FM/AM detecter, AM AGC circuit Audio Power amplifier.

■ PACKAGE OUTLINE

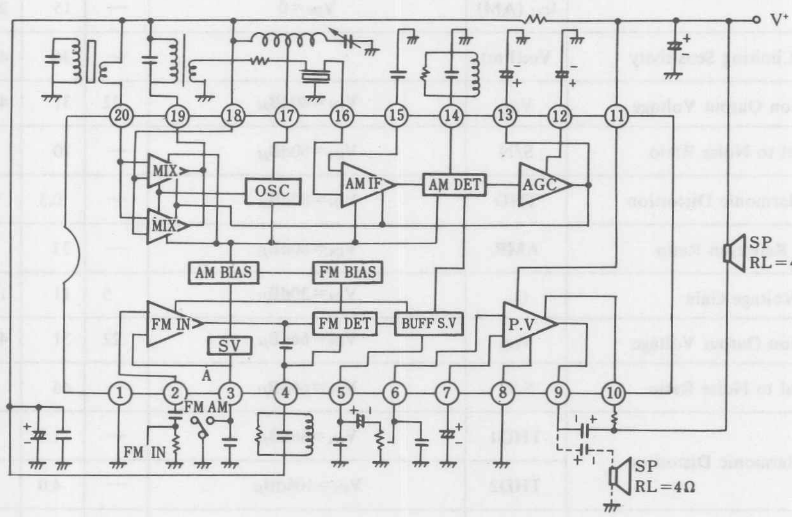


NJM 2237 D

■ FEATURES

- Wide Operating Voltage (1.8～6.0V)
- Very Simple DC switching of FM/AM
- High AM signal handling
- 4Ω speaker direct drive
- Low tweet
- Most suitable to use with NJM2236
- Package Outline DIP20
- Bipolar Technology

■ BLOCK DIAGRAM



(note) Dotted line shws V+ =4.5V

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Output Current	$I_{O(peak)}$	550	mA
Power Dissipation	P_D	1.2	W
Operating Temperature Range	T_{opr}	−20～75	℃
Storage Temperature Range	T_{stg}	−40～125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+ =3V, Ta=25℃, FM: f=10.7MHz, △f=22.5kHz dev., fm=1kHz
AM: f=1MHz, Mod=30%, fm=1kHz Unless otherwise noted)

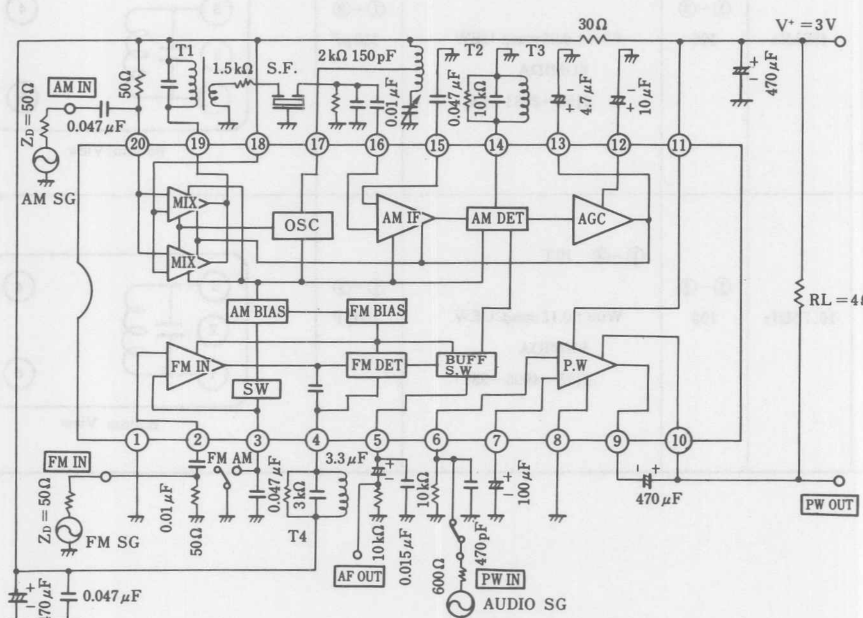
	CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Operating Current	I_{CC} (FM)	$V_{IN}=0$	—	15	20	mA
		I_{CC} (AM)	$V_{IN}=0$	—	15	20	
FM	−3dB Limiting Sensitivity	V_{IN}(lim)		—	36	42	dBμ
	Detection Output Voltage	V_{OD}	$V_{IN}=80dB\mu$	22	31	44	mVrms
	Signal to Noise Ratio	S/N	$V_{IN}=80dB\mu$	—	70	—	dB
	Total Harmonic Distortion	THD	$V_{IN}=80dB\mu$	—	0.3	—	%
	Am Rejection Ratio	AMR	$V_{IN}=80dB\mu$	—	33	—	dB
AM	Voltage Gain	G_V	$V_{IN}=30dB\mu$	5	11	17	mVrms
	Detection Output Voltage	V_{OD}	$V_{IN}=66dB\mu$	22	31	44	mVrms
	Signal to Noise Ratio	S/N	$V_{IN}=66dB\mu$	—	46	—	dB
	Total Harmonic Distortion	THD1	$V_{IN}=66dB\mu$	—	1.5	—	%
		THD2	$V_{IN}=106dB\mu$	—	4.0	—	
	Local OSC Stop Voltage	V_{STOP}	$V_{OSC}-6dB$	—	1.0	1.5	V
PW	Voltage Gain	G_V	f=1kHz, $R_L=4\Omega$	37	40	43	dB
	Output Power	$P_{OD}1$	f=1kHz, $R_L=4\Omega$, THD=10%	180	220	—	mW
		$P_{OD}2$	$V^+=4.5V$ f=1kHz, $R_L=4\Omega$, THD=10%	—	500	—	
	Total Harmonic Distortion	THD	f=1kHz, $R_L=4\Omega$, $P_O=50mW$	—	0.5	20	%
	Output Noise Voltage	V_{NO}	$R_O=10k\Omega$, RL=4Ω BW=30Hz～20kHz	—	0.18	—	mVrms

■ TERMINAL VOLTAGE AT NO SIGNAL

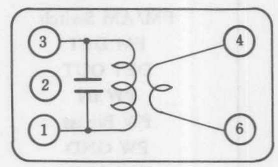
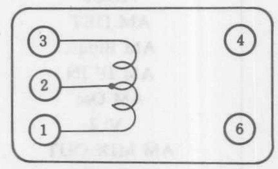
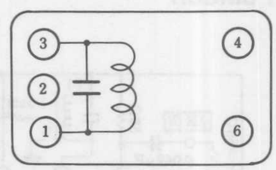
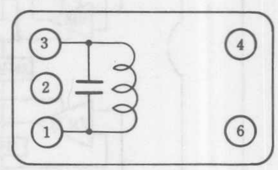
(V^+=3V, Ta=25℃)

CHARACTERISTICS		SYMBOLS	TYPICAL VALUE.		UNIT
PIN NO	FUNCTION		AT AM	AT FM	
1	GND	V_1	0	0	V
2	FM IF IN	V_2	2.4	2.0	V
3	FM/AM Switch	V_3	0	2.0	V
4	FM DET	V_4	2.9	2.9	V
5	DET OUT	V_5	0.4	0.7	V
6	PW IN	V_6	0	0	V
7	PW Bipass	V_7	0.6	0.6	V
8	PW GND	V_8	0	0	V
9	PW OUT	V_9	1.5	1.5	V
10	PW Bootstrap	V_{10}	2.8	2.8	V
11	V^+ 1	V_{11}	3.0	3.0	V
12	AGC1	V_{12}	0.6	0	V
13	AGC2	V_{13}	0.6	0	V
14	AM DET	V_{14}	0	0	V
15	AM Bipass	V_{15}	1.3	0	V
16	AM IF IN	V_{16}	1.3	0	V
17	AM Osc	V_{17}	2.9	2.9	V
18	V^+ 2	V_{18}	2.9	2.9	V
19	AM MIX OUT	V_{19}	2.9	2.9	V
20	AM RF IN	V_{20}	2.9	2.9	V

■ TEST CIRCUIT



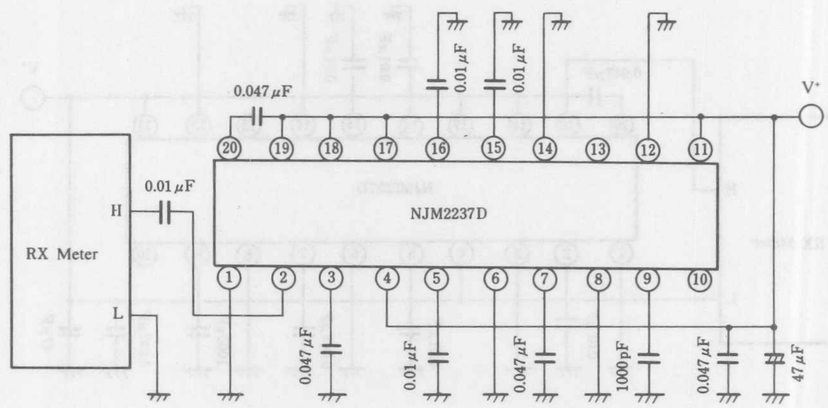
■ TEST CIRCUIT COIL DATA

COIL NO.	Fo	Qo	TURNS	Co	BOTTOM VIEW
T₁ : FM IFT (MIX OUT)	455kHz	①-③ 80	①-③ 60T ④-⑥ 16T Wire : 0.09mmϕ UEW SUMIDA 2150-2173-302	①-③ 1500pF	 Bottom View
T₂ : AM OSC	796kHz	①-③ 125	①-② 15T ②-③ 89T Wire : 0.06mmϕ UEW SUMIDA 2157-2239-213A	–	 Bottom View
T₃ : AM DET	455kHz	①-③ 105	①-③ 127T Wire : 0.06mmϕ UEW SUMIDA 2150-2083-061	①-③ 330pF	 Bottom View
T₄ : FM DET	10.7MHz	①-③ 100	①-③ 10T Wire : 0.12mmϕ UEW SUMIDA 2153-4095-331	①-③ 150pF	 Bottom View

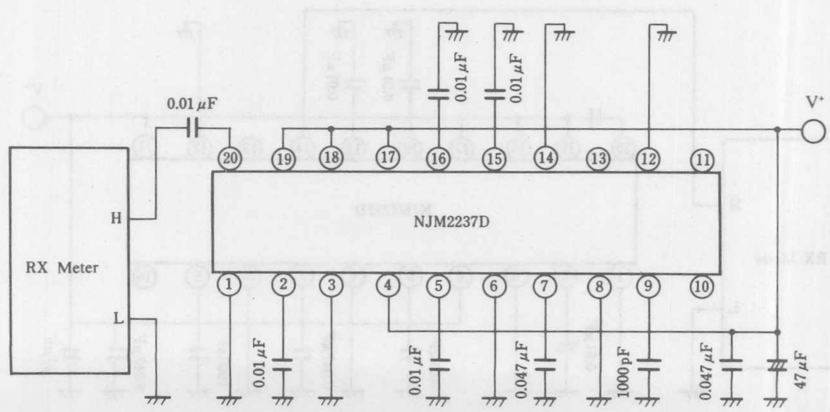
■ INPUT OUTPUT IMPEDANCE

CHARACTERISTIC	SYMBOL	CIRCUIT	TEST CONDITION	TYP.	UNIT
Pin 2 Input Impedance (FM)	R_{IN2} C_{IN2}	1	f=10.7MHz	4.6 5.0	kΩ pF
Pin 20 Input Impedance (AM)	R_{IN20} C_{IN20}	2	f=1MHz	20 11	kΩ pF
Pin 16 Input Impedance (AM)	R_{IN16} C_{IN16}	3	f=455kHz	6 3.7	kΩ pF
Pin 19 Output Impedance (AM)	R_{O19} C_{O19}	4	f=455kHz	2.5 5.5	kΩ pF
Pin 14 Output Impedance (AM)	R_{O14} C_{O14}	5	f=455kHz	100 5.0	kΩ pF

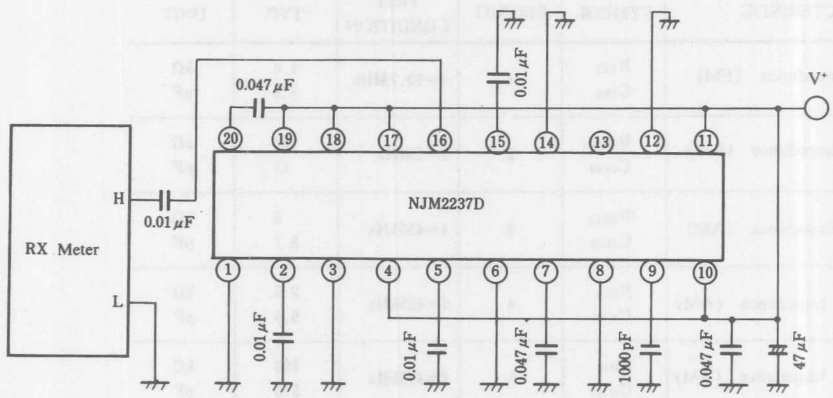
■ TEST CIRCUIT 1 (Pin 2 FM Input Resistance, Capacitance)



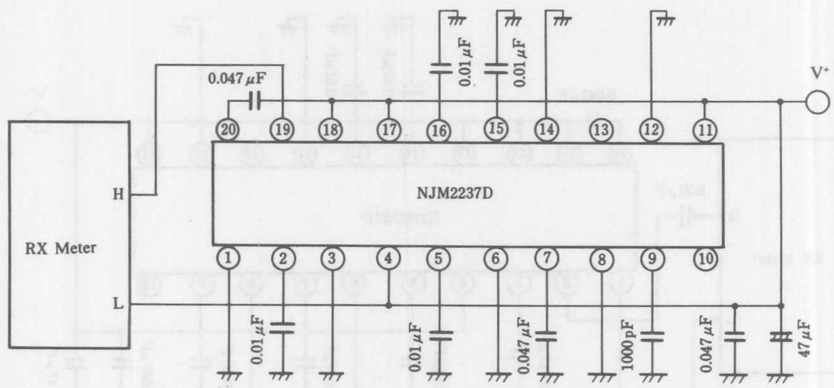
■ TEST CIRCUIT 2 (Pin 20 AM Input Resistance, Capacitance)



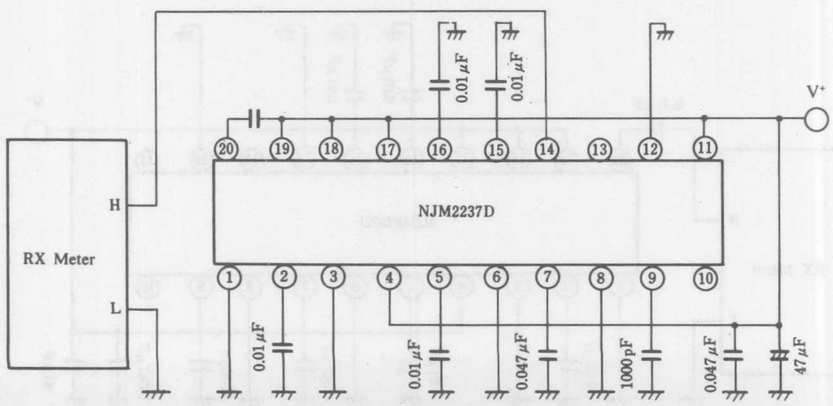
■ **TEST CIRCUIT 3** (Pin 16 AM IF Input Resistance, Capacitance)



■ **TEST CIRCUIT 4** (Pin 19 AM Mix Output Resistance, Capacitance)

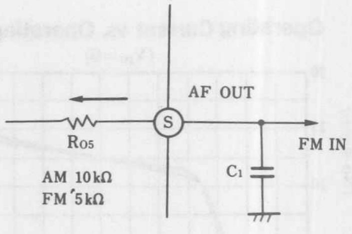


■ **TEST CIRCUIT 5** (Pin 14 AM DET Output Resistance, Capacitance)



■ NOTES

1. The frequency characteristics at AM and FM mode
   The output impedance of pin5 (Ro5) and external capacitor C1 decide frequency characteristics.
   The value of Ro5 turns to 10kΩ at AM mode and 5kΩ at FM mode.
   Accordingly should consider above, trim C1 to get proper frequency response.
   Besides should design the location of C1 closer to pin1 (GND) to get low tweet.



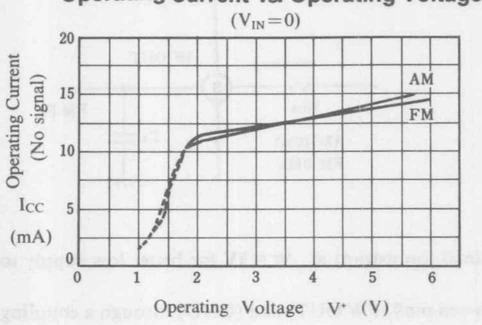
2. Loading speaker
   Recommend to connect the speaker between pin11 (V^+) and pin10 (bootstrap) at $V^+ = 3V$ for better low supply to voltage operation.
   When Vcc is above 4.5V, recommend the speaker connection between pin9 (PW OUT) and (GND) through a coupling capacitor.

3. Termination to the power stage
   The audio signal of output pin5 includes carrier component slightly, therefore a capacitor between pin6 and GND have to be connected to decrease carrier component.

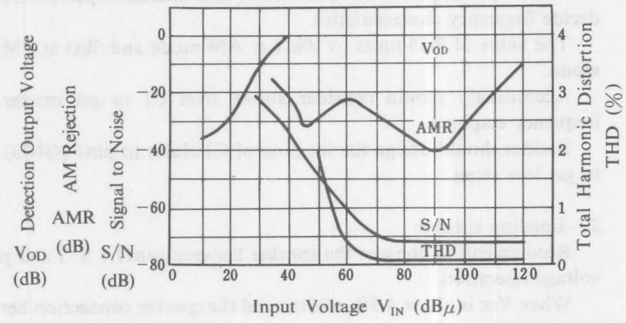
4. Supply voltage start-up
   The supply voltage of radio circuit block should not start up before power stage start-up.

■ TYPICAL CHARACTERISTICS

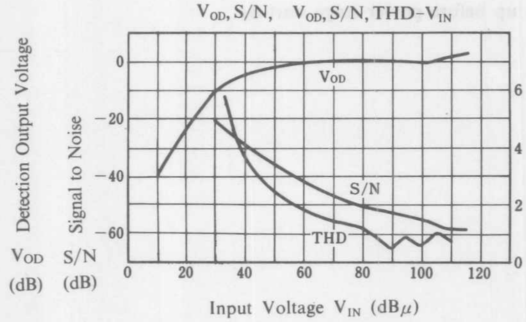
Operating Current vs. Operating Voltage



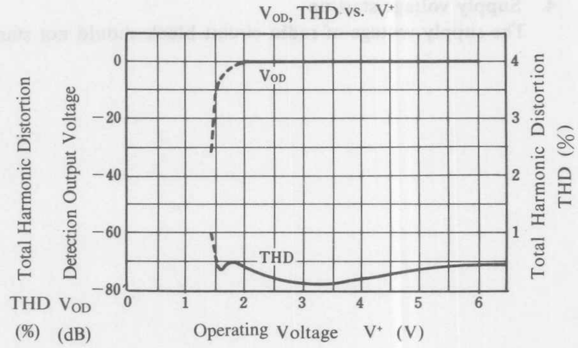
V_{OD}, AMR, S/N, THD vs. V_{IN}



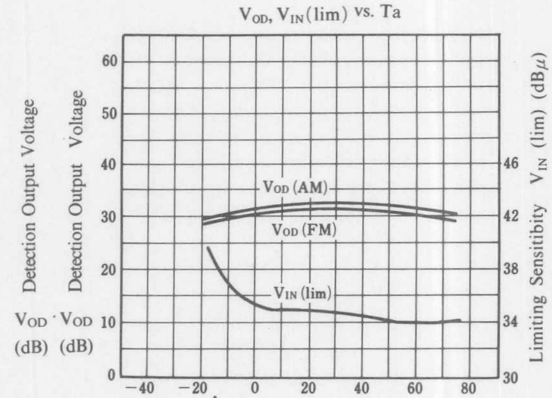
V_{OD}, S/N, V_{OD}, S/N, THD-V_{IN}



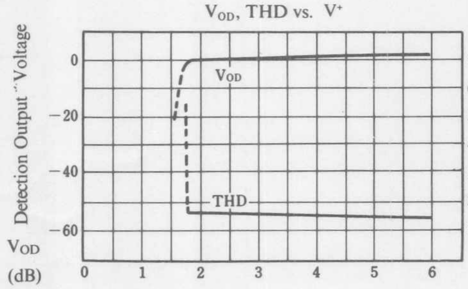
V_{OD}, THD vs. V^+



V_{OD}, V_{IN}(lim) vs. Ta

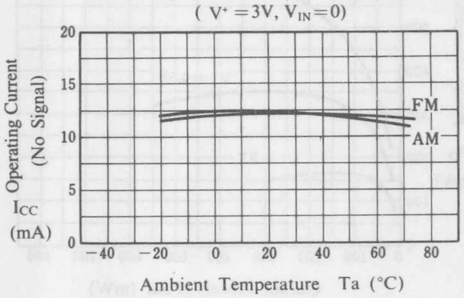


V_{OD}, THD vs. V^+

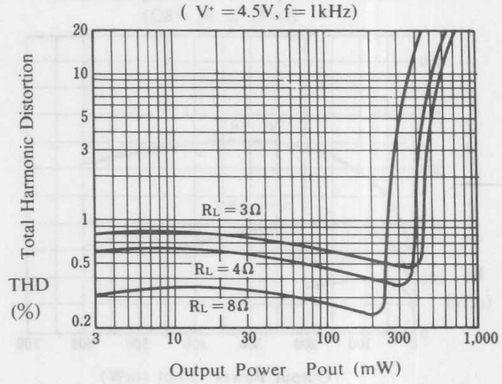


■ TYPICAL CHARACTERISTICS

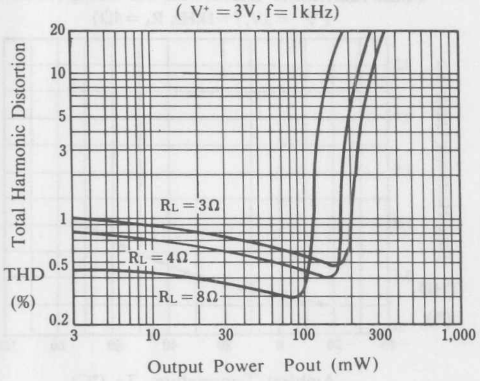
Operating Current vs. Temperature
($V^+=3V$, $V_{IN}=0$)



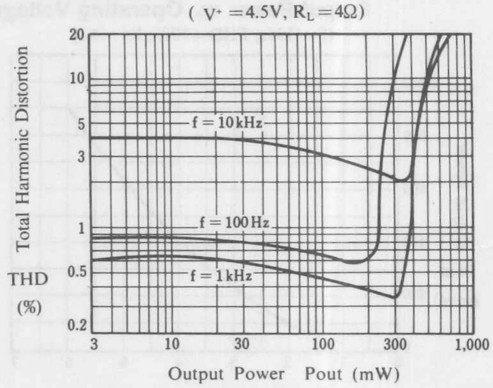
Total Harmonic Distortion vs. Output Power
($V^+=4.5V$, f=1kHz)



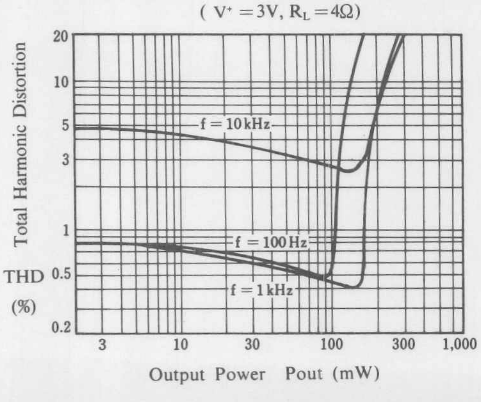
Total Harmonic Distortion vs. Output Power
($V^+=3V$, f=1kHz)



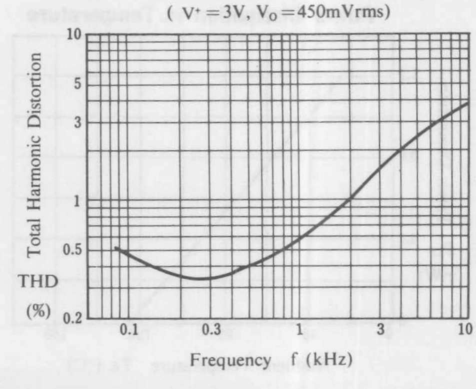
Total Harmonic Distortion vs. Output Power
($V^+=4.5V$, $R_L=4\Omega$)



Total Harmonic Distortion vs. Output Power
($V^+=3V$, $R_L=4\Omega$)

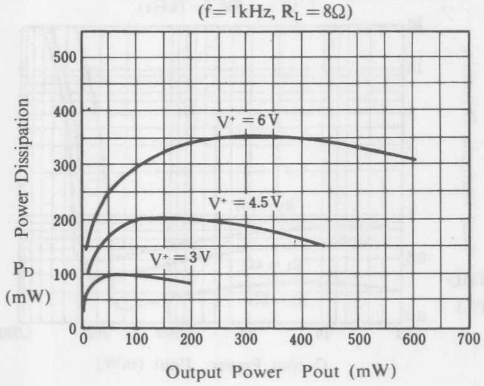


Total Harmonic Distortion vs. Frequency
($V^+=3V$, $V_O=450mVrms$)

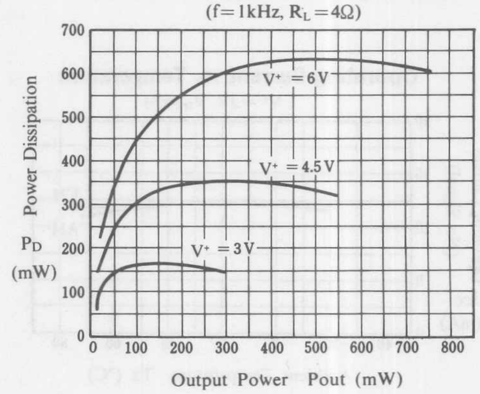


■ TYPICAL CHARACTERISTICS

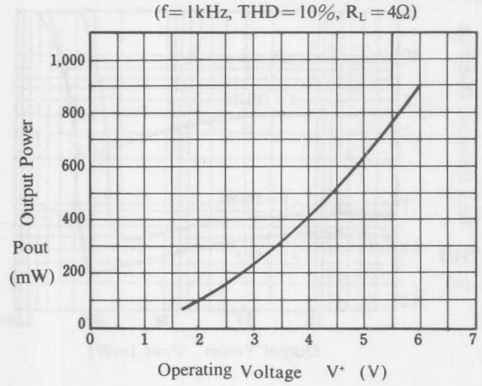
Power Dissipation vs. Output Power
(f=1kHz, R_L=8Ω)



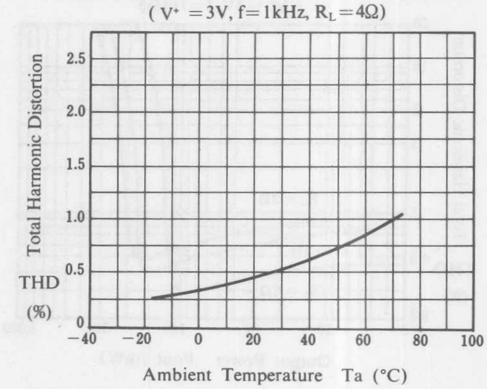
Power Dissipation vs. Output Power
(f=1kHz, R_L=4Ω)



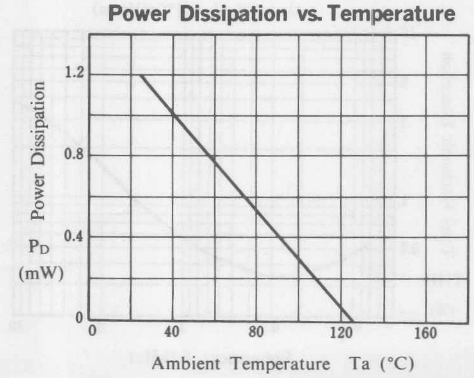
Output Power vs. Operating Voltage
(f=1kHz, THD=10%, R_L=4Ω)



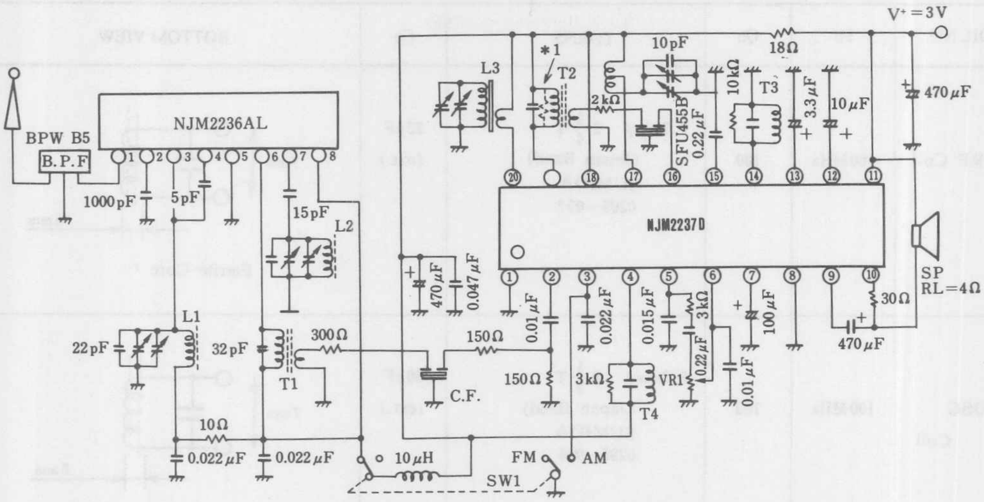
Total Harmonic Distortion vs. Temperature
(V+ =3V, f=1kHz, R_L=4Ω)



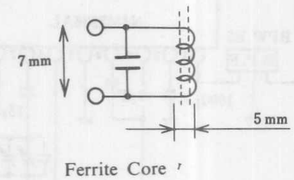
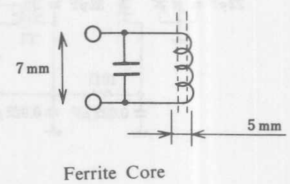
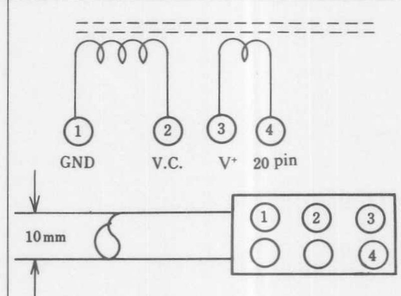
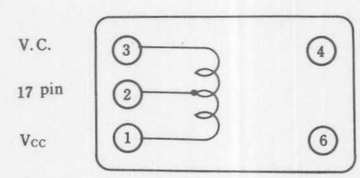
Power Dissipation vs. Temperature

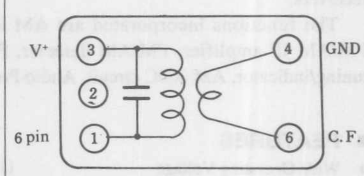
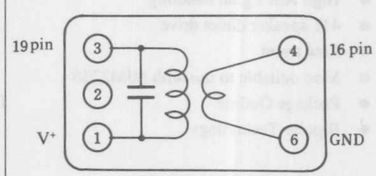
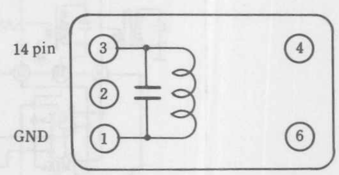
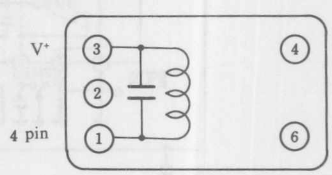


■ FM/AM RADIO APPLICATION CIRCUIT



■ FM/AM RADIO APPLICATION CIRCUIT

COIL NO.	F_0	Q_0	TURNS	C_0	BOTTOM VIEW
L_1 : RF Coil	100 MHz	100	0.7mmφ $2\frac{1}{4}$ T (Japan Band) SUMIDA 0295−057	22 pF (ext.)	
L_2 : OSC Coil	100 MHz	100	0.7mmφ $2\frac{1}{2}$ T (Japan Band) SUMIDA 0295−056	30 pF (ext.)	
L_3 : AM ANT	796 kHz	①−② 200	①−② 100 T L=600 μH ③−④ 17 T Wire : 4/0.07mm UATC Core : 10mmφ×80mm MITUMI YI−7160−1	−	 BOTTOM VIEW
L_4 : AM OSC	796 kHz	①−③ 125	①−② 15 T ②−③ 89 T Wire : 0.06mmφ UEW SUMIDA 2157−2239−213 A	−	 BOTTOM VIEW

COIL NO.	F0	Q0	TURNS	C0	BOTTOM VIEW
T_1 : FM IFT	10.7MHz	①−③ 90	①−③ 11 T ④−⑥ 2 T Wire : 0.12 mmφ UEW SUMIDA 2153−414−041	①−③ 82pF	
T_2 : AM IFT	455kHz	①−③ 80	①−③ 60 T ④−⑥ 16 T Wire : 0.09 mmφ UEW SUMIDA 2150−2173−302	①−③ 1500pF	
T_3 : AM DET	455kHz	①−③ 105	①−③ 127 T Wire : 0.06 mmφ UEW SUMIDA 2150−2083−061	①−③ 3330pF	
T_4 : FM DET	10.7MHz	①−③ 100	①−③ 10 T Wire : 0.12 mmφ UEW SUMIDA 2153−4095−331	①−③ 150pF	

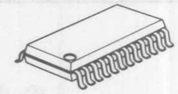
AM/FM RADIO

■ GENERAL DESCRIPTION

The NJM2241 is monolithic integrated circuit in a 24-lead small outline package designed for use in 3-6V protable AM/FM radio receivers.

The functions incorporated are AM RF amplifier, AM mixer, FM/AM IF amplifier, FM/AM detecter, FM/AM detecter, FM/AM tuning/indicator, AM AGC circuit, Audio Power amplifier.

■ PACKAGE OUTLINE

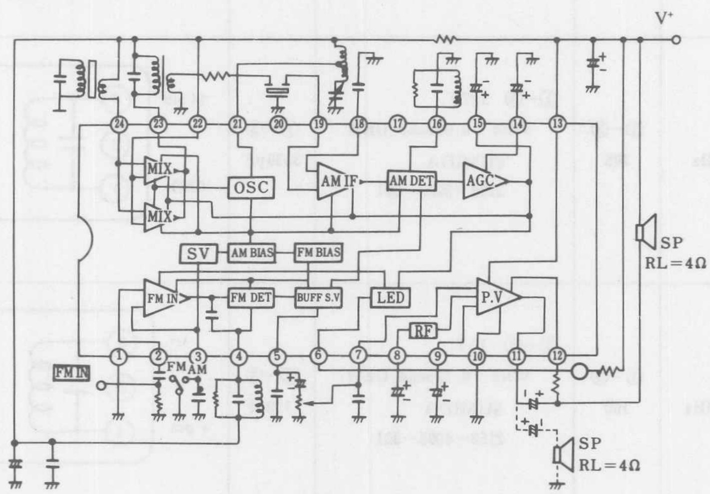


NJM2241M

■ FEATURES

- Wide Operating Voltage (1.8~6.0V)
- Tuning Indicator LED direct drive (10mA Max.)
- Very Simple DC switching of FM/AM
- High AM signal handling
- 4Ω speaker direct drive
- Low tweet
- Most suitable to use with NJM2236
- Package Outline DMP24
- Bipolar Technology

■ BLOCK DIAGRAM



(note) Dotted line shows V_{CC}=4.5V

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8	V
Lamp Current	$I_{Lamp(Max)}$	10	mA
Output Current	$I_{O(peak)}$	550	mA
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=3V, Ta=25℃, FM: f=10.7MHz, △f=22.5kHz dev., fm=1kHz
AM: f=1MHz, Mod=30%, fm=1kHz Unless otherwise noted)

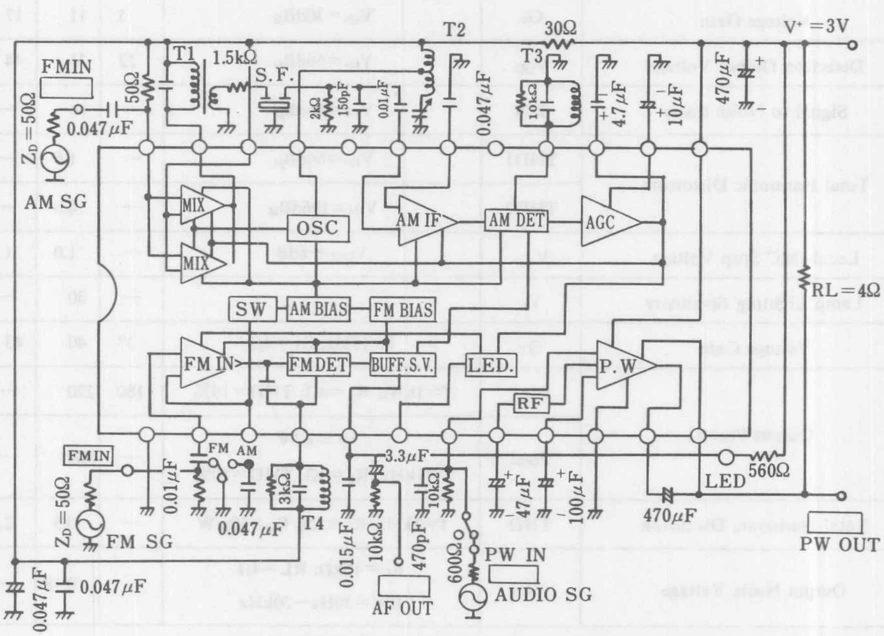
	CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Operating Current	I_{CC} (FM)	$V_{IN}=0$	—	15	20	mA
		I_{CC} (AM)	$V_{IN}=0$	—	15	20	
FM	−3dB Limiting Sensitivity	V_{IN}(lim)		—	36	42	dBμ
	Detection Output Voltage	V_{OD}	$V_{IN}=80$dBμ	22	31	44	mVrms
	Signal to Noise Ratio	S/N	$V_{IN}=80$dBμ	—	70	—	dB
	Total Harmonic Distortion	THD	$V_{IN}=80$dBμ	—	0.3	—	%
	Am Rejection	AMR	$V_{IN}=80$dBμ	—	33	—	dB
	Lamp Lighting Sensitivity	V_L		—	47	55	dBμ
AM	Voltage Gain	G_V	$V_{IN}=30$dBμ	5	11	17	mVrms
	Detection Output Voltage	V_{OD}	$V_{IN}=66$dBμ	22	31	44	mVrms
	Signal to Noise Ratio	S/N	$V_{IN}=66$dBμ	—	46	—	dB
	Total Harmonic Distortion	THD1	$V_{IN}=66$dBμ	—	1.5	—	%
		THD2	$V_{IN}=106$dBμ	—	4.0	—	
	Local OSC Stop Voltage	V_{stop}	$V_{OSC}-6$dB	—	1.0	1.5	V
	Lamp Lighting Sensitivity	V_L		—	30	—	dBμ
PW	Voltage Gain	G_V	f=1kHz, $R_L=4\Omega$	37	40	43	dB
	Output Power	$P_{OD}1$	f=1kHz, $R_L=4\Omega$, THD=10%	180	220	—	mW
		$P_{OD}2$	$V^+=4.5$V f=1kHz, $R_L=4\Omega$, THD=10%	—	500	—	
	Total Harmonic Distortion	THD	f=1kHz, $R_L=4\Omega$, $P_O=50$mW	—	0.5	2.0	%
	Output Noise Voltage	V_{NO}	$R_O=10$kΩ, RL=4Ω BW=30Hz～20kHz		0.18	—	mVrms

■ TERMINAL VOLTAGE AT NO SIGNAL

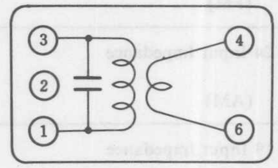
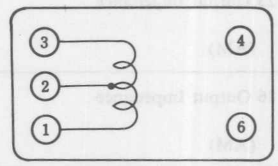
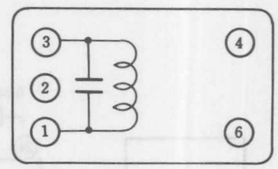
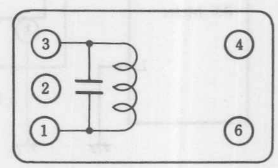
(V⁺=3V, Ta=25℃)

CHARACTERISTICS		SYMBOLS	TYPICAL VALUES		UNIT
PIN NO	FUNCTION		AT AM	AT FM	
1	GND	V_1	0	0	V
2	FM IF IN	V_2	2.4	2.0	V
3	FM/AM Switch	V_3	0	2.0	V
4	FM DET	V_4	2.9	2.9	V
5	DET OUT	V_5	0.4	0.7	V
6	LED DRIVER	V_6	—	—	V
7	PW IN	V_7	0	0	V
8	PW REF	V_8	1.35	1.35	V
9	PW Bipass	V_9	0.6	0.6	V
10	PW GND	V_{10}	0	0	V
11	PW OUT	V_{11}	1.5	1.5	V
12	PW Bootstrap	V_{12}	2.8	2.8	V
13	V⁺ 1	V_{13}	3.0	3.0	V
14	AGC1	V_{14}	0.6	0	V
15	AGC2	V_{15}	0.6	0	V
16	AM DET	V_{16}	0	0	V
17	Not Use	—	—	—	—
18	AM Bipass	V_{18}	1.3	0	V
19	AM IF IN	V_{19}	1.3	0	V
20	Not Use	—	—	—	—
21	AM Osc	V_{21}	2.9	2.9	V
22	V⁺ 2	V_{22}	2.9	2.9	V
23	AM MIX OUT	V_{23}	2.9	2.9	V
24	AM RF IN	V_{24}	2.9	2.9	V

■ TEST CIRCUIT



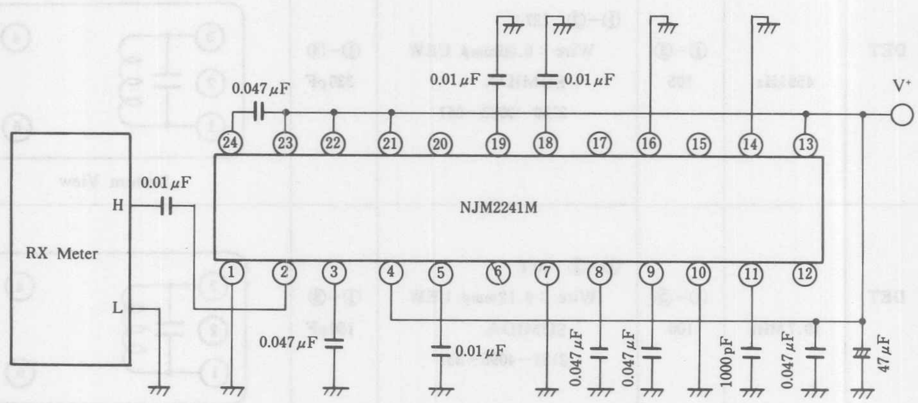
■ TEST CIRCUIT COIL DATA

COIL NO.	F_0	Q_0	TURNS	C_0	
T_1 : AM IFT (MIX OUT)	455 kHz	①-③ 80	①-③ 60 T ④-⑥ 16 T Wire : 0.09 mmφ UEW SUMIDA 2150-2173-302	①-③ 1500 pF	 Bottom View
T_2 : AM OSC	796 kHz	①-③ 125	①-② 15 T ②-③ 89 T Wire : 0.06 mmφ UEW SUMIDA 2157-2239-213 A	—	 Bottom View
T_3 : AM DET	455 kHz	①-③ 105	①-③ 127 T Wire : 0.06 mmφ UEW SUMIDA 2150-2083-061	①-③ 330 pF	 Bottom View
T_4 : FM DET	10.7 MHz	①-③ 100	①-③ 10 T Wire : 0.12 mmφ UEW SUMIDA 2153-4095-331	①-③ 150 pF	 Bottom View

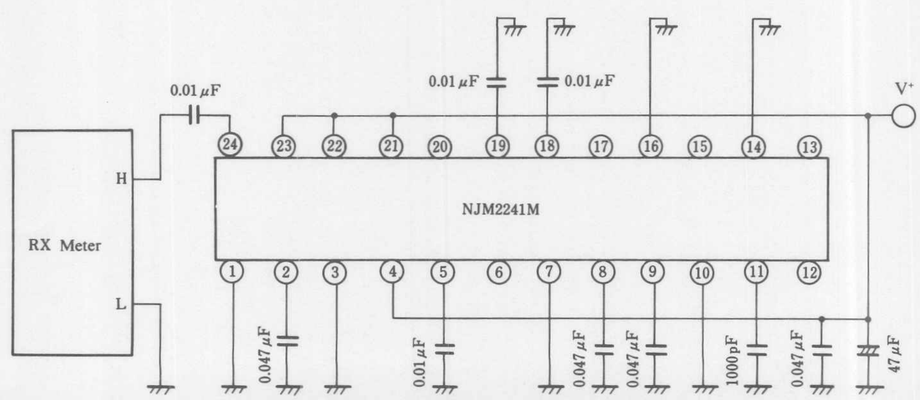
■ INPUT OUTPUT IMPEDANCE

CHARACTERISTICS	SYMBOLS	CIRCUITS	TEST CONDITIONS	TYP.	UNIT
Pin 2 Input Impedance	RIN2	1	f=10.7MHz	4.6	kΩ
(FM)	CIN2			5.0	pF
Pin 24 Input Impedance	RIN24	2	f=1kHz	20	kΩ
(AM)	CIN24			11	pF
Pin 19 Input Impedance	RIN19	3	f=455kHz	6	kΩ
(AM)	CIN19			3.7	pF
Pin 23 Output Impedance	RO23	4	f=455kHz	2.5	kΩ
(AM)	CO23			5.5	pF
Pin 16 Output Impedance	RO16	5	f=455kHz	100	kΩ
(AM)	CO16			5.0	pF

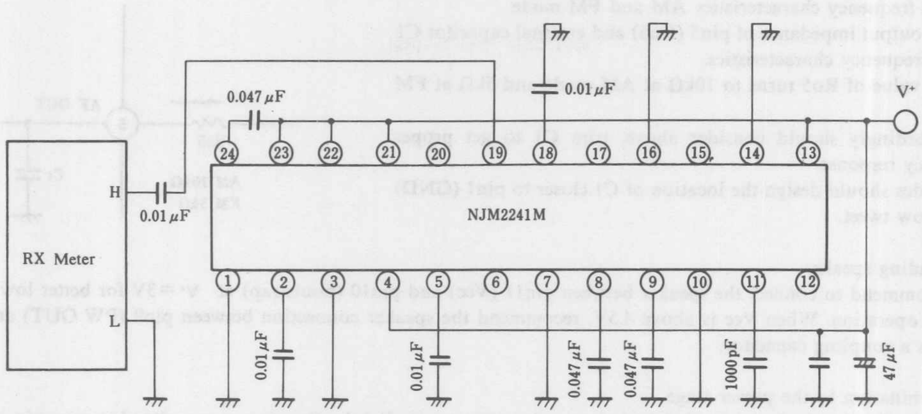
■ TEST CIRCUIT 1 (Pin 2 FM Input Resistance, Capacitance)



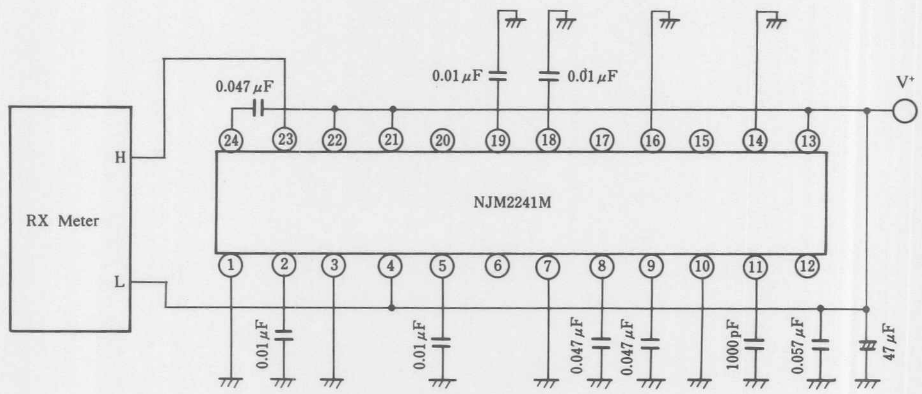
■ TEST CIRCUIT 2 (Pin 24 AM Input Resistance, Capacitance)



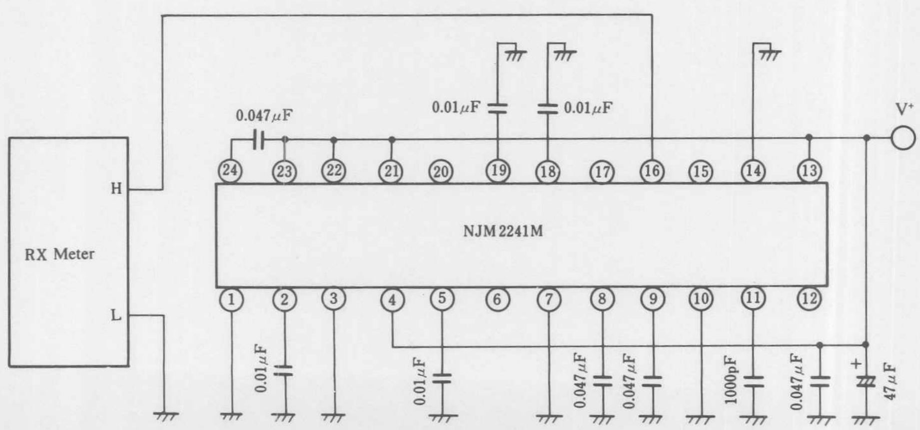
■ **TEST CIRCUIT 3** (Pin 19 AM IF Input Resistance, Capacitance)



■ **TEST CIRCUIT 4** (Pin 23 AM Mix Output Resistance, Capacitance)



■ **TEST CIRCUIT 5** (Pin 16 AM DET Output Resistance, Capacitance)



■ NOTES

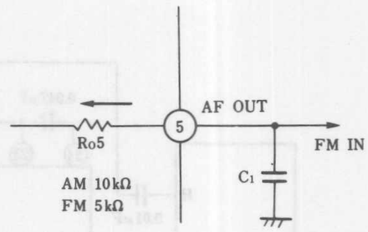
1. The frequency characteristics AM and FM mode

The output impedance of pin5 (Ro5) and external capacitor C1 decide frequency characteristics.

The value of Ro5 turns to 10kΩ at AM mode and 5kΩ at FM mode.

Accordingly should consider above, trim C1 to get proper frequency response.

Besides should design the location of C1 closer to pin1 (GND) to get low tweet.



2. Loading speaker

Recommend to connect the speaker between pin11 (Vcc) and pin10 (bootstrap) at $V^+=3V$ for better low supply to voltage operation. When Vcc is above 4.5V, recommend the speaker connection between pin9 (PW OUT) and (GND) through a coupling capacitor.

3. Termination to the power stage

The audio signal of output pin5 includes carrier component slightly, therefore a capacitor between pin and GND have to be connected to decrease carrier component.

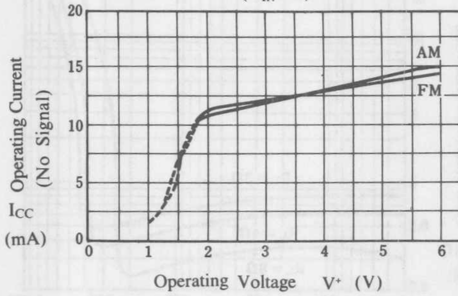
4. Supply voltage start-up

The supply voltage of radio circuit block should not start up before power stage start-up.

■ TYPICAL CHARACTERISTICS

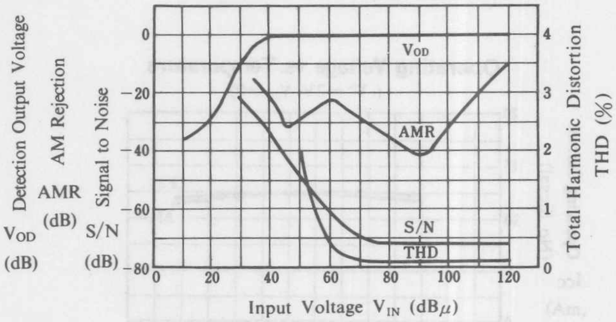
Operating Current vs. Operating Voltage

$(V_{IN}=0)$



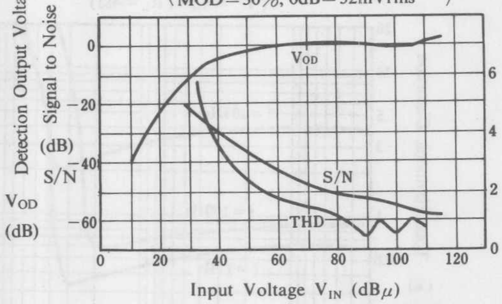
V_{OD},AMR, S/N, THDvs. Input Voltage

($V^+=3V$, $f=10.7MHz$, $f_m=1kHz$
$\Delta f=22.5kHz$ dev., $0dB=34.5mVrms$)



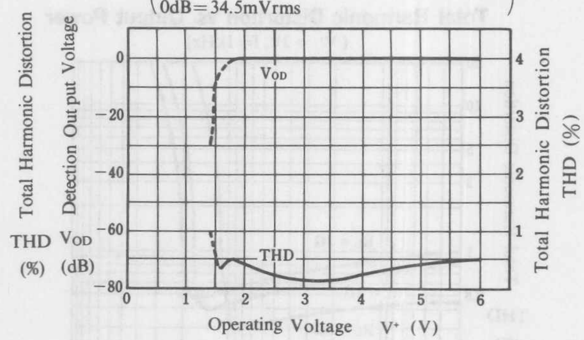
V_{OD},S/N, THD vs. Input Voltage

($V^+=3V$, $f=1005kHz$, $f_m=1kHz$, $MOD=30\%$, $0dB=32mVrms$)



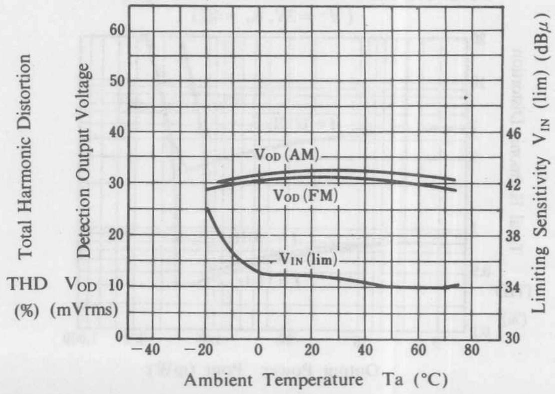
V_{OD}, THD vs. Operating Voltage

($f=10.7MHz$, $f_m=1kHz$, $\Delta f=22.5kHz$ dev., $0dB=34.5mVrms$)



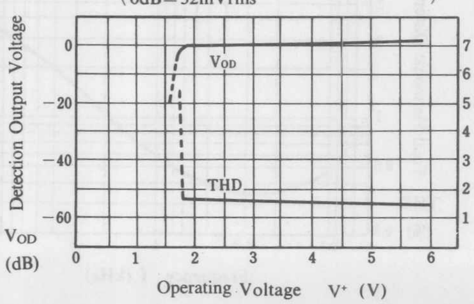
V_{OD},V_{IN}(lim) vs. Temperature

($V^+=3V$, AM:$f=1005kHz$, $f_{IN}=1kHz$, $MOD=30\%$
FM:$f=10.7MHz$, $f_m=1kHz$, $\Delta f=22.5kHz$dev.)



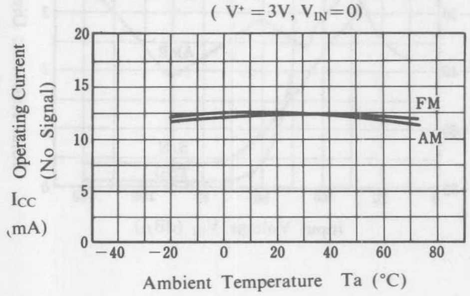
V_{OD}, THD vs. Operating Voltage

($f=1005kHz$, $f_m=1kHz$, $MOD=30\%$, $0dB=32mVrms$)

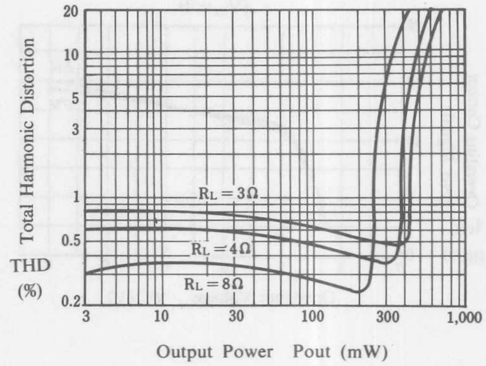


■ TYPICAL CHARACTERISTICS

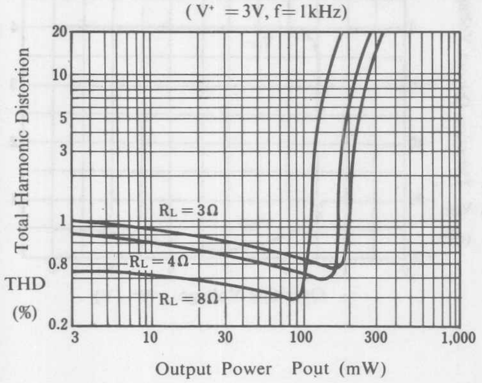
Operating Voltage vs. Temperature
($V^+ = 3V$, $V_{IN} = 0$)



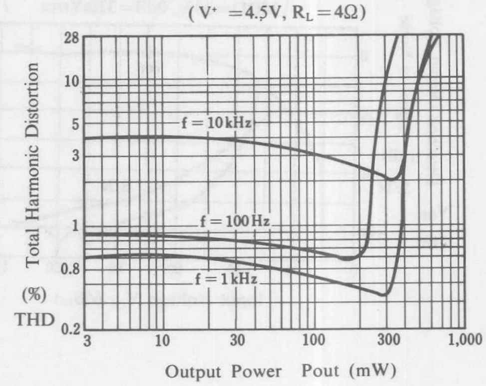
Total Harmonic Distortion vs. Output Power
($V^+ = 4.5V$, $f = 1kHz$)



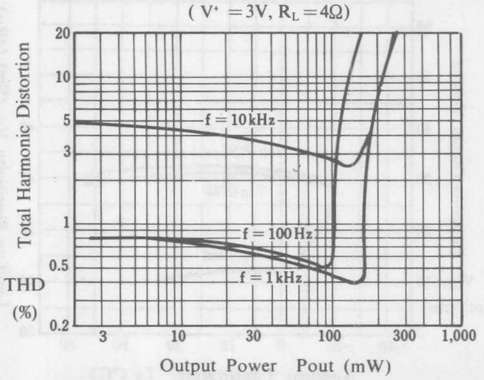
Total Harmonic Distortion vs. Output Power
($V^+ = 3V$, $f = 1kHz$)



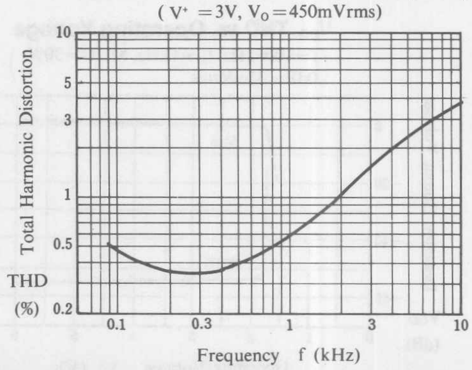
Total Harmonic Distortion vs. Output Power
($V^+ = 4.5V$, $R_L = 4\Omega$)



Total Harmonic Distortion vs. Output Power
($V^+ = 3V$, $R_L = 4\Omega$)

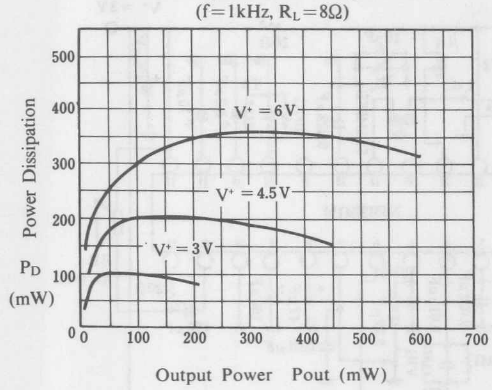


Total Harmonic Distortion vs. Frequency
($V^+ = 3V$, $V_O = 450mVrms$)

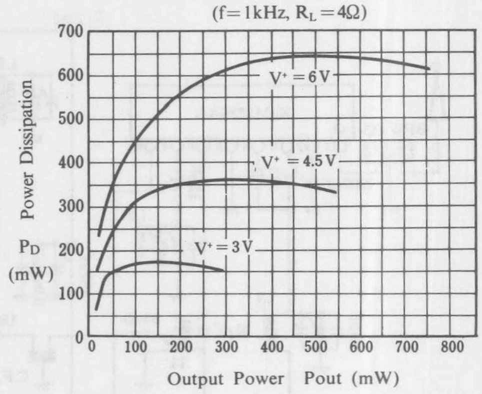


■ TYPICAL CHARACTERISTICS

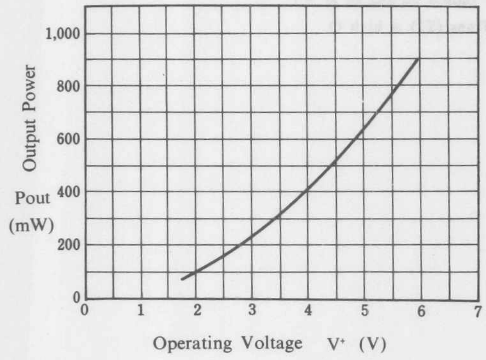
Power Dissipation vs. Output Power
($f = 1kHz$, $R_L = 8\Omega$)



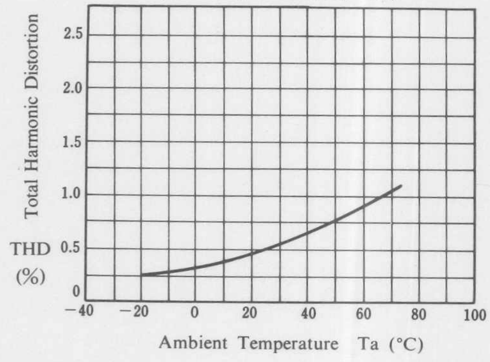
Power Disspation vs. Output Power
($f = 1kHz$, $R_L = 4\Omega$)



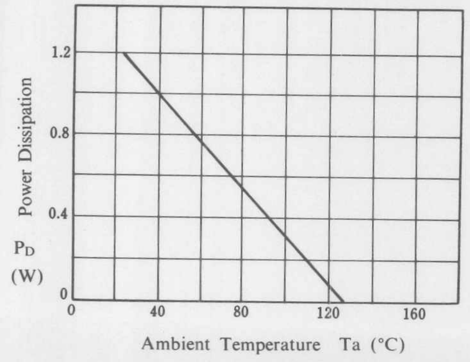
Output Power vs. Operating Voltage
($f = 1kHz$, THD = 10%, $R_L = 4\Omega$)



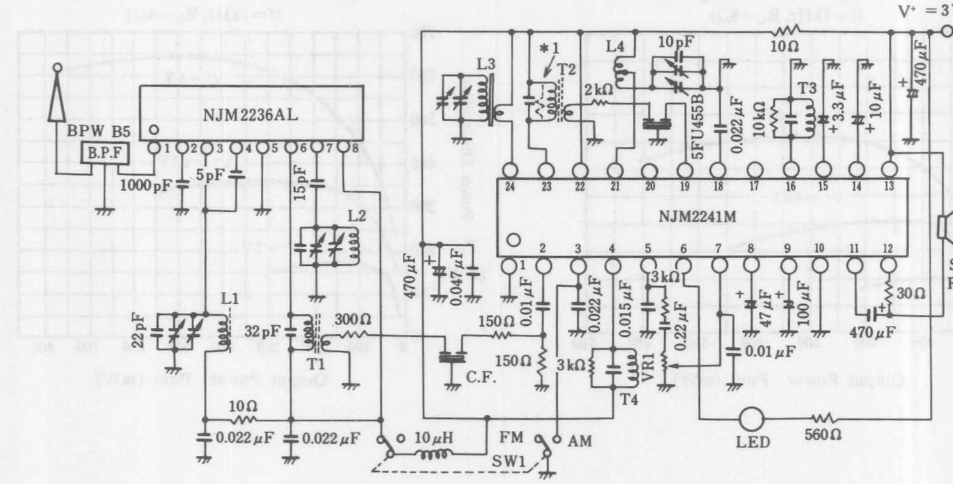
Total Harmonic Distortion vs. Temperature
($V^+ = 3V$, $f = 1kHz$, $R_L = 4\Omega$)



Power Dissipation vs. Temperature

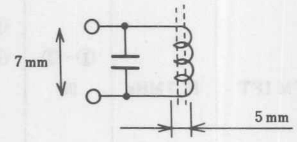
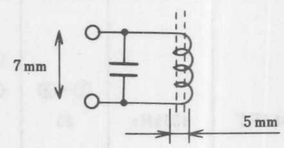
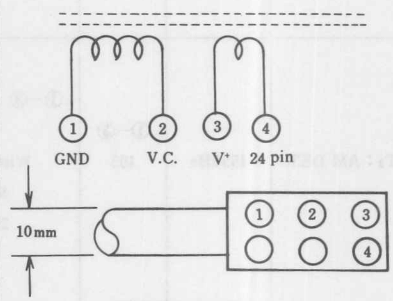
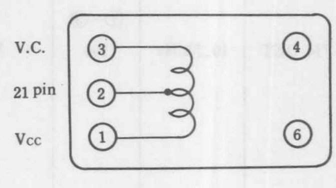


■ FM/AM RADIO APPLICATION CIRCUIT

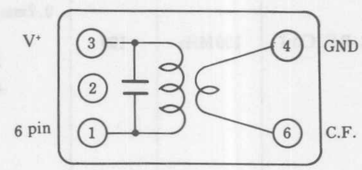
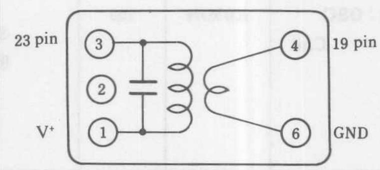
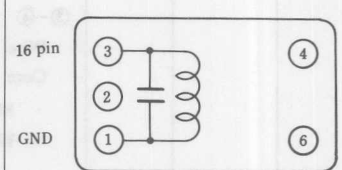
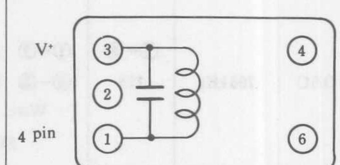


Resister should be located at $*1$
if the Trans (T2) is high Q

■ FM/AM RADIO APPLICATION CIRCUIT

COIL NO.	Fo	Qo	TURNS	Co	
L_1 : RF Coil	100MHz	100	0.7mmφ $2\frac{1}{4}$ T SUMIDA 0295−057	22pF (ext.)	 Ferrite Core
L_2 : OSC Coil	100MHz	100	0.7mmφ $2\frac{1}{2}$ T SUMIDA 0295−056	30pF (ext.)	 Ferrite Core
L_3 : AM ANT	796kHz	①−② 200	①−② 100 T L=600μH ③−④ 17 T Wire : 4/0.07mm UATC Core : 10mmφ×80mm MITUMI YI−7160−1		 BOTTOM VIEW
L_4 : AM OSC	796kHz	①−③ 125	①−② 15 T ②−③ 89 T Wire : 0.06mmφ UEW SUMIDA 2157−2239−213A	−	 BOTTOM VIEW

■ FM/AM RADIO APPLICATION CIRCUIT

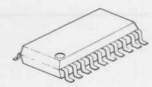
COIL NO.	F_0	Q_0	TURNS	C_0	BOTTOM VIEW
T_1 : FM IFT	10.7MHz	①-③ 90	①-③ 11T ④-⑥ 2 T Wire : 0.12mmφ UEW SUMIDA 2153-414-041	①-③ 82pF	 Bottom View
T_2 : AM IFT	455kHz	①-③ 80	①-③ 60T ④-⑥ 16 T Wire : 0.09mmφ UEW SUMIDA 2150-2173-302	①-③ 1500pF	 Bottom View
T_3 : AM DET	455kHz	①-③ 105	①-③ 127 T Wire : 0.06mmφ UEW SUMIDA 2150-2083-061	①-③ 330pF	 Bottom View
T_4 : FM DET	10.7MHz	①-③ 100	①-③ 10 T Wire : 0.12mmφ UEW SUMIDA 2153-4095-331	①-③ 150pF	 Bottom View

NARROW BAND FM IF IC

■ GENERAL DESCRIPTION

The NJM2292 is a narrow band FM IF IC designed for use in cordless telephones and amature radios, etc...It contains almost all blocks of the narrow band FM IF system-a mixer, an IF amplifier, an RSSI and a Quadrature detector, for example. It features low supply current to make a sharp reduction of total power consumption possible.

■ PACKAGE OUTLINE



NJM2292V

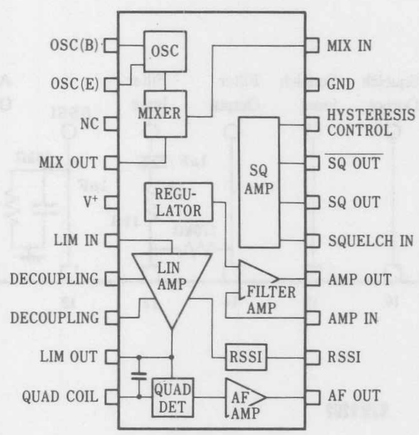
■ FEATURES

- Low Operating Voltage (1.8 ~ 7.0V)
- Low Operating Current (20mA typ. @V^+=2.4V)
- Maximum input frequency (100MHz)
- A ceramic discriminator is available
- Package Outline SSOP20
- Bipolar Technology

■ APPLICATIONS

- Amature radios
- Cordless telephones, etc.

■ PIN CONFIGURATION



NJM2292V

■ MAXIMUM ABSOLUTE RATINGS

(Ta=25℃)

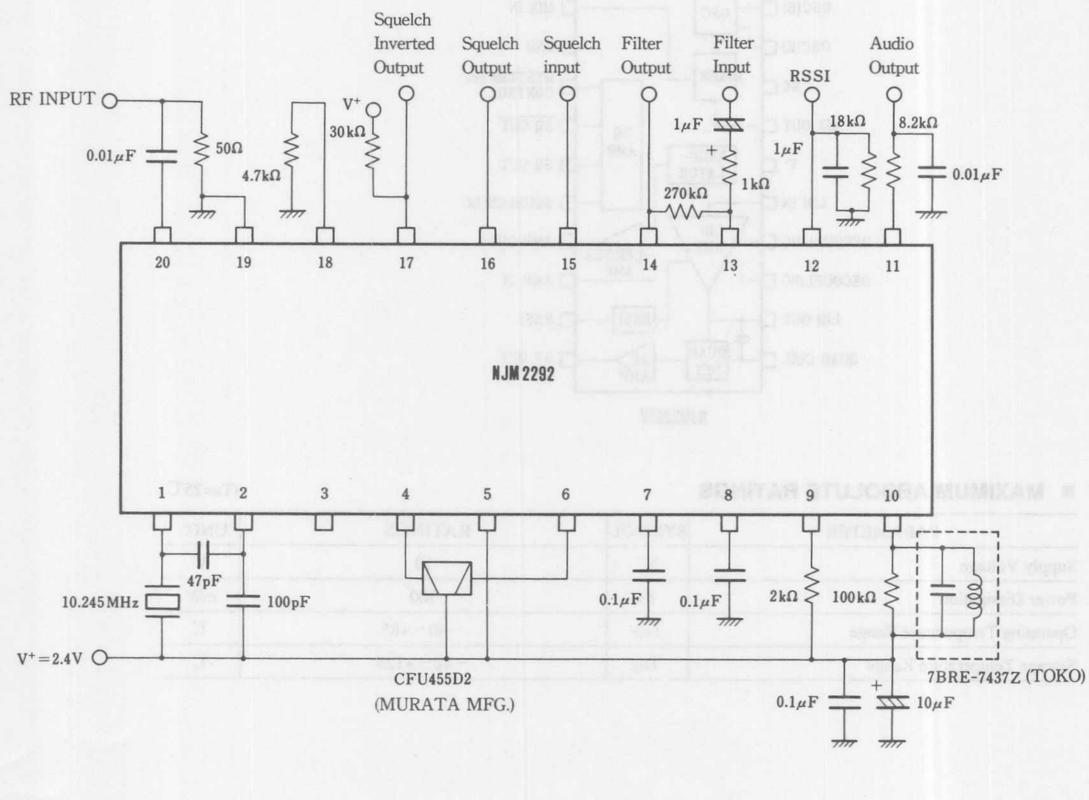
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	10	V
Power Dissipation	P_d	300	mW
Operating Temperature Range	T_{opr}	−30 ~ +85	℃
Storage Temperature Range	T_{stg}	−40 ~ +125	℃

■ ELECTRICAL CHARACTERISTICS

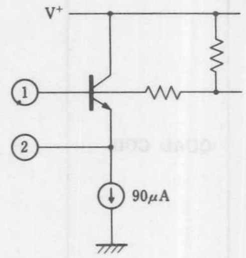
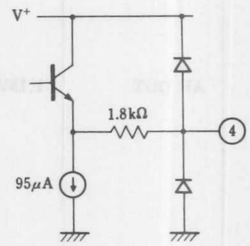
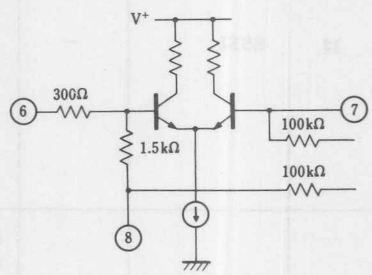
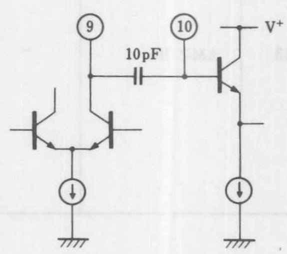
(V^+=2.4V, fc=21.7MHz, fmod=1kHz 1mV, fdev=±3kHz, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	No signal, Squelch off		2.0	2.7	mA
Mixer						
Gain	G_{MIX}		20	25		dB
Input resistance	R_{MIX}		2.7	3.6	4.5	kΩ
Limiting sensitivity	LIMIT	−3dB limiting		3.0		μV_{rms}
Audio output voltage	V_{OUT}		50	70		mV_{rms}
Filter amplifier gain	A_f	V_i =1mV_{rmsy}, 1kHz	45	48		dB
Filter amplifier output voltage	V_{ref}		0.75	0.9	1.05	V
RSSI maximum output voltage	V_{RMAX}	R_{rs}=18kΩ, IF_{in}=100mV_{rms}	0.65	0.9	1.2	V
RSSI minimum output voltage	V_{RMIN}	R_{rs}=18kΩ, NO signal			0.5	V
Squelch Hysteresis	Hys	R_{hys}=4.7kΩ	30	80	105	mV
Squelch output voltage High level	S_{PHI}		1.0	1.4	1.8	V
Low level	S_{PLO}				0.2	V
Squelch inverted output voltage High level	S_{NHI}	30kΩ pull up	2.2			V
Low level	S_{NLO}	30kΩ pull up			0.2	V

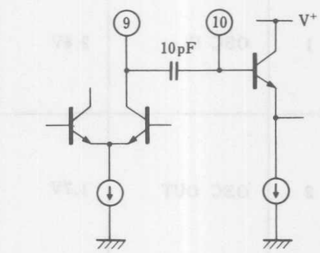
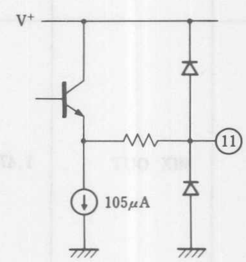
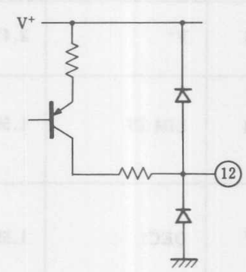
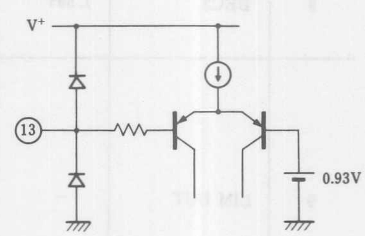
■ TEST CIRCUIT



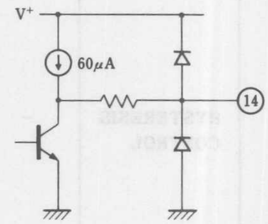
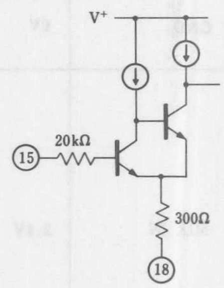
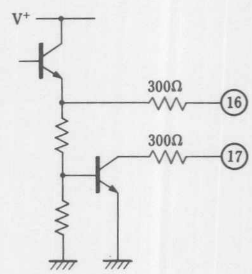
■ TERMINAL FUNCTION (V⁺=2.4V)

PIN NO.	SYMBOL	PIN VOLTAGE (typ.)	FUNCTION	EQUIVARENT CIRCUIT
1	OSC IN	2.4V	These terminals are connected with a crystal resonator to construct a colpitts circuit.	
2	OSC OUT	1.7V		
3	NC		No connection.	
4	MIX OUT	1.47V	Amixer output.	
5	V⁺	2.4V	Supply voltage.	
6	LIM IN	1.59V	A limiter input and decoupling terminals. The 7 and 8 pins are connected with about 100μF capacitors. (ESD protection diodes are connected internally with each terminal.)	
7	DEC1	1.59V		
8	DEC2	1.59V		
9	LIM OUT	–	A limiter output	

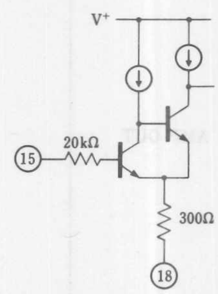
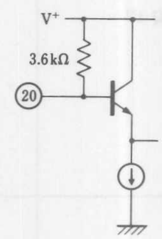
■ TERMINAL FUNCTION (V$^+$=2.4V)

PIN NO.	SYMBOL	PIN VOLTAGE (typ.)	FUNCTION	EQUIVARENT CIRCUIT
10	QUAD COIL	–	A quadrature detector input.	
11	AF OUT	1.18V	The output of the FM demodulated signal.	
12	RSSI	–	An RSSI output. The output current signal is in logarithmic proportion to the input signal.	
13	AMP IN	–	An operational amplifier inverted input.	

■ TERMINAL FUNCTION (V⁺=2.4V)

PIN NO.	SYMBOL	PIN VOLTAGE (typ.)	FUNCTION	EQUIVARENT CIRCUIT
14	AMP OUT	–	An operational amplifier output.	
15	SQ IN	–	A squelch amplifier input. (ESD protection diodes are connected internally with this terminal.)	
16	SQ OUT	–	A squelch amplifier input. (ESD protection diodes are connected internally with this terminal.)	
17	$\overline{\text{SQ OUT}}$	–	A squelch amplifier inverted output. (ESD protection diodes are connected internally with this terminal.)	

■ TERMINAL FUNCTION $(V^+=2.4V)$

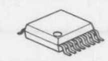
PIN NO.	SYMBOL	PIN VOLTAGE (typ.)	FUNCTION	EQUIVARENT CIRCUIT
18	HYSTERESIS CONTROL	–	A hysteresis control terminal. (ESD protection diodes are connected internally with this terminal.)	
19	GND	0V	Ground.	
20	MIX IN	2.4V	A mixer input.	

FM IF IC FOR PAGER

■ GENERAL DESCRIPTION

NJM2294 is a super low current FM IF IC for pagers. It includes almost all functions of the paging IF system. In those functions, the RSSI function can be used for automatic gain control. When the electric field strength is high, the RSSI output signal can control the attenuation of an RF amplifier to improve the received condition.

■ PACKAGE OUTLINE



NJM2294V

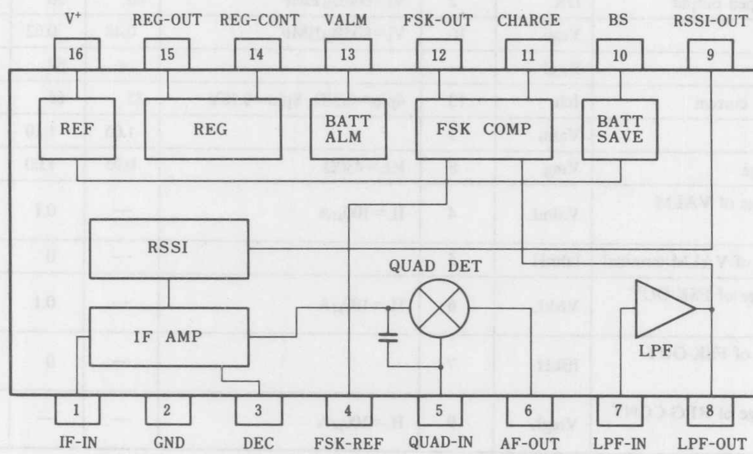
■ FEATURES

- Super low Operating Current (600 μA)
- Low Operating Voltage (1.1～4.0V)
- RSSI (Received Signal Strength Indicator)
- FSK wave shaper
- Battery check alarm function (Alarm Voltage=1.1V typ.)
- Battery saving function
- A high output current voltage regurator with an external transistor (1.1V typ.)
- A ceramic discriminator is available.
- Package Outline SSOP16
- Bipolar Technology

■ RECOMMENDED OPERATIONAL CONDITION

- Operating Voltage V^+ 1.1～4.0V

■ PIN CONFIGURATION



NJM2294V

■ MAXIMUM ABSOLUTE RATINGS

(Ta=25℃)

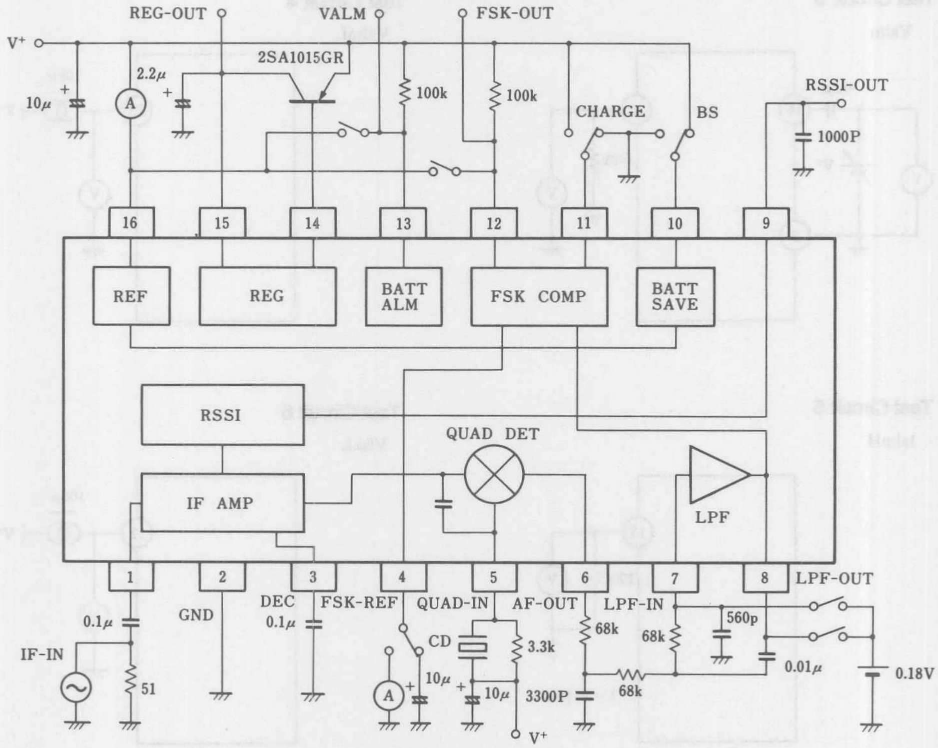
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	5	V
Power Dissipation	P_d	300	mW
Operating Temperature Range	T_{opr}	−20〜+75	℃
Storage Temperature Range	T_{stg}	−40〜+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=14V, fi=455kHz, f_{mod}=600Hz, f_{dev}=±4kHz, Ta=25℃)

PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
No signal Operating Current	I_{CCq}	11	V_i =0, 10pin=V^+	—	600	900	μA
Battery saving Operating Current	I_{CCS}	12	V_i =0, 10pin=GND	—	0	5	μA
IF amplifier input resistance	Rin	—		—	2		kΩ
S/N 1	S/N1	1	Vi=60dBμEMF	—	62	—	dB
S/N 2	S/N2	1	Vi=25dBμEMF	—	35	—	dB
−3dB limiting sensitivity	Vin(lim)	1		—	22	27	dBμEMF
Demodulated output level	Vod	1	Vi=60dBμEMF	30	46	65	mVrms
AM rejection ratio	AMR	1	Vi=60dBμEMF, AM=30%	—	50		dB
Duty ratio of wave shaped output	DR	2	Vi=60dBμEMF	40	50	60	%
RSSI output voltage	Vrssi	10	Vi=80dBμEMF	0.48	0.62	0.76	V
RSSI output resistance	Rrssi	—		—	62	—	kΩ
Quick charge/discharge current	Ich	13	4pin=GND, 8pin=0.18V	35	65	110	μA
Alarm voltage	Valm	3		1.05	1.10	1.15	V
Regulator output voltage	Vreg	8	RL=430Ω	0.95	1.00	1.05	V
Low level output voltage of VALM terminal	ValmL	4	IL=100μA	—	0.1	0.4	V
High level leak current of VALM terminal	IalmH	5		—	0	2	μA
Low level output voltage of FSK-OUT terminal	VfskL	6	IL=100μA	—	0.1	0.4	V
High level leak current of FSK-OUT terminal	IfskH	7		—	0	2	μA
Low level output voltage of REG-CONT terminal	VregL	9	IL=100μA	—	—	0.6	V

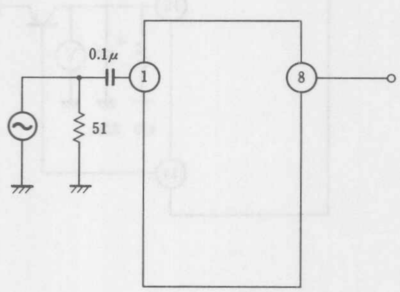
■ TEST CIRCUIT



CD:CDBC455CX (MURATA MFG.)

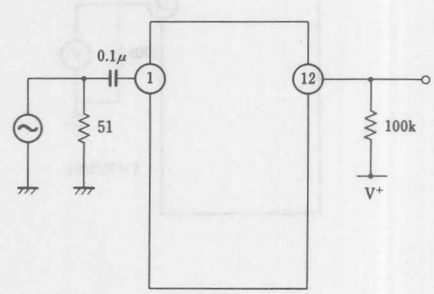
Test Circuit 1

SN1, SN2, Vi (LIM), Vod, AMR



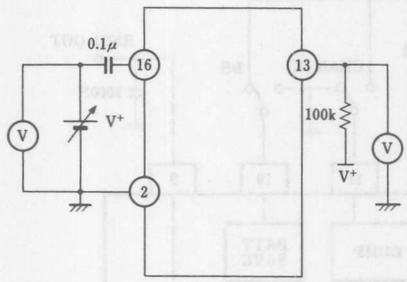
Test Circuit 2

DR



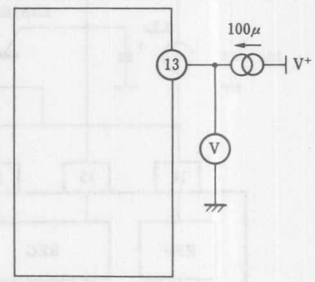
Test Circuit 3

Valm



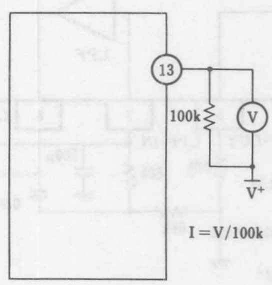
Test Circuit 4

ValmL



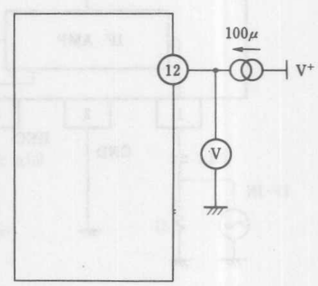
Test Circuit 5

IalmH



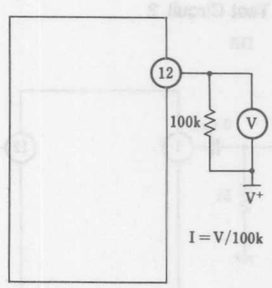
Test Circuit 6

VfskL



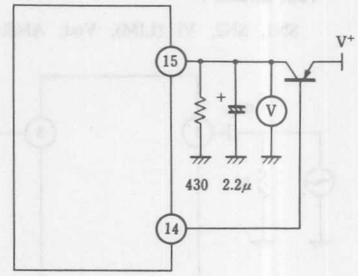
Test Circuit 7

IfskH



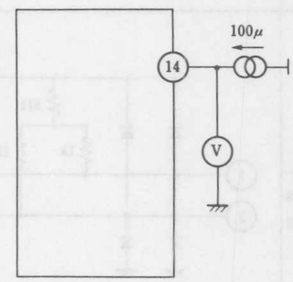
Test Circuit 8

Vreg



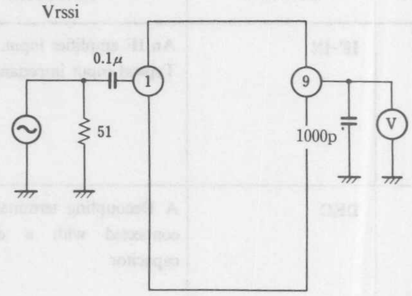
Test Circuit 9

VregL



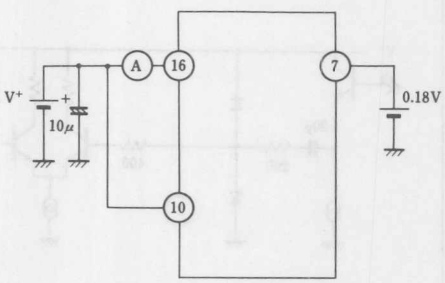
Test Circuit 10

Vrssi



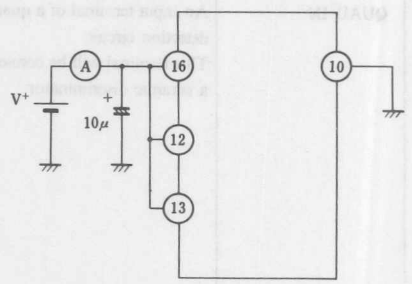
Test Circuit 11

Iccq



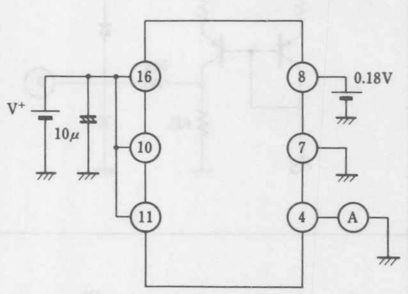
Test Circuit 12

Iccs

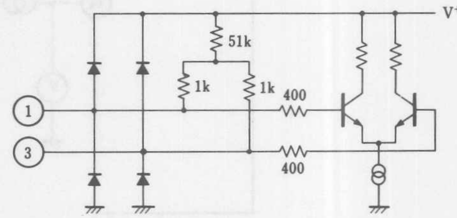
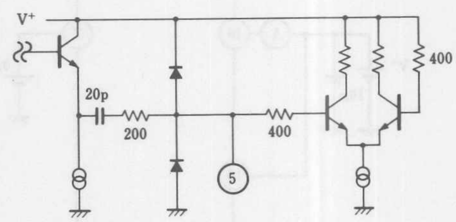
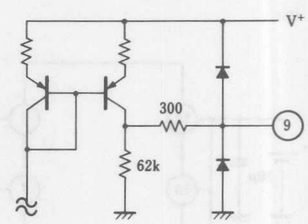
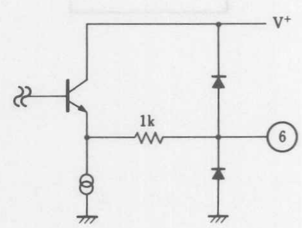


Test Circuit 13

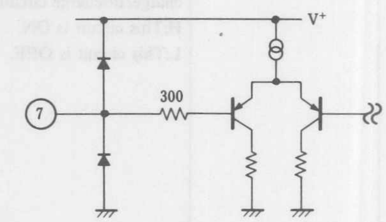
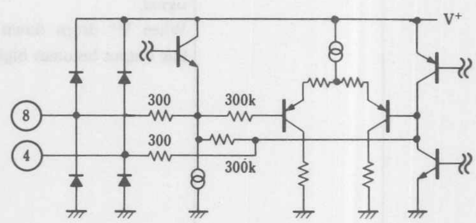
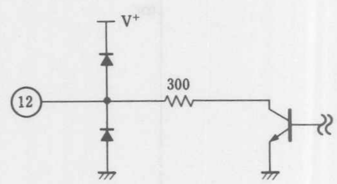
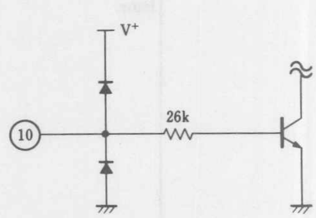
Ich



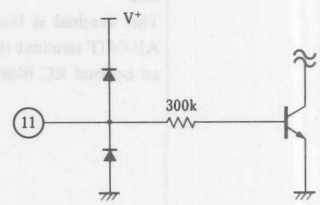
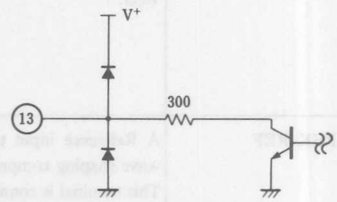
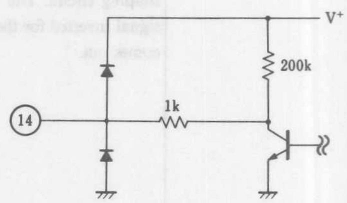
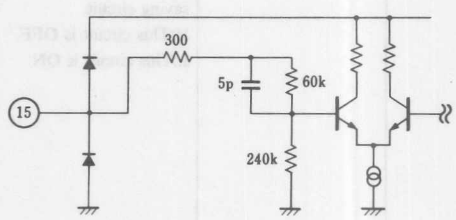
■ TERMINAL FUNCTION

PIN NO.	SYMBOL	FUNCTION	EQUIVARENT CIRCUIT
1	IF-IN	An IF amplifier input. Typical input impedance is 2kΩ.	
3	DEC	A Decoupling terminal which is connected with a decoupling capacitor.	
2	GND	Ground	
5	QUAD-IN	An input terminal of a quadrature detection circuit. This terminal will be connect with a ceramic discriminator.	
9	RSSI OUT	An RSSI Output. This voltage level is in logarithmic proportion to the input signal level.	
6	AF-OUT	An FM demodulated signal output.	

■ TERMINAL FUNCTION

PIN NO.	SYMBOL	FUNCTION	EQUIVARENT CIRCUIT
7	LPF-IN	An input terminal of a low pass filter. This terminal is biased from the AF-OUT terminal (6pin) through an external RC filter.	
8	LPF-OUT	An output terminal of a low pass filter.	
4	FSK-REF	A Reference input terminal of a wave shaping comparator. This terminal is connected with an external capacitor.	
12	FSK-OUT	An output terminal of a wave shaping circuit. The Wave shaped signal inverted for the LPF output comes out.	
10	BS	A Control terminal of a battery saving circuit. H:This circuit is OFF. L:This circuit is ON.	

■ TERMINAL FUNCTION

PIN NO.	SYMBOL	FUNCTION	EQUIVARENT CIRCUIT
11	CHARGE	A Control terminal of a quick charge/discharge circuit. H:This circuit is ON. L:This circuit is OFF.	
13	VALM	An output terminal of the alarm signal. When V+ drops down to 1.1V, this output becomes high.	
14	REG CONT	A Control terminal of an external PNP transistor used for the regulator.	
15	REG-OUT	A Monitering terminal of the regulator.	
16	V+	Supply voltage.	

■ FSK WAVE SHAPING FUNCTION

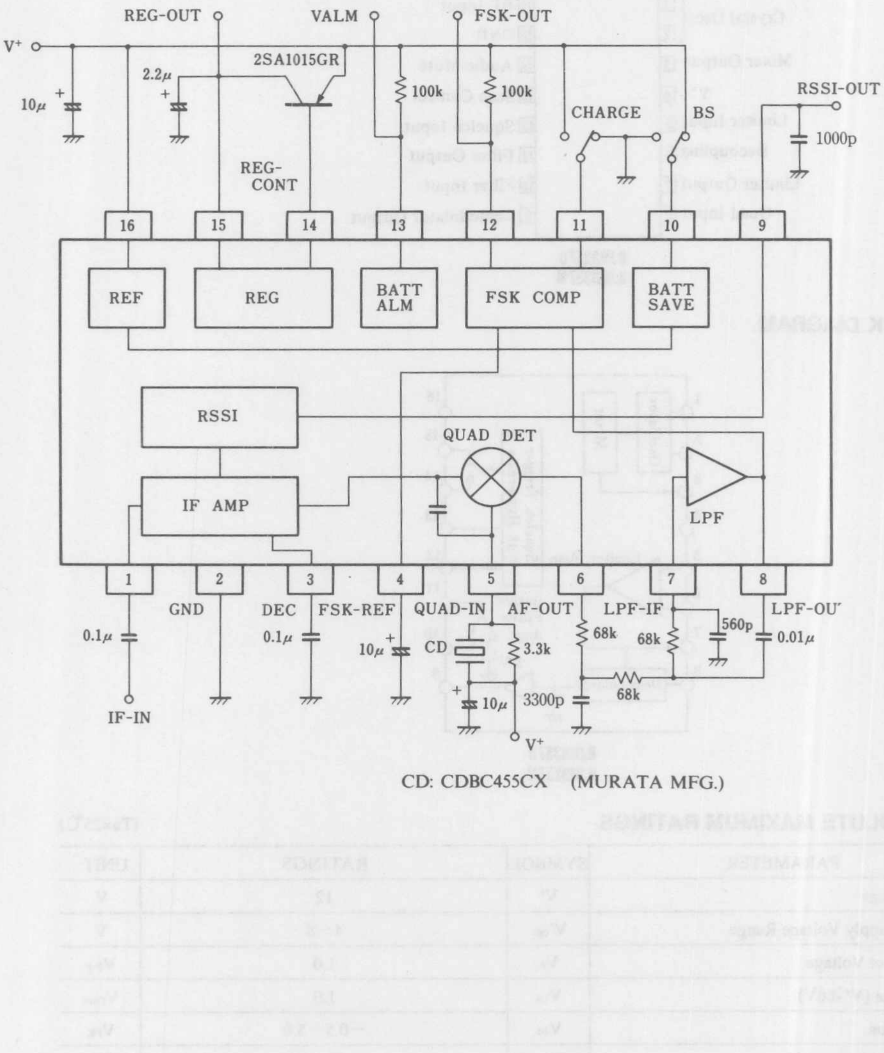
When the demodulated FSK signal is weak or noisy, the micro computer may fail to read data.
The wave shaping circuit (comparator) will change those signals to the correct logical signal to prevent the readerror.

■ QUICK CHARGE/DISCHARGE FUNCTION

The DC voltage of the FSK-REF terminal is equal to that of the demodulated FSK signal. When the battery saving state turns into the ordinary state, the FSK-REF terminal voltage will be late to come up to the reference voltage by the time constant of an external capacitor and an internal resistor, and the wave shaped data may be failed. This circuit will charge/discharge the external capacitor quickly to prevent the error.

When the DC level of the FM demudulated output changes in the operation mode of this function, the FSK-REF terminal voltage follows to the FSK demodulated output DC voltage, and the FSK output duty ratio can be constant.

■ APPLICATION CIRCUIT



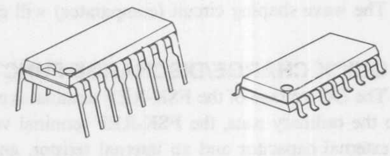
CD: CDBC455CX (MURATA MFG.)

LOW POWER NARROW BAND FM IF

■ GENERAL DESCRIPTION

The NJM3357 includes Oscillator, Mixer, Limiting Amplifier Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The NJM3357 is designed for use in FM dual conversion communication equipment.

■ PACKAGE OUTLINE

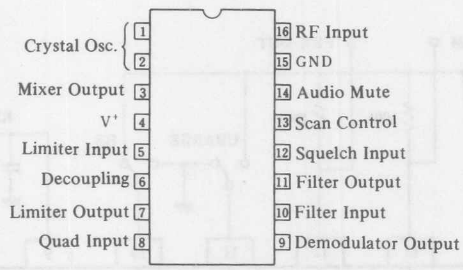


NJM3357D NJM3357M

■ FEATURES

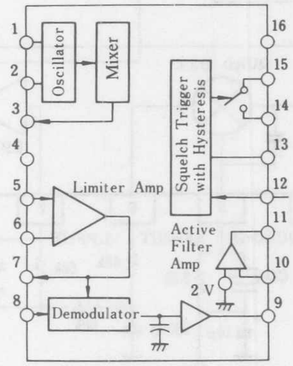
- Low Operating Current (3.0mA typ @V^+=6V)
- Minimum other parts.
- Package Outline DIP16, DMP16
- Bipolar Technology

■ PIN CONFIGURATION



NJM3357D
NJM3357M

■ BLOCK DIAGRAM



NJM3357D
NJM3357M

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

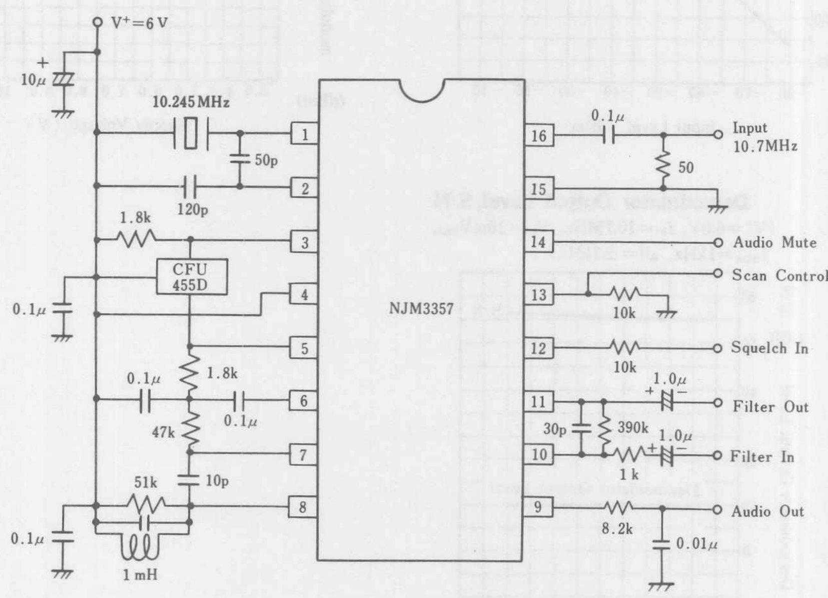
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	12	V
Operating Supply Voltage Range	V^+_{opr}	4~8	V
Detector Input Voltage	V_8	1.0	V_{P-P}
Input Voltage (V^+≧6V)	V_{16}	1.0	V_{rms}
Mute Function	V_{14}	−0.5~5.0	V_{PK}
Operating Temperature Range	T_{opr}	−20~75	℃
Storage Temperature Range	T_{stg}	−40~125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=6V, fo=10.7MHz, △f=±3.0kHz, F_{mod}=1.0kHz, Ta=25℃)

PARAMETER	PIN	MIN.	TYP.	MAX.	UNIT
Operating Current	4				
Squelch OFF		—	2.0	—	mA
Squelch ON		—	3.0	5.0	mA
Input Limitting Voltage (−3dB Limitting)	16	—	5.0	10.0	μV
Detector Output Voltage	9	—	3.0	—	V
Detector Output Impedance	—	—	400	—	Ω
Recovered Audio Output Voltage (V_{in}=10mVrms)	9	200	350	—	mVrms
Filter Gain (f=10kHz, V_{in}=5mVrms)	—	40	46	—	dB
Filter Output Voltage	11	1.8	2.0	2.5	V
Trigger Hysterisis.	—	—	100	—	mV
Mute Function Low	14	—	15	50	Ω
Mute Function High	14	1.0	10	—	MΩ
Scan Function Low (Mute OFF V_{12}=2V)	13	—	0	0.5	V
Scan Function High (Mute ON V_{12}=0V)	13	5.0	—	—	V
Mixer Conversion Gain	3	—	20	—	dB
Mixer Input Resistance	16	—	3.3	—	kΩ
Mixer Input Capacitance	16	—	2.2	—	pF

■ TEST CIRCUIT

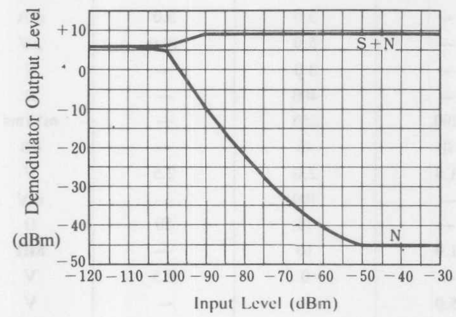


1mH: TOKO IFP455B

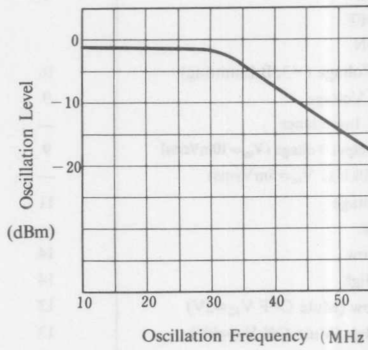
■ TYPICAL CHARACTERISTICS

Input-Output

($V^+=6.0V$, $f_{in}=10.7MHz$, $f_{mod}=1kHz$, $\Delta f=\pm 3kHz$)

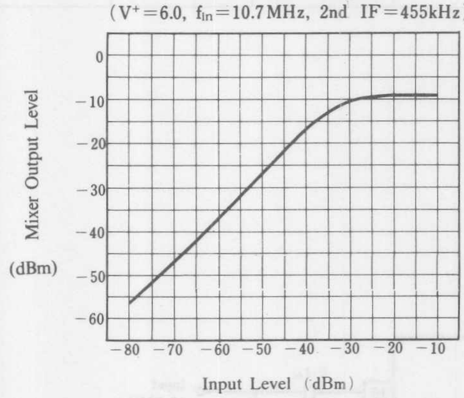


Local OSC Frequency



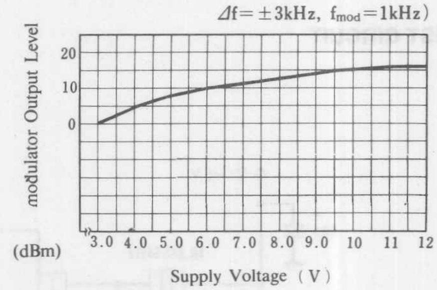
Mixer Input-Output

($V^+=6.0$, $f_{in}=10.7MHz$, 2nd IF=455kHz)



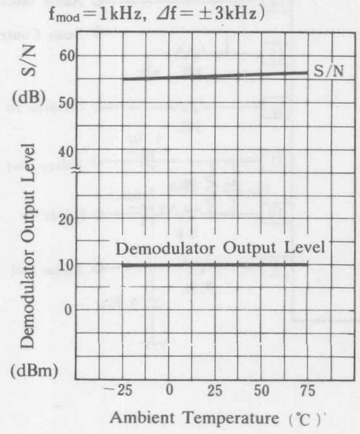
Demodulator Output Level

($f_{in}=10.7MHz$, $V_{in}=10mV_{rms}$, $\Delta f=\pm 3kHz$, $f_{mod}=1kHz$)



Demodulator Output Level, S/N

($V^+=6.0V$, $f_{in}=10.7MHz$, $V_{in}=10mV_{rms}$, $f_{mod}=1kHz$, $\Delta f=\pm 3kHz$)



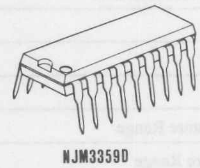
LOW POWER NARROW BAND FM IF

■ GENERAL DESCRIPTION

The NJM3359 is a low power narrow band FM detector integrated circuit for FM dual conversion of communication equipment. The NJM3359 includes oscillator, limiting amplifier, AFC circuit, quadrature detect, operational amplifier, squelch circuit, scan-control and muting switch.

The NJM3359 is a circuit of NJM3357 plus one stage limiting IF amplifier and AFC output terminal.

■ PACKAGE OUTLINE



NJM3359D

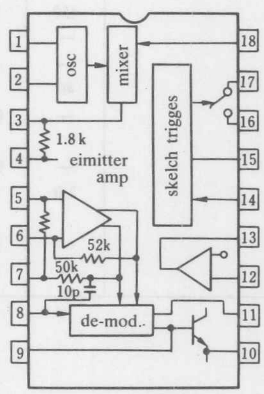
■ FEATURES

- Low Operating Current (3.6mA typ @V^+=6V)
- Input Limiting Voltage (2.0 μVrms typ @ −3dB)
- Minimum other parts.
- Package Outline DIP18
- Bipolar Technology

■ RECOMMENDED OPERATIONAL CONDITION

- Operating Voltage 4~9V

■ PIN CONFIGURATION



NJM3359D

PIN FUNCTION

Pin No.

1. crystal
2. crystal
3. mixer output
4. V^+
5. limitter input
6. de-coupling
7. de-coupling
8. detector input
9. de-modulator input
10. de-modulator output
11. AFC
12. filter input
13. filter output
14. skelch input
15. scan, control
16. audio muting
17. GND
18. RF input

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

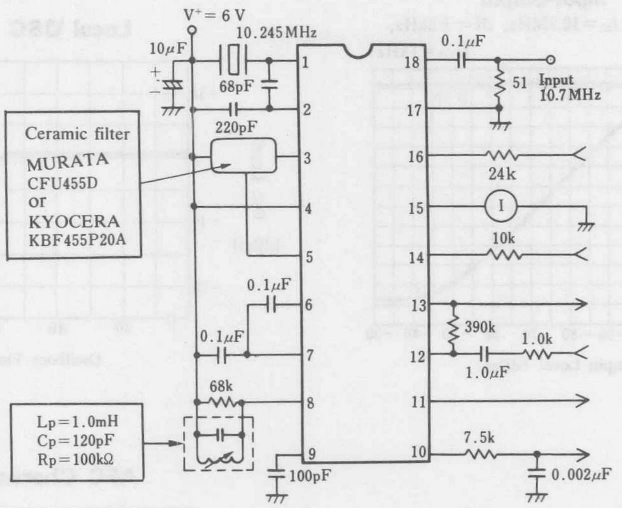
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	12	V
Input Voltage	V_{18}	1.0	V_{rms}
Muting Function	V_{16}	−0.7～12	V_{PK}
Operating Temperature Range	T_{opr}	−20～75	℃
Storage Temperature Range	T_{stg}	−40～125	℃

■ ELECTRICAL CHARACTERISTICS

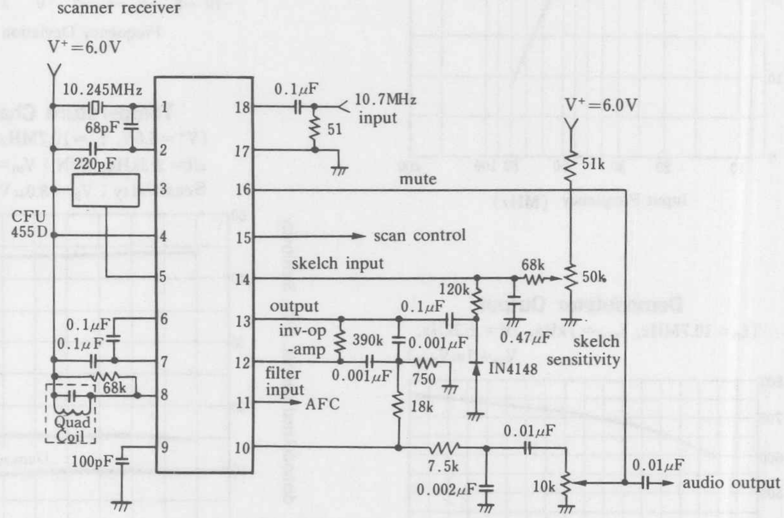
(V^+=6V, fo=10.7MHz, △f=±3.0kHz, f_{mod}=1.0kHz, Ta=25℃)

PARAMETER	PIN	MIN.	TYP.	MAX.	UNIT
Operating Current	P_{IN} 4, 8				
Squelch OFF		—	3.6	6.0	mA
Squelch ON		—	5.4	7.0	mA
Input Sensitivity (S/N: 20dB)		—	8.0	—	μVrms
Input Limitting Voltage (−3dB)		—	2.0	—	μVrms
Mixer Voltage Gain	$P_{IN}18 – P_{IN}3$ Open	—	33	—	dB
Mixer Intercept Point	50Ω input	—	−1.0	—	dBm
Mixer Input Resistance		—	3.6	—	kΩ
Mixer Input Capacitance		—	2.2	—	pF
Recovered Audio Output Voltage	$P_{IN}10$, V_{IN}=1.0mVrms	450	700	—	mVrms
Detector Center Frequency Slope	$P_{IN}10$	—	0.3	—	V/kHz
AFC Center Frequency Slope	$P_{IN}11$, $R_L=\infty$	—	12	—	V/kHz
Filter Gain	f_{in}=10kHz, V_{IN}=5mV	40	51	—	dB
Squelch Threshold Voltage	$P_{IN}14$, 10kΩ	—	0.62	—	V_{dc}
Scan Control Current	$P_{IN}15$				
	$P_{IN}14$ – High	—	0.01	1.0	μA
	– Low	2.0	2.4	—	mA
Mute Switch Impedance	$P_{IN}16$ – GND				
	$P_{IN}14$ – High	—	5.0	10	Ω
	– Low	—	1.5	—	MΩ

■ TEST CIRCUIT



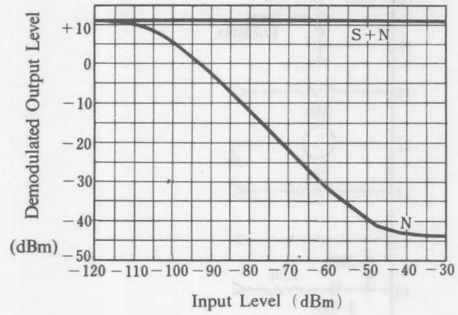
■ APPLICATION EXAMPLE



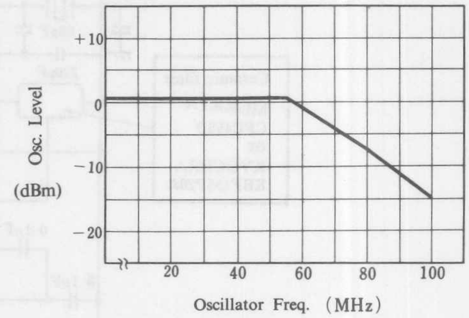
■ TYPICAL CHARACTERISTICS

Input-Output

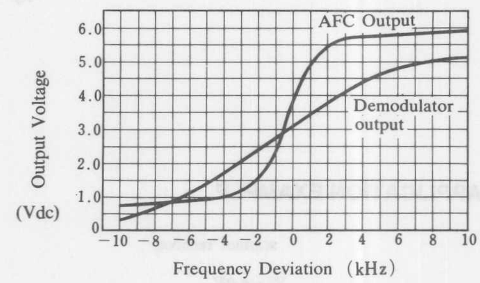
(V+=6.0V, f_{in}=10.7MHz, Δf=±3kHz, f_{mod}=1kHz)



Local OSC Frequency

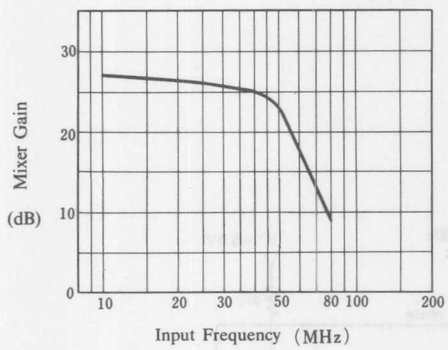


AFC Characteristics



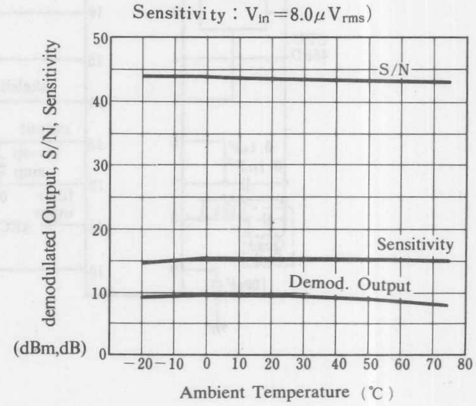
Mixer Gain vs. Input Frequency

(2nd IF=455kHz, adjust Local OSC frequency)



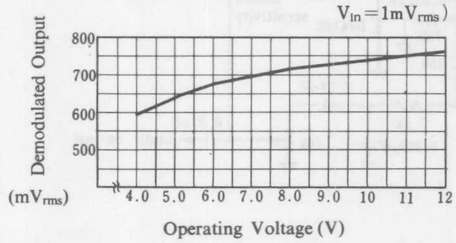
Temperature Characteristics

(V+=6.0V, f_{in}=10.7MHz, f_{mod}=1kHz, Δf=±3kHz, S/N : V_{in}=1mV_{rms}, Sensitivity : V_{in}=8.0μV_{rms})



Demodulator Output

(f_{in}=10.7MHz, f_{mod}=1kHz, Δf=±3kHz, V_{in}=1mV_{rms})



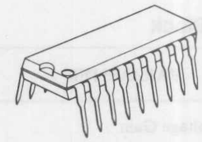
FDD READ AMPLIFIER SYSTEM

■ GENERAL DESCRIPTION

The NJM3470/3470A are monolithic read amplifier systems for obtaining digital signal from floppy disk storage.

The NJM3470/3470A are designed to get pulse output signal produced by the magnetic head amp of the input signal. They contain amplifiers, peak detector, and pulse shape circuit. They are classified two ranks by peak shift characteristic; NJM3470(5%), NJM3470A(2%)

■ PACKAGE OUTLINE

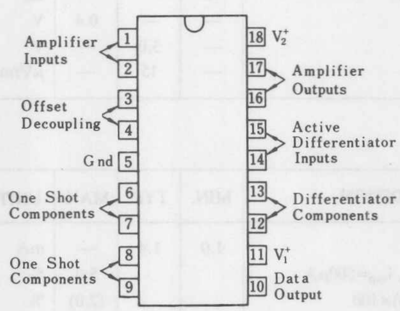


NJM3470D/3470AD

■ FEATURES

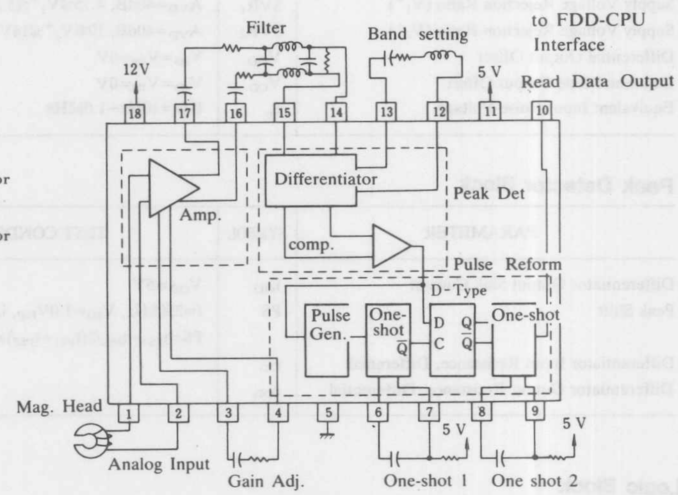
- Gain Adjastable
- Wide Bandwidth (5MHz min. @ −3dB)
- Peak Shift (A-rank : 2%max.)
- Package Outline DIP18
- Bipolar Technology

■ PIN CONFIGURATION



NJM3407D/3470AD

■ BLOCK DIAGRAM



NJM3470 BLOCK DIAGRAM
and
STANDARD OUTPUT CIRCUIT

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage I (Pin 11)	V^+	7	V
Supply Voltage II (Pin 18)	V^+_2	16	V
Input Voltage (Pin 1-2)	V_{IN}	−0.2〜7.0	V
Output Voltage (Pin 10)	V_O	−0.2〜7.0	V
Operating Temperature Range	T_{opr}	−20〜75	℃
Storage Temperature Range	T_{stg}	−40〜125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V^+_1=5V, V^+_2=12V) note: ( ) apply to A-rank.

Amplifier Block

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Differential Voltage Gain	A_{VD}	f=200kHz, V_{ID}=5.0mVrms	80 (100)	100 (110)	120 (120)	V/V
Input Bias Current	I_B		—	−10	−25	μA
Input Common Mode Range	V_{ICM}	THD=5%	−0.1		1.0	V
Differential Input Voltage Range	V_{ID}	THD=5%	—		25	mV_{P-P}
Output Voltage Swing Differential	V_{OD}		3.0	4.0		V_{P-P}
Output Source Current	I_{SOURCE}		—	8.0		mA
Output Sink Current	I_{SINK}		2.8	4.0	—	mA
Small Signal Input Resistance	r_i		100	250	—	kΩ
Small Signal Output Resistance	r_o		—	15	—	Ω
Bandwidth, −3.0dB	BW	V_{ID}=2.0mVrms	5.0	—	—	MHz
Common Mode Rejection Ratio	CMR	f=100kHz, A_{VD}=40dB, V_{in}=200mV_{p-p}	50	—	—	dB
Supply Voltage Rejection Ratio (V_1^+)	SVR_1	A_{VD}=40dB, 4.75≦V_1^+≦5.25V	50	—	—	dB
Supply Voltage Rejection Ratio (V_2^+)	SVR_2	A_{VD}=40dB, 10≦V_2^+≦14V	60	—	—	dB
Differential Output Offset	V_{DO}	V_{ID}=V_{IN}=0V	—	—	0.4	V
Common Mode Output Offset	V_{CO}	V_{ID}=V_{IN}=0V	—	3.0	—	V
Equivalent Input Noise Voltage	e_n	BW=10Hz~1.0MHz	—	15	—	μVrms

Peak Detector Block

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Differentiator Output Sink Current	I_{OD}	V_{OD}=5V	1.0	1.4	—	mA
Peak Shift	PS	f=250kHz, V_{ID}=1.0V_{P-P}, i_{cap}=500μA PS=t_{PS1}−t_{PS2}/2(t_{PS1}+t_{PS2})×100			5.0 (2.0)	% %
Differentiator Input Resistance, Differenial	r_{ID}		—	30	—	kΩ
Differentiator Output Resistance, Differential	r_{OD}		—	40	—	Ω

Logic Block

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Timing Accuracy (mono #1)	E_{t1}	t_1=1.0μS=0.625R_1C_1+200nS R_1=6.4kΩ C_1=200pF (accuracy: R_1, C_1) 1.5kΩ≦R_1≦10kΩ 150pF≦C_1≦680pF	85	—	115	%
Timing Accuracy (mono #2)	t_2		150		1000	nS
Timing Accuracy (mono #2)	E_{t2}	t_2=200nS=0.625R_2C_2 R_2=1.6kΩ C_2=200pF (accuracy; R_2, C_2) 1.5kΩ≦R_2≦10kΩ 100pF≦C_2 800pF	85	—	115	%

OTHERS 7

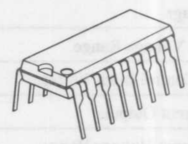
8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

■ GENERAL DESCRIPTION

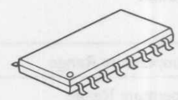
NJMDAC-08C series are 8-bit monolithic multiplying digital to analog converters with very highspeed performance. Open collector output provides dual complementary current outputs increasing versatility in application.

Adjustable threshold logic input voltage through V_{LC} pin, can be connected to various type of digital IC products.

■ PACKAGE OUTLINE



NJMDAC-08DC

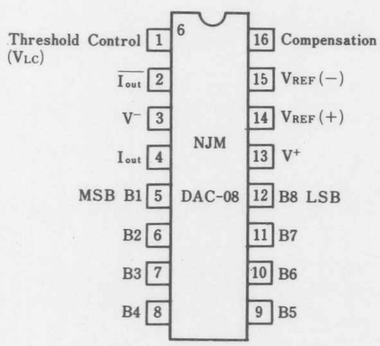


NJMDAC-08MC

■ FEATURES

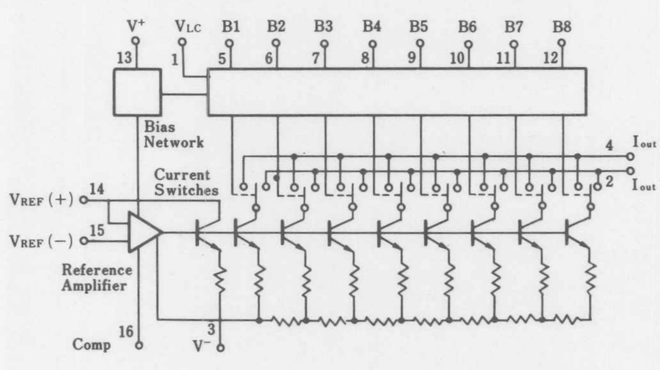
- Resolution (8bit)
- Settling Time (85ns)
- Linearity Error (±0.1%FS MAX (NJM DAC-08H))
- Full Scale Current Temperature Drift (50ppm/℃ MAX (NJM DAC-08H/E))
- Wide Operating Voltage (±5V ~ ±18V)
- Wide Output Voltage Range (−10V ~ +18V)
- Wide Range Adjustable Threshold Logic Input (−10V ~ + 13.5V(V^+/V^- =±15V))
- Multiplying operations can be performed
- Package Outline DIP16, DMP16
- Bipolar Technology

■ PIN CONFIGURATION



NJMDAC-08DC
NJMDAC-08MC

■ BLOCK DIAGRAM



■ **ABSOLUTE MAXIMUM RATINGS** (Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply voltage	$V^+ - V^-$	36	V
Logic Input Voltage Range	V_I	$V^- \sim V^- + 36$	V
Threshold Control Input Voltage	V_{LC}	$V^- \sim V^+$	V
Analog Current Outputs	I_O	4.2	mA
Reference Input Voltage Range	V_{REF}	$V^- \sim V^+$	V
Reference Input Differential Voltage	$V_{REF(+)} - V_{REF(-)}$	± 18	V
Reference Input Current	I_{REF}	5.0	mA
Power Dissipation	P_D	(DIP16) 500	mW
		(DMP16) 300	mW
Operating Temperature Range	T_{opr}	$-20 \sim +75$	℃
Storage Temperature Range	T_{stg}	$-40 \sim +125$	℃

■ ELECTRICAL CHARACTERISTICS

($V^{+}=\pm 15V$, $I_{REF}=2.0mA$, $Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Resolution			8	8	8	Bit
Monotonicity			8	8	8	Bit
Nonlinearity	NL				±0.39	%FS
*1 Settling Time	t_s	To ±1/2LSB,all bits switched ON or OFF		85	150	ns
*1 Propagation Delay	t_{PLH} t_{PHL}	All bits switched		35	60	ns
*1 Full Scale Temperature Coefficient	TCI_{FS}			±10	±80	ppm/℃
Output Voltage Compliance	V_{OC}	$\Delta I_{FS}<1/2$ LSB $R_{OUT}>20M\Omega$ typ.	−10		+18	V
Full Scale Current	I_{FS4}	$V_{REF}=10.000V$ $R_{14}, R_{15}=5.000k\Omega$	1.94	1.99	2.04	mA
Full Scale Symmetry	I_{FSS}	$I_{FS4}-I_{FS2}$		±2.0	±16.0	μA
Zero Scale Current	I_{ZS}			0.2	4.0	μA
Output Current Range	I_{OR1}	$V_{REF}=15V, V^{-}=10V$ $R_{14,15}=15.000k\Omega$	2.1			mA
	I_{OR2}	$V_{REF}=25V, V^{-}=12V$	4.2			mA
Logic Input Level "0"	V_{IL}	$V_{LC}=0V$			0.8	V
〃 "1"	V_{IH}	$V_{LC}=0V$	2.0			V
Logic Input Current "0"	I_{IL}	$V_{LC}=0V, V_{IN}=-10V\sim+0.8V$		−2.0	−10	μA
"1"	I_{IH}	$V_{LC}=0V, V_{IN}=2V\sim18V$		0.002	10	μA
Logic Input Swing	V_{IS}		−10		+18	V
Logic Threshold Range	V_{TH2}	―――	−10		+13.5	V
Reference Bias Current	I_{IS}			−1.0	−3.0	μA
*1 Reference Input Slew Rate	dI/dt		4.0	8.0		mA/μs
*2 Power Supply Sensitivity	$PSSI_{FS}$	$V^{-}=4.5V\sim18V, I_{REF}=1.0mA$		±0.0003	±0.01	%/%
	$PSSI_{FS}$	$V^{-}=-4.5V\sim18V, I_{REF}=1.0mA$		±0.002	±0.01	%/%
*3 Operating Current	I^{+}	$V^{\pm}=\pm5V, I_{REF}=1.0mA$		2.3	3.8	mA
	I^{-}	〃		−4.3	−5.8	mA
	I^{+}	$V^{+}=5V, V^{-}=-15V$		2.4	3.8	mA
	I^{-}	〃		−6.4	−7.8	mA
	I^{+}	―――		2.5	3.8	mA
	I^{-}	―――		−6.5	−7.8	mA

*1 Guaranteed by design

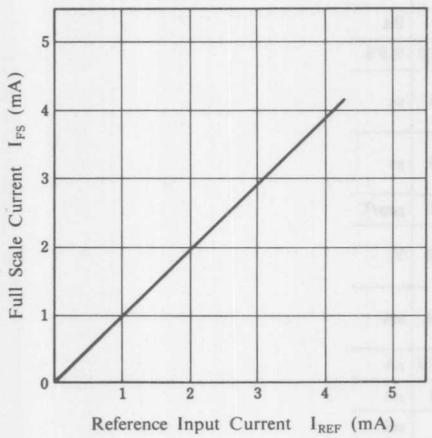
*2 Caluculation formula $PSSI_{FS}=\left(\frac{|\Delta I_{FS}|}{I_{FS}}\times100\right)\div\left(\frac{18-4.5}{15}\right)\times100$

*3 Caluculation formula $P_D=I^{+}\times(V^{+}-V^{-})+2I_{REF}\times|V^{-}|$

■ TYPICAL CHARACTERISTICS

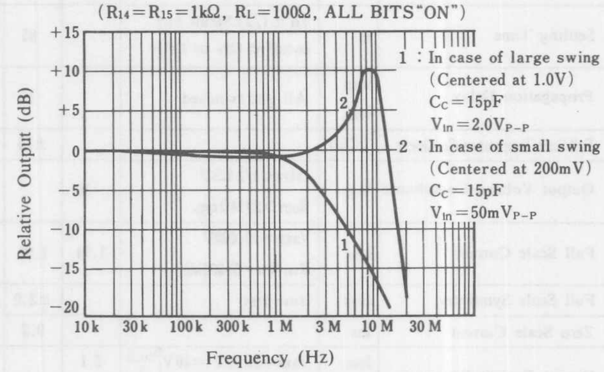
Full Scale Current vs. Reference Input Current

(All bits on, $V^- = -15V$)

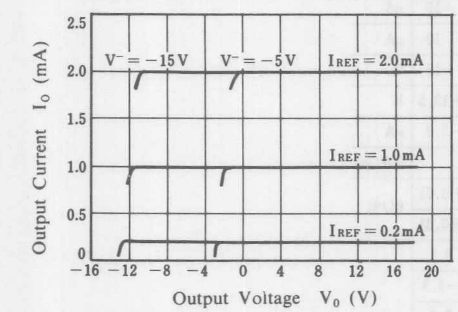


Reference Input Frequency Respons

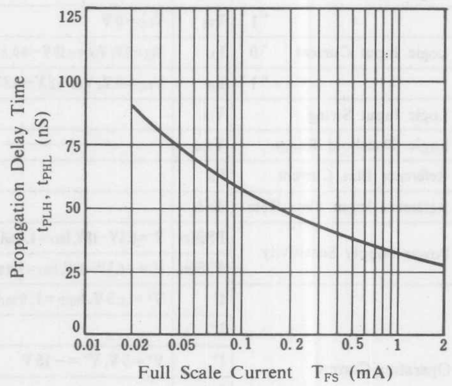
($R_{14} = R_{15} = 1k\Omega$, $R_L = 100\Omega$, ALL BITS "ON")



Output Current vs. Output Voltage

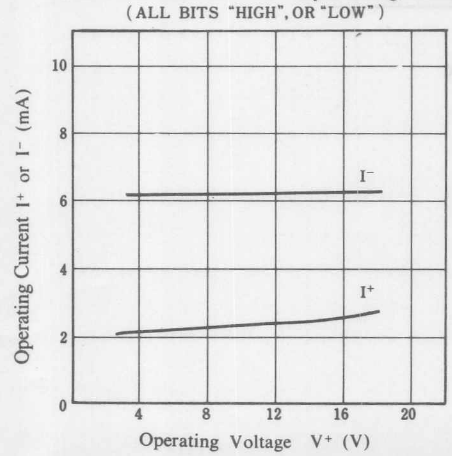


Propagation Delay Time vs. Full Scale Current



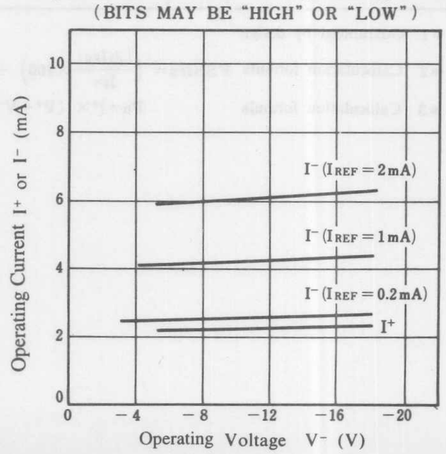
Operating Current vs. Operating Voltage

(ALL BITS "HIGH", OR "LOW")



Operating Current vs. Operating Voltage

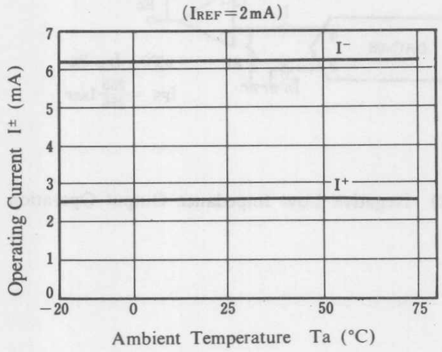
(BITS MAY BE "HIGH" OR "LOW")



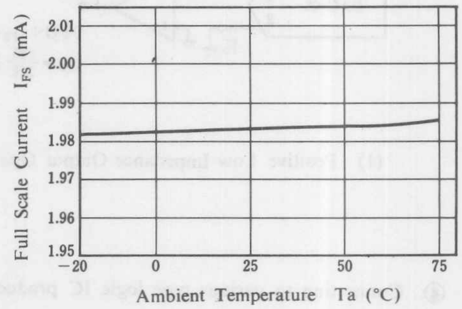
■ TYPICAL CHARACTERISTICS

Operating Current vs. Ambient Temperature

(I_{REF}=2mA)

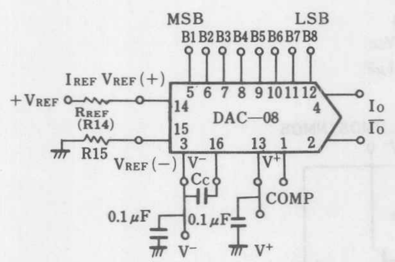


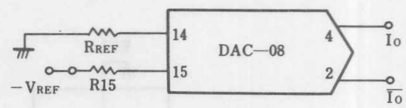
Full Scale Current vs. Ambient Temperature



■ TYPICAL APPLICATION

① Connecting Reference Voltage

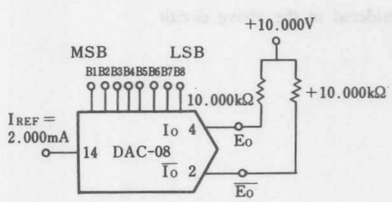


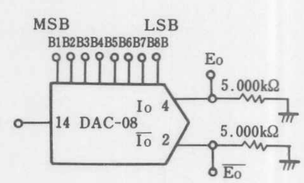


① Positive Reference Voltage
Minimum Compensation Capacitance
$C_C = R_{REF}(k\Omega) \times 15(pF)$

② Negative Reference Voltage
Recommended C_C Value
(When V_{REF} is DC)

② Connecting Output Circuit





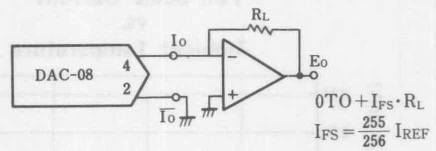
	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS FULL RANGE	1	1	1	1	1	1	1	1	− 9.920	÷10.000
POS FULL RANGE−LSB	1	1	1	1	1	1	1	0	− 9.840	÷ 9.920
ZERO SCALE÷LSB	1	0	0	0	0	0	0	1	− 0.050	÷ 0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	÷ 0.050
ZERO SCALE−LSB	0	1	1	1	1	1	1	1	÷ 0.080	0.000
NEG FULL SCALE÷LSB	0	0	0	0	0	0	0	1	÷ 9.920	− 9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	÷10.000	− 9.920

(1) Basic Bipolar Output Operation

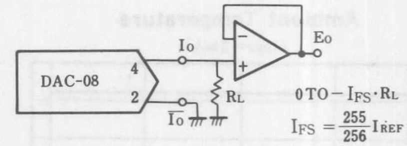
	B1	B2	B3	B4	B5	B6	B7	B8	I_{nmA}	I_{nmA}	E_O	$\overline{E_O}$
FULL RANGE	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	−0.000
HALF SCALE÷LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
HALF SCALE−LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
ZERO SCALE÷LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	1.992	−0.000	−9.950

(2) Basic Unipolar Negative Operation

③ Connecting Output Buffer Amp.

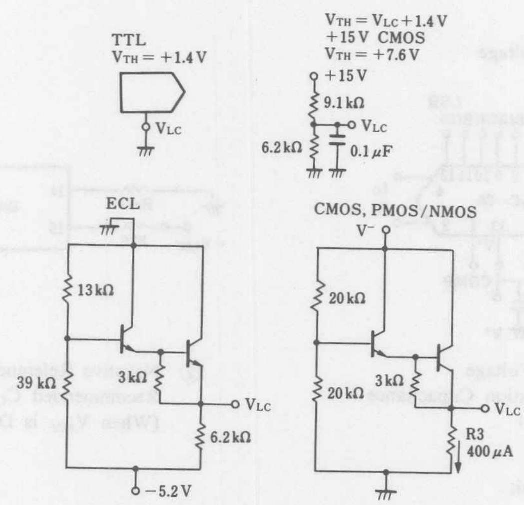


(1) Positive Low Impedance Output Operation



(2) Negative Low Impedance Output Operation

④ Connecting to various type logic IC products



V_{TH} temperature compensation is considered in the above circuit

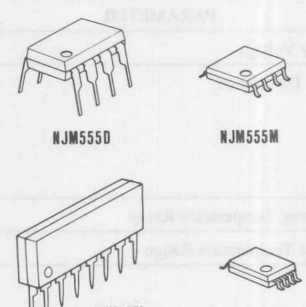
TIMER

■ GENERAL DESCRIPTION

The NJM555 monolithic timing circuit is a highly stable controller capable of producing accruate time delays or oscillation. In the time delay mode, delay time is precisely controlled by only two external parts: a resistor and a capacitor. For operation as an oscillator, both the free running frequency and the duty cycle are accurately controlled by two external resistors and a capacitor.

Terminals are provided for triggering and resetting. The circuit will trigger and reset on falling waveforms. The output can source or sink up to 200mA or drive TTL circuits.

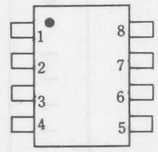
■ PACKAGE OUTLINE



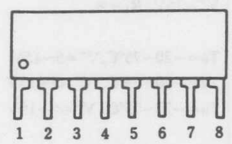
■ FEATURES

- Operating Voltage (4.5V ~ 16V)
- Less Number of External Components
- Package Outline DIP8, DMP8, SSOP8, SIP8
- Bipolar Technology

■ PIN CONFIGURATION



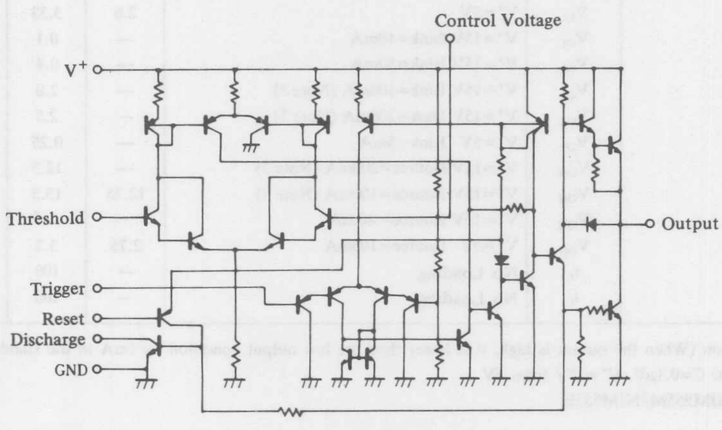
NJM555D
NJM555M
NJM555V



NJM555L

PIN FUNCTION
1. GND
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V^+

■ EQUIVALENT CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	18	V
Power Dissipation	P_D	(DIP8) 500 (DMP8) 300 (SSOP8) 250 (SIP8) 800	mW mW mW mW
Operating Temperature Range	T_{opr}	−20〜+75	℃
Storage Temperature Range	T_{stg}	−40〜+125	℃

■ ELECTRICAL CHARACTERISTICS

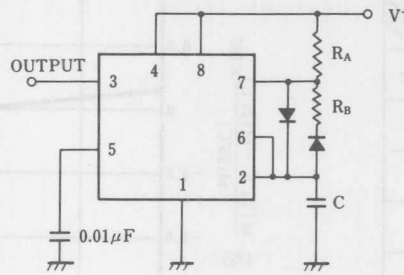
(V^+=5〜15V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		4.5	—	16	V
Operating Current (Note 1)	I_{CC}	V^+=5V, $R_L=\infty$	—	3.0	6.0	mA
Operating Current (Note 1)	I_{CC}	V^+=15V, $R_L=\infty$	—	10	15	mA
Timing Error (Note 2)						
Initial Accuracy	E_t	Ta=−20~75°C, V^+=5~15V	—	1.0	—	%
Drift with Temperature	E_t	Ta=−20~75°C, V^+=5~15V	—	50	—	ppm/°C
Drift with Supply Voltage	E_t	Ta=−20~75°C, V^+=5~15V	—	0.1	—	%/V
Threshold Voltage	V_{th}		—	2/3	—	$\times V^+$
Trigger Voltage	V_T	V^+=15V	—	5.0	—	V
Trigger Voltage	V_T	V^+=5V	—	1.67	—	V
Trigger Current	I_T		—	0.5	—	μA
Reset Voltage	V_R		0.4	0.5	1.0	V
Reset Current	I_R		—	0.1	—	mA
Threshold Current	I_{th}		—	0.1	0.25	μA
Control Voltage Level	V_{CL}	V^+=15V	9	10	11	V
Control Voltage Level	V_{CL}	V^+=5V	2.6	3.33	4.0	V
Output Voltage (Low)	V_{OL}	V^+=15V Isink=10mA	—	0.1	0.25	V
Output Voltage (Low)	V_{OL}	V^+=15V Isink=50mA	—	0.4	0.75	V
Output Voltage (Low)	V_{OL}	V^+=15V Isink=100mA (Note 3)	—	2.0	2.5	V
Output Voltage (Low)	V_{OL}	V^+=15V Isink=200mA (Note 3)	—	2.5	—	V
Output Voltage (Low)	V_{OL}	V^+=5V Isink=5mA	—	0.25	0.35	V
Output Voltage (High)	V_{OH}	V^+=15V Isource=200mA (Note 3)	—	12.5	—	V
Output Voltage (High)	V_{OH}	V^+=15V Isource=100mA (Note 3)	12.75	13.3	—	V
Output Voltage (High)	V_{OH}	V^+=15V Isource=40mA	—	5	—	V
Output Voltage (High)	V_{OH}	V^+=5V Isource=100mA	2.75	3.3	—	V
Rise Time of Output	t_r	No Loading	—	100	—	ns
Fall Time of Output	t_f	No Loading	—	100	—	ns

Note 1: Low output condition (When the output is high, it is lower than the low output condition by 1mA in the standard specification.)
Note 2: R_A, R_B=1k~100kΩ, C=0.1μF, V^+=15V from 5V
Note 3: Not specified for NJM555M/NJM555E

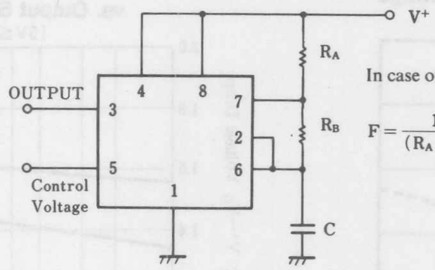
■ TYPICAL APPLICATION

(1) 50% Duty Cycle Oscillator



Duty cycle 50% at $R_A = R_B$
Due to R_A, R_B value the duty ratio becomes lower than 50%.

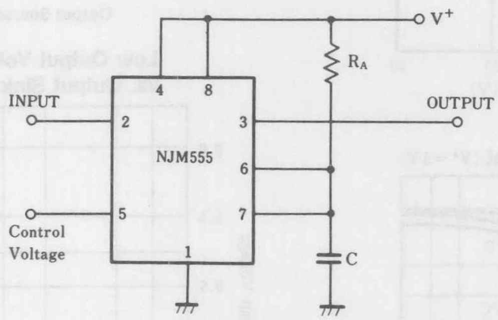
(2) Oscillatoion frequency can be changed by changing the control voltage.



In case of 5pin open

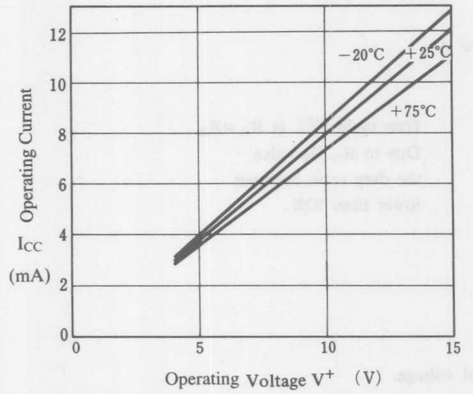
$$F = \frac{1.44}{(R_A + 2R_B) \cdot C}$$

(3) Pulse Width Modulation

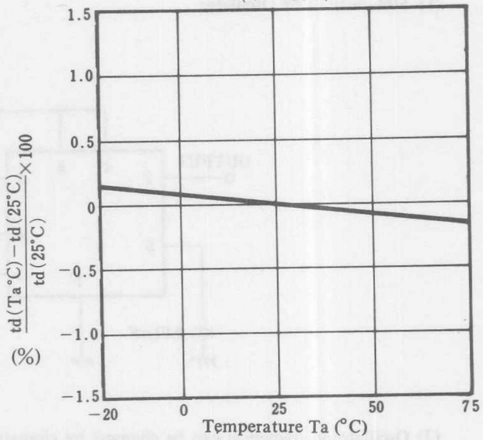


■ TYPICAL CHARACTERISTICS

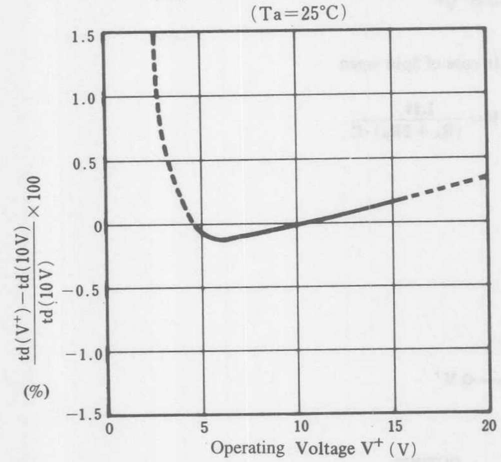
Operating Current vs. Operating Voltage
(V_{OUT}=LOW STATE)



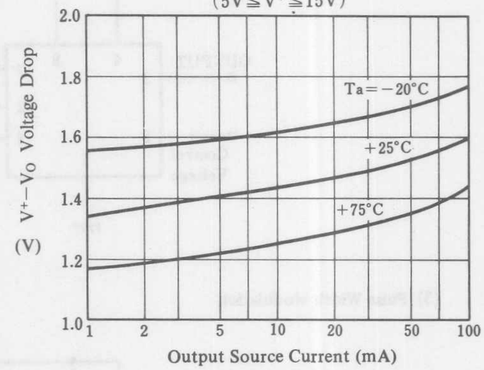
Delay Time vs. Temperature
(V^+=10V)



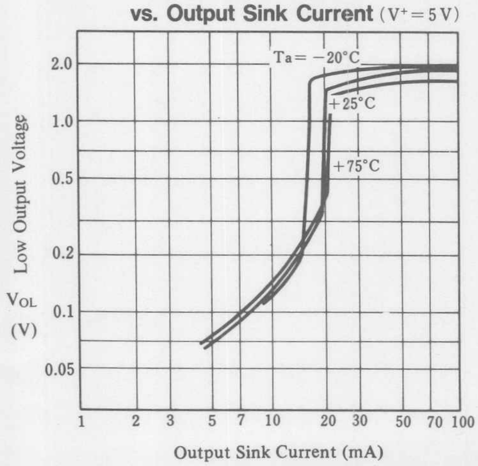
Delay Time vs. Operating Voltage
(Ta=25°C)



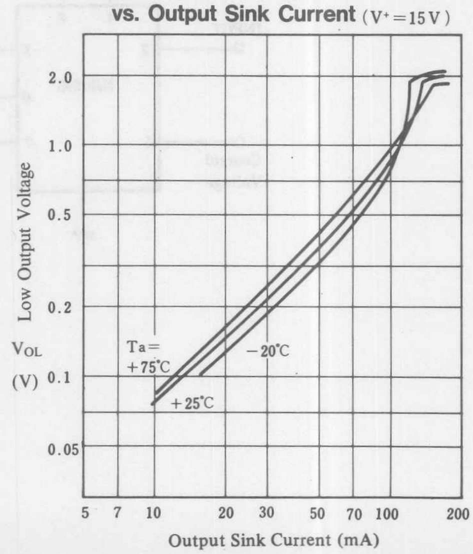
High Output Voltage Drop vs. Output Source Current
($5V \leq V^+ \leq 15V$)



Low Output Voltage vs. Output Sink Current (V^+=5V)



Low Output Voltage vs. Output Sink Current (V^+=15V)



■ TYPICAL CHARACTERISTICS

1. Monostable Operation

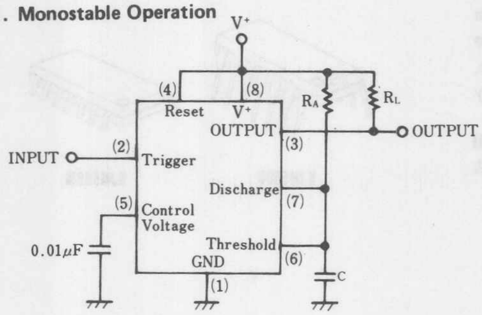


Fig. 1

2. Free Running Operation

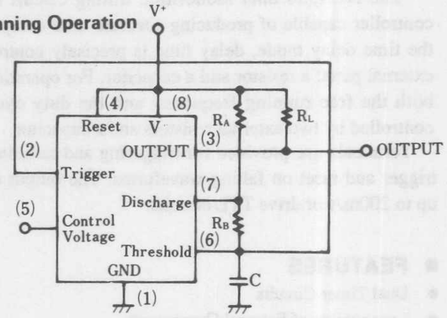


Fig. 3

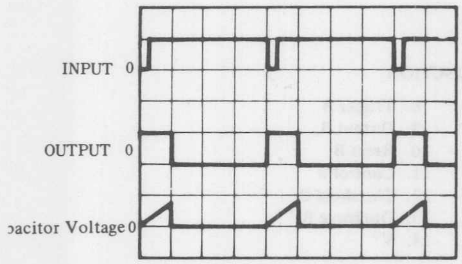


Fig.2 Wave Form

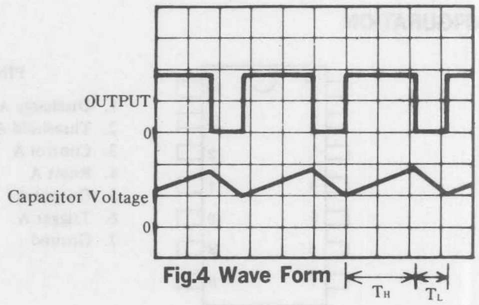
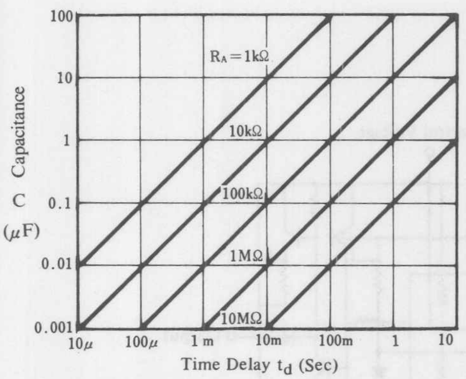
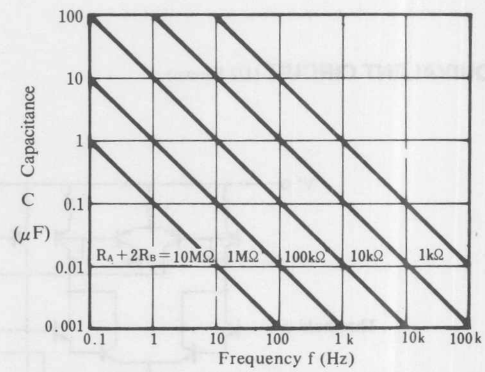


Fig.4 Wave Form



Time Delay vs. R_A, R_B and C

Fig. 2 shows a typical example of the monostable operation. $T_H = 1.1R_A \cdot C$ assuming that T_H be the time at the high output level in this figure.



Free Running Frequency vs. R_A, R_B and C

Fig. 4 shows a typical example of the free running operation.

The charge time (output High) is given by:

$$T_H = 0.693\,(R_A + R_B) \cdot C$$

And the discharge time (output Low) by:

$$T_L = 0.693 R_B \cdot C$$

The frequency of oscillation is:

$$F = \frac{1.44}{(R_A + 2R_B) \cdot C}$$

The duty cycle is:

$$D = \frac{T_H}{T_H + T_L} = \frac{R_A + R_B}{R_A + 2R_B}$$

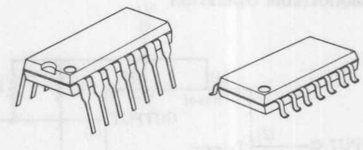
DUAL TIMER

■ GENERAL DESCRIPTION

The NJM556 dual monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode, delay time is precisely controlled by only two external parts: a resistor and a capacitor. For operation as an oscillator, both the free running frequency and the duty cycle are accurately controlled by two external resistors and a capacitor.

Terminals are provided for triggering and resetting. The circuit will trigger and reset on falling waveforms. The output can source or sink up to 200mA or drive TTL circuits.

■ PACKAGE OUTLINE



NJM556D NJM556M

■ FEATURES

- Dual Timer Circuits
- Less number of External Components
- Package Outline DIP14, DMP14
- Bipolar Technology

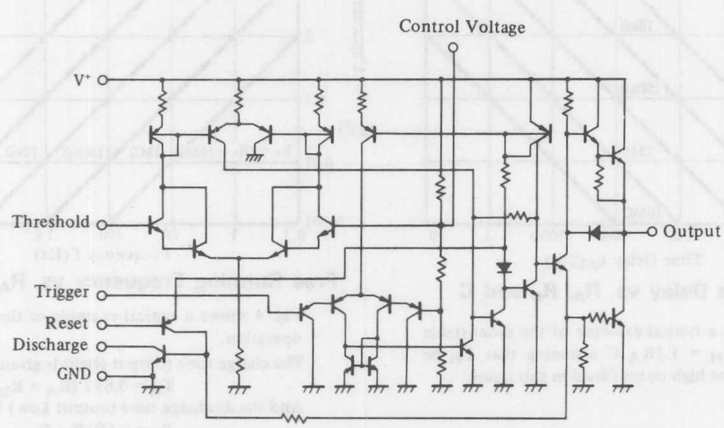
■ PIN CONFIGURATION

NJM556D
NJM556M

PIN FUNCTION

1. Discharge A
2. Threshold A
3. Control A
4. Reset A
5. Output A
6. Trigger A
7. Ground
8. Trigger B
9. Output B
10. Reset B
11. Control B
12. Threshold B
13. Discharge B
14. V^+

■ EQUIVALENT CIRCUIT (1/2 Shown)



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	18	V
Power Dissipation	P_D	(DIP14) 570 (DMP14) 700(note)	mW mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

(note) At on PC board

■ ELECTRICAL CHARACTERISTICS

(V^+=+5～+15V, Ta=25℃)

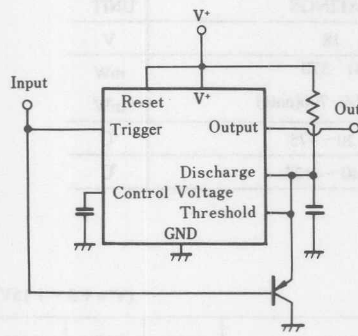
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		4.5	—	16	V
Operating Current (Note 2)	I_{CC}	V^+=5V, $R_L=\infty$ (Each Section)	—	3	6	mA
Operating Current (Note 2)	I_{CC}	V^+=15V, $R_L=\infty$ (Each Section)	—	10	14	mA
Threshold Voltage	V_{TH}		—	2/3	—	×V^+
Trigger Voltage	V_T	V^+=15V	—	5	—	V
Trigger Voltage	V_T	V^+=5V	—	1.67	—	V
Trigger Current	I_T		—	0.5	—	μA
Reset Voltage	V_R		0.4	0.7	1.0	V
Reset Current	I_R		—	0.1	—	mA
Threshold Current	I_T		—	0.03	0.1	μA
Control Voltage Level	V_{CL}	V^+=15V	9	10	11	V
Control Voltage Level	V_{CL}	V^+=5V	2.6	3.33	4	V
Output Voltage Drop (Low)	V_{OL}	V^+=15V I_{SINK}=10mA	—	0.1	0.25	V
Output Voltage Drop (Low)	V_{OL}	V^+=15V I_{SINK}=50mA	—	0.4	0.75	V
Output Voltage Drop (Low)	V_{OL}	V^+=15V I_{SINK}=100mA	—	2	2.75	V
Output Voltage Drop (Low)	V_{OL}	V^+=15V I_{SINK}=200mA	—	2.5	—	V
Output Voltage Drop (Low)	V_{OL}	V^+=5V I_{SINK}=5mA	—	0.25	0.35	V
Output Voltage Drop (High)	V_{OH}	V^+=15V I_{SOURCE}=200mA	—	12.5	—	V
Output Voltage Drop (High)	V_{OH}	V^+=15V I_{SOURCE}=100mA	12.75	13.3	—	V
Output Voltage Drop (High)	V_{OH}	V^+=15V I_{SOURCE}=40mA	—	13.5	—	V
Output Voltage Drop (High)	V_{OH}	V^+=5V I_{SOURCE}=100mA	2.75	3.3	—	V

(Note 2) Operating Current when output high typically 2mA less.

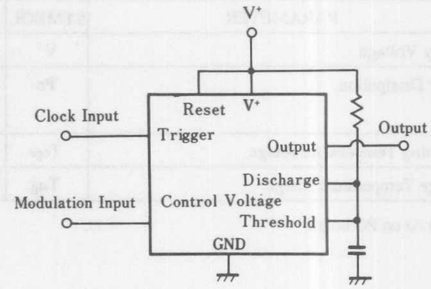
PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Timing Error	Initial Accuracy	E_{ta}	R_A, R_B=2k～100kΩ, C=0.1μF	—	2.25	—	%
(Free Running)	vs. Temperature	E_{ta}	R_A, R_B=2k～100kΩ, C=0.1μF	—	150	—	ppm/°C
(Note 3)	vs. Operating Voltage	E_{ta}	R_A, R_B=2k～100kΩ, C=0.1μF	—	0.3	—	%/Volt
Timing Error	Initial Accuracy	E_{tm}	R_A, R_B=2k～100kΩ, C=0.1μF	—	0.75	—	%
(Monostable)	vs. Temperature	E_{tm}	R_A, R_B=2k～100kΩ, C=0.1μF	—	50	—	ppm/°C
(Note 3)	vs. Operating Voltage	E_{tm}	R_A, R_B=2k～100kΩ, C=0.1μF	—	0.1	—	%/Volt
Matching Characteristics	Initial Accuracy			—	0.5	1	%
Between Each Section	vs. Temperature			—	±10	—	ppm/°C
	vs. Operating Voltage			—	0.2	0.5	%/Volt

(Note 3): Tested at V^+=+5V～+15V

■ TYPICAL APPLICATION



Missing pulse Diection Circuit

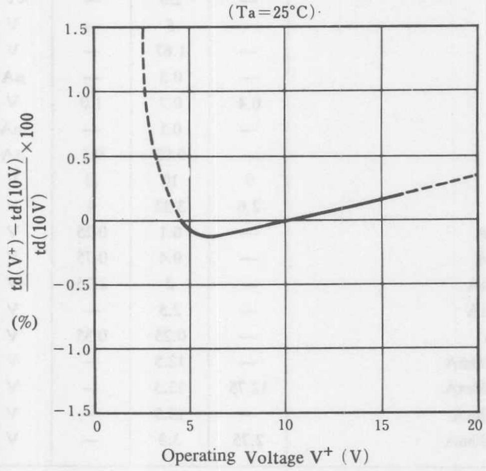


Pulse Width Moduration Circuit

■ TYPICAL CHARACTERISTICS

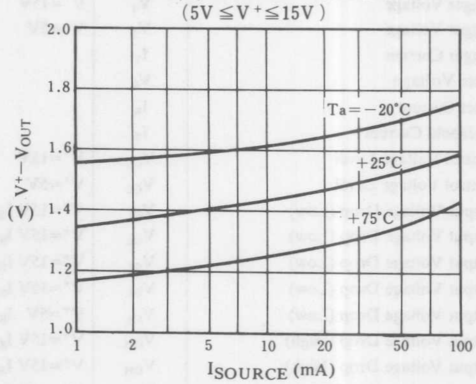
Delay Time vs. Operating Voltage

(Ta=25°C)



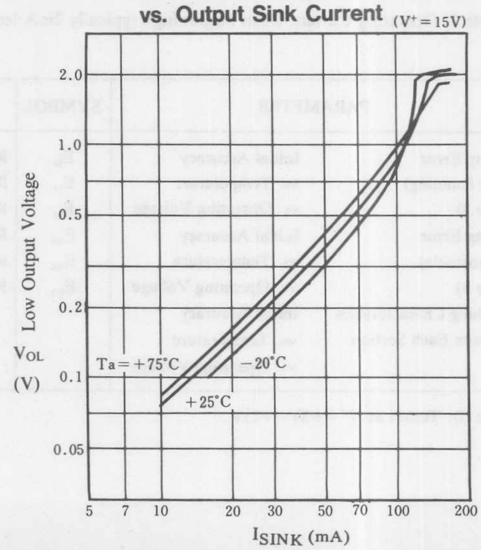
High Output Voltage Drop vs. Output Source Current

(5V ≦ V+ ≦ 15V)



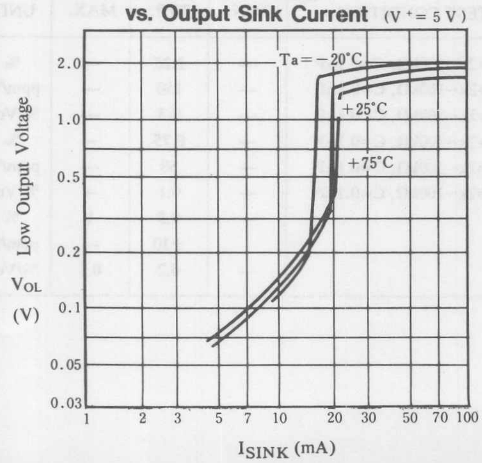
Low Output Voltage vs. Output Sink Current

(V+ = 15V)

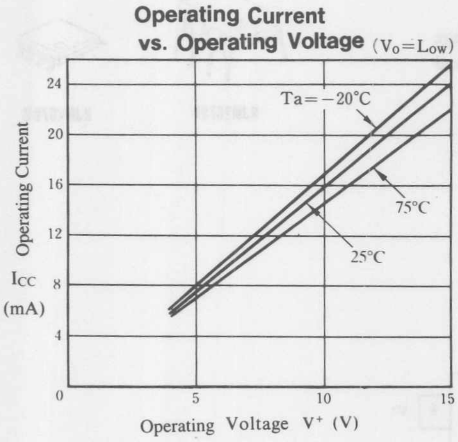


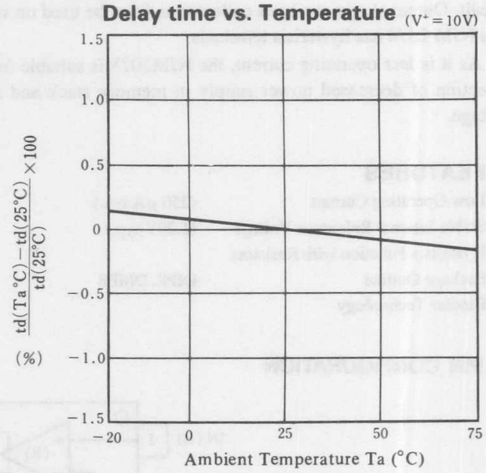
Low Output Voltage vs. Output Sink Current

(V+ = 5 V)



■ TYPICAL CHARACTERISTICS





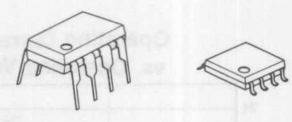
VOLTAGE DETECTOR

■ GENERAL DESCRIPTION

The NJM2078 is a dual comparator including precise reference circuit. Output stages are open collector and can be used on wired OR. The NJM 2078 has hysterisis terminals.

As it is less operating current, the NJM2078 is suitable for voltage detection of decreased power supply in memory stack and abnormal voltage.

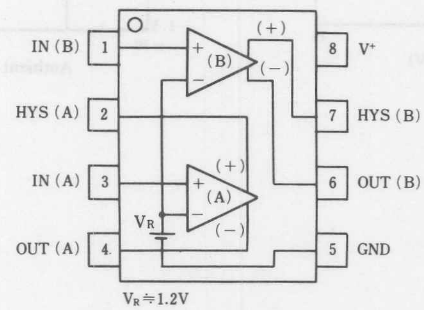
■ PACKAGE OUTLINE



■ FEATURES

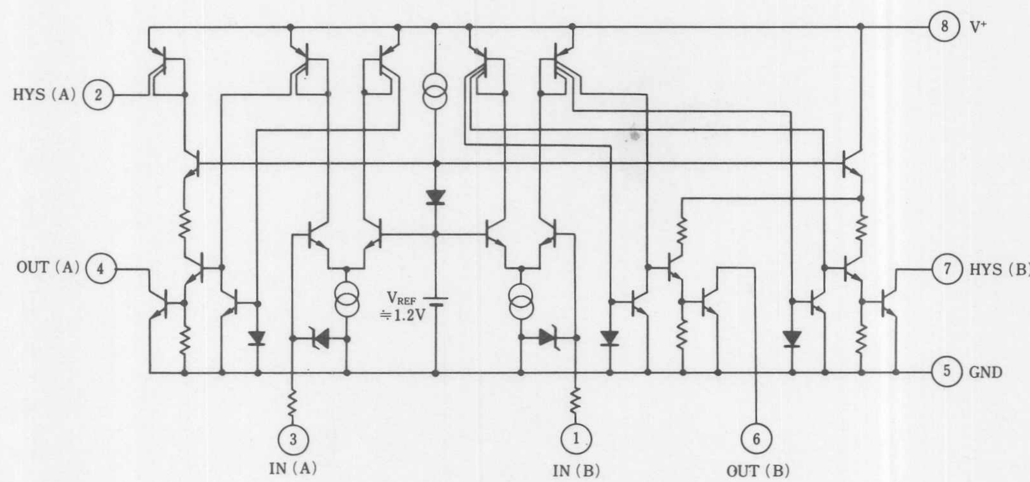
- Low Operating Current (250 μA typ.)
- Stable Internal Reference Voltage (1.20V typ.)
- Hysterisis Function with Resistors
- Package Outline DIP8, DMP8
- Bipolar Technology

■ PIN CONFIGURATION



NJM2078D
NJM2078M

■ EQUIVALENT CIRCUIT



■ **ABSOLUTE MAXIMUM RATINGS** (Ta=25℃)

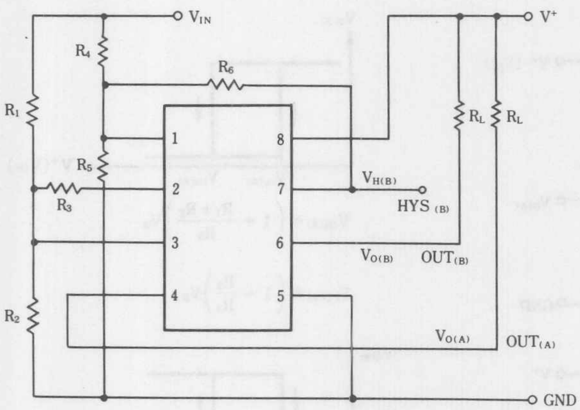
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	21	V
Output Voltage	V_O	21	V
Output Current	I_O	50	mA
Input Voltage	V_{IN}	−0.3～+6.5	Vdc
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

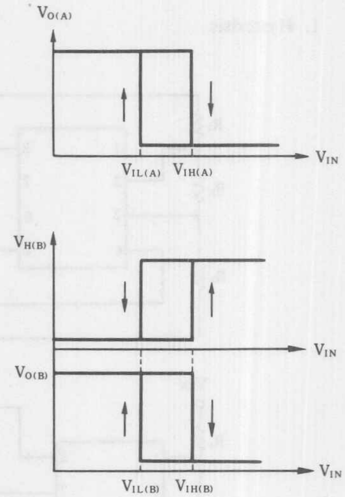
■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CCL}	V^+=20V, V_{IL}=1.0V	—	250	400	μA
	I_{CCH}	V^+=20V, V_{IH}=1.5V	—	400	600	μA
Threshold Voltage	V_{TH}	I_O=2mA, V_O=1V	1.15	1.20	1.25	V
Threshold Voltage Deviation vs. Operating Voltage	ΔV_{TH1}	2.5V≦V^+≦5.5V	—	3	12	mV
	ΔV_{TH2}	4.5V≦V^+≦20V	—	10	40	mV
Offset Voltage Between Normal Output and Hysterisis Output		$I_O(A)$=4.5mA, $V_O(A)$=2V, $I_H(A)$=20μA, $V_H(A)$=3V	—	2.0	—	mV
		$I_O(B)$=3mA, $V_O(B)$=2V, $I_H(B)$=3mA, $V_H(B)$=2V	—	2.0	—	mV
Threshold Voltage Temperature Coefficient		−20°C≦Ta≦70°C	—	±0.05	—	mV/°C
Threshold Voltage Difference Between Channels			−10	—	10	mV
Input Current	I_{IL}	I_{IL}=1.0V	—	5	—	nA
	I_{IH}	I_{IH}=1.5V	—	100	500	nA
Output Leak Current	I_{OH}	V_O=20V, V_{IL}=1.0V	—	—	1	μA
Hysterisis Output Leak Current	$I_{HL}(A)$	V^+=20V, $V_H(A)$=0V, V_{IL}=1.0V	—	—	0.1	μA
	$I_{HH}(B)$	$V_H(B)$=20V, V_{IH}=1.5V	—	—	1	μA
Output Sink Current	$I_{OL}(A)$	V_O=1.0V, V_{IH}=1.5V	6	12	—	mA
	$I_{OL}(B)$	V_O=1.0V, V_{IH}=1.5V	4	10	—	mA
Hysterisis Current	$I_{HH}(A)$	V_H=0V, V_{IH}=1.5V	40	80	—	μA
	$I_{HL}(B)$	V_H=1.0V, V_{IL}=1.0V	4	10	—	mA
Output Saturation Voltage	$V_{OL}(A)$	I_O=4.5mA, V_{IH}=1.5V	—	120	400	mV
	$V_{OL}(B)$	I_O=3.0mA, V_{IH}=1.5V	—	120	400	mV
Hysterisis Output Saturation Voltage	$V_{HH}(A)$	I_H=20μA, V_{IH}=1.5V	—	50	200	mV
	$V_{HL}(B)$	I_H=3.0mA, V_{IL}=1.0V	—	120	400	mV
Delay Time	t_{PHL}	R_L=5kΩ	—	2	—	μs
	t_{PLH}	R_L=5kΩ	—	3	—	μs

■ OPERATION PRINCIPLE





Equation

$$V_{IH(A)} = \left(1 + \frac{R_1}{R_2}\right) V_R$$

$$V_{IL(A)} = \left(1 + \frac{R_1}{R_2 /\!/ R_3}\right) V_R - \frac{R_1}{R_3} V^+$$

$$V_{IH(B)} = \left(1 + \frac{R_4}{R_5 /\!/ R_6}\right) V_R$$

$$V_{IL(B)} = \left(1 + \frac{R_4}{R_5}\right) V_R$$

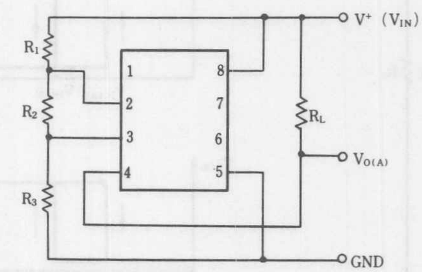
(note) $V_R \fallingdotseq V_{TH}$ ($\fallingdotseq$1.20V)

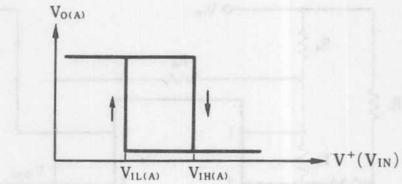
$$R_2 /\!/ R_3 = \frac{R_2 R_3}{R_2 + R_3}$$

$$R_5 /\!/ R_6 = \frac{R_5 R_6}{R_5 + R_6}$$

■ TYPICAL APPLICATION

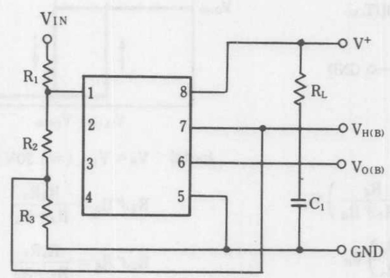
1. Hysterisis

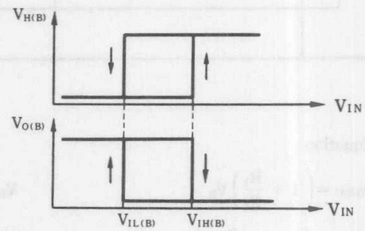




$$V_{IH(A)} \fallingdotseq \left(1+\frac{R_1+R_2}{R_3}\right)V_R$$

$$V_{IL(A)} \fallingdotseq \left(1+\frac{R_2}{R_3}\right)V_R$$



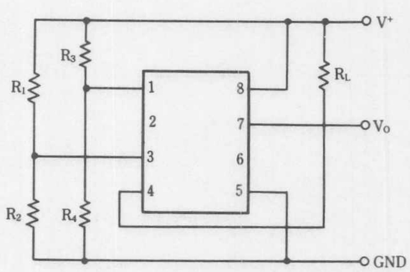


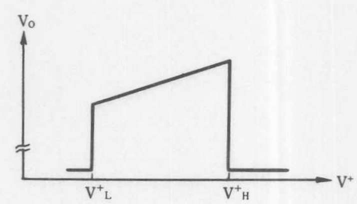
$$V_{IH(B)} \fallingdotseq \left(1+\frac{R_1}{R_2}\right)V_R$$

$$V_{IL(B)} \fallingdotseq \left(1+\frac{R_1}{R_2+R_3}\right)V_R$$

Each equation is calculated without considering the saturation voltage. It is necessary to compensate by the saturation voltage fit to lead conditions, precisely.

2. Detection of Abnormal Supply Voltage





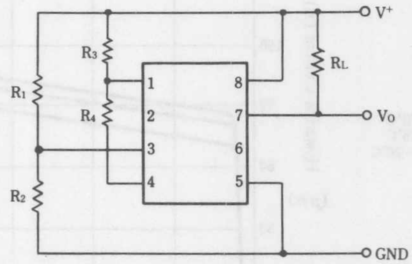
$$V^+_H = \left(1+\frac{R_1}{R_2}\right)V_R$$

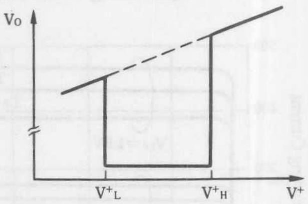
$$V^+_L = \left(1+\frac{R_3}{R_4}\right)V_R$$

Note: $V^+ \geqq 2.5V$

Hysterisis; Positive feedback from pin 2 or pin 7 (ref. 1).

3. Detection of Abnormal Operating Voltage



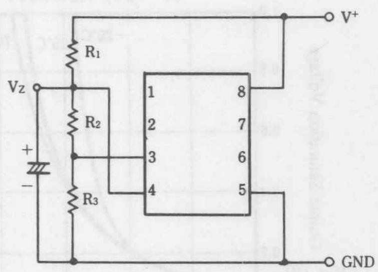


$$V^+_H = \left(1 + \frac{R_3}{R_4}\right) V_R$$

$$V^+_L = \left(1 + \frac{R_1}{R_2}\right) V_R$$

Note: $V^+_L \geqq 2.5V$

4. Programmable Zener

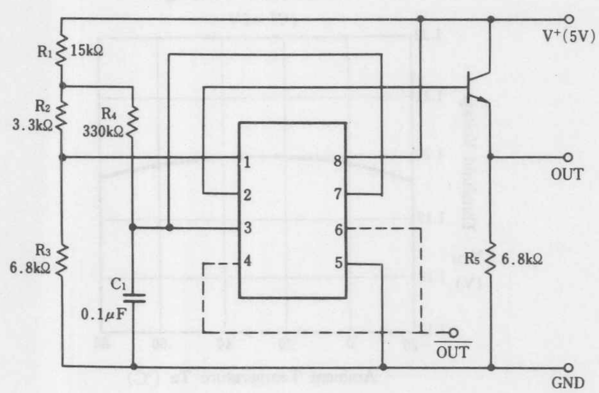


$$V_Z \fallingdotseq \left(1 + \frac{R_2}{R_3}\right) V_R$$

$$\frac{V_Z}{R_2 + R_3} \leqq \frac{V^+ - V_Z}{R_1} \leqq 6\,\text{mA}$$

Can use channel B independently.

5. Reset Circuit for Decreased Operating Voltage



Comparate Voltage and hysterisis width can be adjustable by $R_1 \sim R_4$. Roughly.

$$V^+_{(L)} = \frac{R_1 + R_2 + R_3}{R_3} V_{TH}$$

$$V^+_{(H)} = V^+_{(L)} \frac{R_1 (R_2 + R_3)}{R_3 R_4} V_{TH}$$

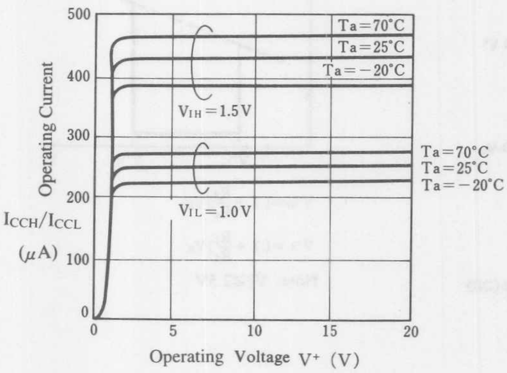
- Power-on reset time t_{RST} (roughly)

$$t_{RST} = -C_1 R_4 \ln \left\{ 1 - \frac{V_{TH}}{V^+} \left(1 + \frac{R_1}{R_2 + R_3}\right) \right\}$$

- Transistor; Recommended h_{FE}=50~200
- Rapid Signal Off; Be care to remained charge of C_1. It affects to t_{RST}.
- Reverse polarity output $\overline{OUT}$: Open collector.

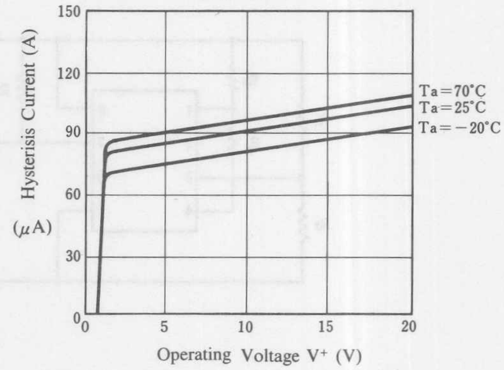
■ TYPICAL CHARACTERISTICS

Operating Current



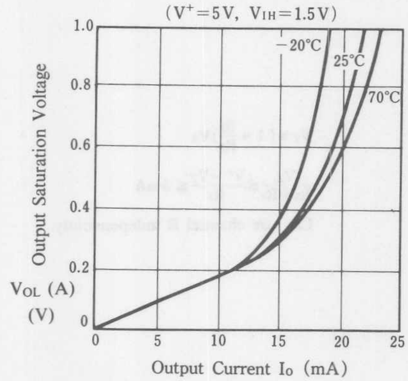
Hysterisis Current(A)

(VIH=1.5V)



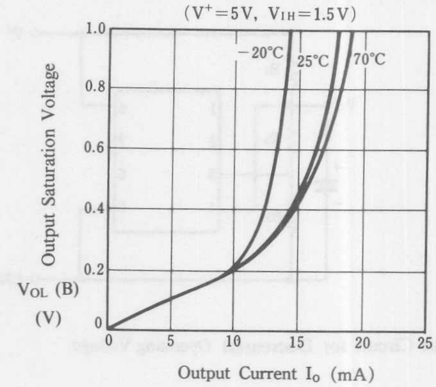
Output Saturation Voltage (A)

(V+=5V, VIH=1.5V)



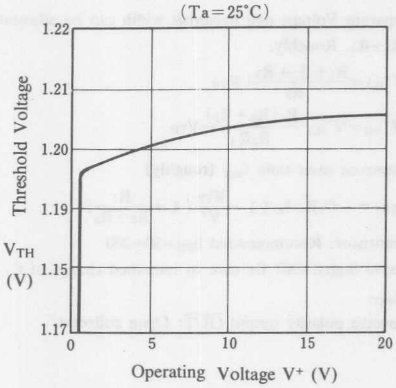
Output Saturation Voltage (B)

(V+=5V, VIH=1.5V)



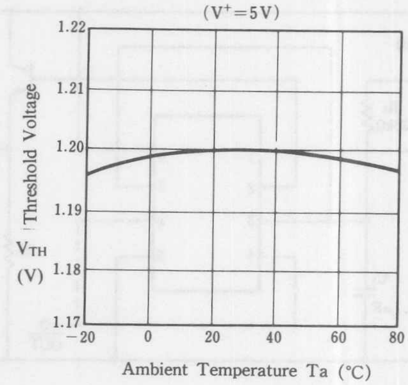
Threshold Voltage

(Ta=25°C)



Threshold Voltage

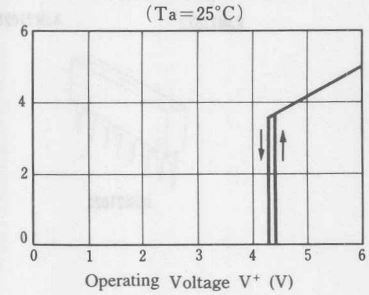
(V+=5V)



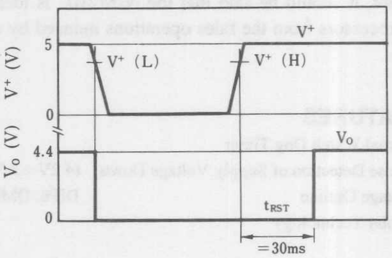
■ TYPICAL CHARACTERISTICS (Refer to Application 5 of Reset Circuit for Decreased Supply Voltage)

DC Characteristics

(Ta=25°C)



Pulse Response

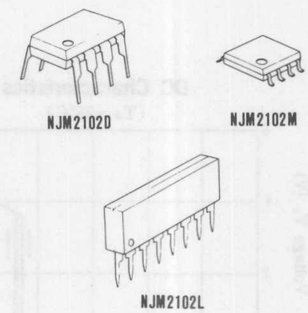


SYSTEM RESET IC

■ GENERAL DESCRIPTION

The NJM2102 Possesses two functions. One is to detect a voltage which decays from the desired voltage and generate a warning signal. And also, the NJM2102 holds the warning signal for a certain term after the specified voltage is obtained or recovered. The other one (Watch Dog Timer) is to identify missing clocks of microprocessors. Therefore, it should be said that the NJM2102 is ideal to protect any microprocessors from the fales operations induced by undesired condition.

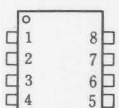
■ PACKAGE OUTLINE



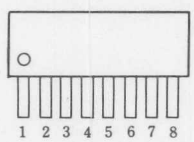
■ FEATURES

- Internal Watch Dog Timer
- Precise Detection of Supply Voltage Down (4.2V±2.5%)
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

■ PIN CONFIGURATION



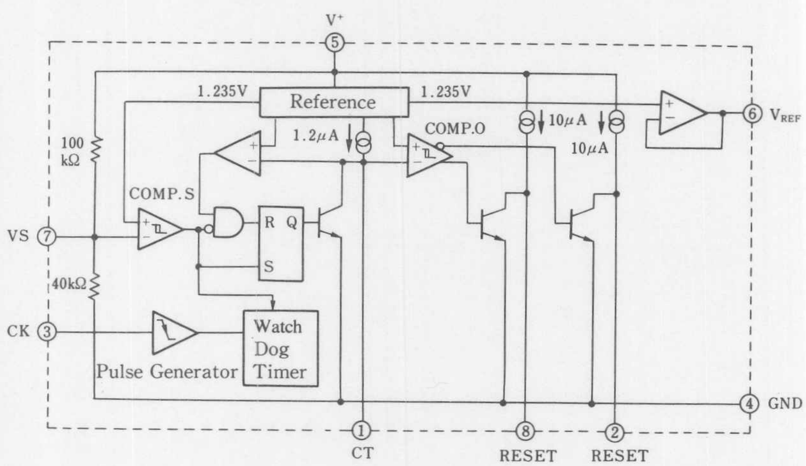
NJM2102D
NJM2102M



NJM2102L

PIN FUNCTION
1. CT
2. RESET
3. CK
4. GND
5. V^+
6. V_{REF}
7. V_S
8. $\overline{RESET}$

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(T_a=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V^+{}_1$	13.5	V
Input Voltage	V_S	V^++0.3(<20)	V
Input Voltage	V_{CK}	20	V
Power Dissipation	P_D	(DIP8) 500	mW
		(SIP8) 600	mW
		(DMP8) 300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=5V, T_a=25℃)

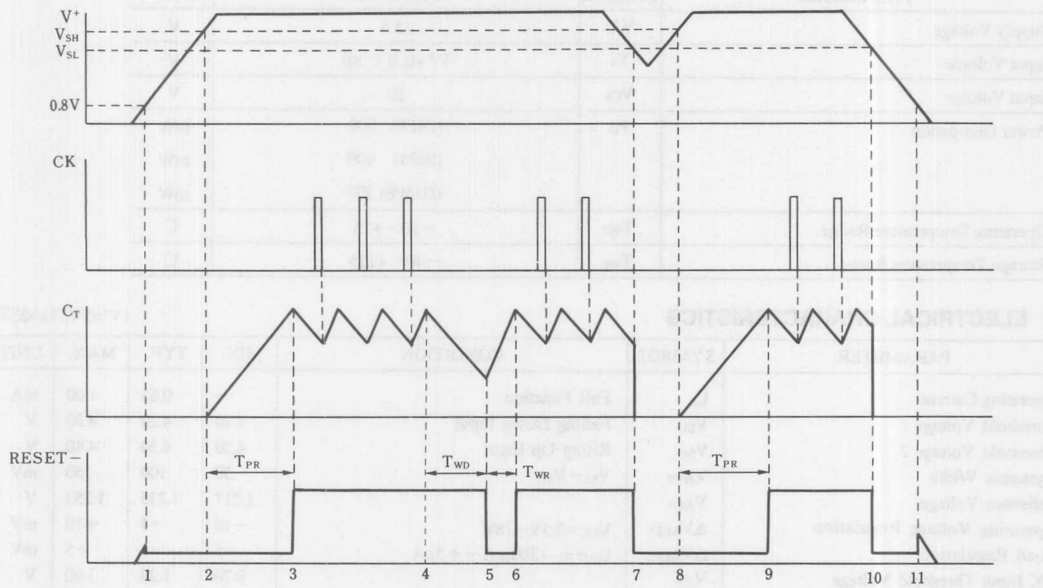
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{cc}	Full Function	—	0.65	1.00	mA
Threshold Voltage 1	V_{SL}	Falling Down Input	4.10	4.20	4.30	V
Threshold Voltage 2	V_{SH}	Rising Up Input	4.20	4.30	4.40	V
Hysteresis Width	V_{HYS}	$V_{SL}-V_{SH}$	50	100	150	mV
Reference Voltage	V_{RFF}		1.217	1.235	1.253	V
Operating Voltage Regulation	ΔV_{REF1}	V_{CC}=3.5V～18V	−10	+3	+10	mV
Load Regulation	ΔV_{REF2}	$I_{OUT}=-200\mu A\sim+5\mu A$	−5	—	+5	mV
CK Input Threshold Voltage	V_{TH}		0.70	1.24	1.90	V
CK Input Current 1	I_{IH}	V_{CK}=5.0V	—	0	1.0	μA
CK Input Current 2	I_{IL}	V_{CK}=0.0V	−1.0	−0.1	—	μA
C_T Charge Current 1	I_{CTC1}	(Note 1)	20	50	110	μA
C_T Charge Current 2	I_{CTC2}	V_{CK}=0.0V	0.6	1.4	3.0	μA
Capacitor Discharge Current 1	I_{CTD1}	(Note 1)	6	9	13	μA
Capacitor Discharge Current 2	I_{CTD2}	V_{CK}=0.0V	100	600	—	μA
Output Voltage (High) 1	V_{OH1}	V_S=Open. $I_{\overline{RESET}}=-5\mu A$	4.5	4.9	—	V
Output Voltage (High) 2	V_{OH2}	V_S=0V,$I_{RESET}=-5\mu A$	4.5	4.9	—	V
Output Voltage (Low) 1	V_{OL1}	V_S=0V,$I_{\overline{RESET}}$=3mA	—	0.2	0.4	V
Output Voltage (Low) 2	V_{OL2}	V_S=0V,$I_{\overline{RESET}}$=10mA	—	0.3	0.5	V
Output Voltage (Low) 3	V_{OL3}	V_S =Open. I_{RESET}=3mA	—	0.2	0.4	V
Output Voltage (Low) 4	V_{OL4}	V_S =Open. I_{RESET}=10mA	—	0.3	0.5	V
Output Sink Current 1	I_{OL1}	V_S =0V $V_{\overline{RESET}}$=1.0V	20	70	—	mA
Output Sink Current 2	I_{OL2}	V_S =Open. V_{RESET}=1.0V	20	70	—	mA
Minimum Operating Voltage 1	V_{CCL1}	$V_{\overline{RESET}}$=0.4V, $I_{\overline{RESET}}$=0.2mA	—	0.8	1.2	V
Minimum Operating Voltage 2	V_{CCL2}	$V_{RESET}=V^+-0.1V$, R_L =1MΩ	—	0.8	1.2	V

AC CHARACTERISTICS

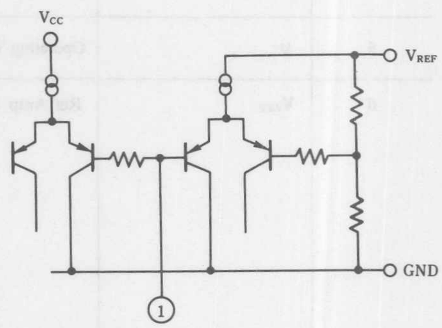
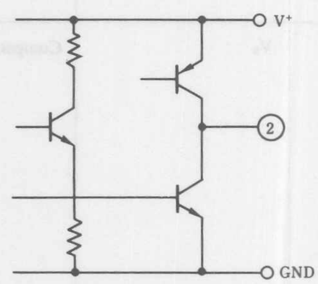
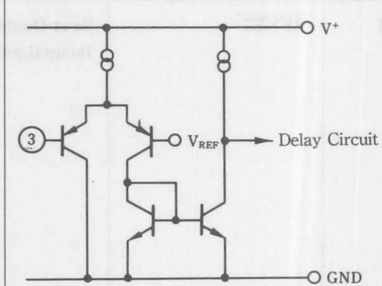
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
V^+ Input Pulse Width	T_{PI}	V_{CC} 5V 4V (Note 2)	—	10	—	μS
CK Input Pulse Width	T_{CKW}	CK or (Note 2)	—	1.8	—	mS
CK Input Period	T_{CK}	(Note 2)	—	12	—	mS
Watch Dog Timer Warning Threshold Time	T_{WD}	C_T =0.1μF	—	10	—	mS
Watch Dog Timer Reset Pulse Width	T_{WR}	C_T =0.1μF	—	2	—	mS
Reset Signal Hold Time	T_{PR}	C_T =0.1μF	—	100	—	mS
Propagation Delay ($\overline{RESET}$ Terminal)	T_{PD1}	R_L =2.2kΩ, C_L =100pF	—	2	—	μS
(RESET Terminal)	T_{PD2}	R_L =2.2kΩ, C_L =100pF	—	3	—	μS
Output Rise Time	t_R	R_L =2.2kΩ, C_L =100pF	—	1.0	—	μS
Output Fall Time	t_F	R_L =2.2kΩ, C_L =100pF	—	0.1	—	μS

(Note1) : The specified pulses (Refer to AC Characteristics) are applied to CK-pin.
(Note2) : This characteristics is guaranteed within the design.

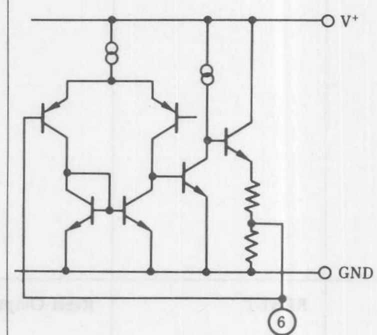
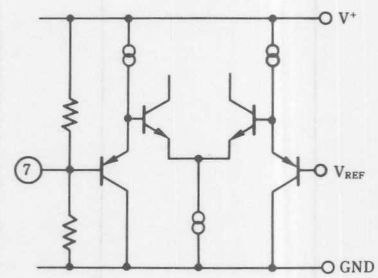
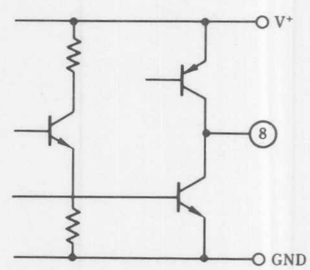
■ TIMING CHART



■ **TERMINAL FUNCTION**

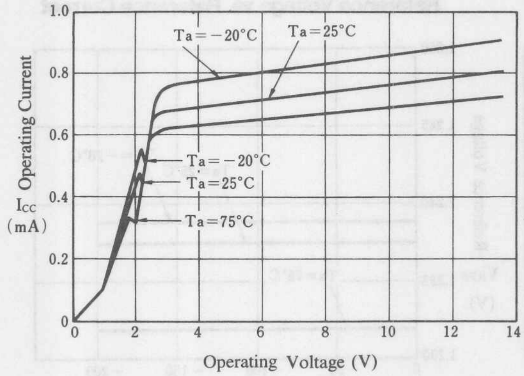
PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	C_T	Pin Connection to Capacitor, Set the reset holding time	
2	RESET	Reset Output	
3	CK	Crock Input	

■ TERMINAL FUNCTION

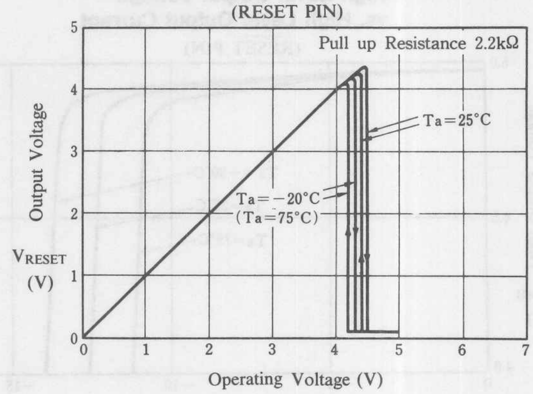
PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
4	GND	Ground	
5	V^+	Operating Voltage	
6	V_{REF}	Ref Amp Output	
7	V_S	Comparator S Input	
8	$\overline{\text{RESET}}$	Reset Output Internal pull up resistor	

■ TYPICAL CHARACTERISTICS

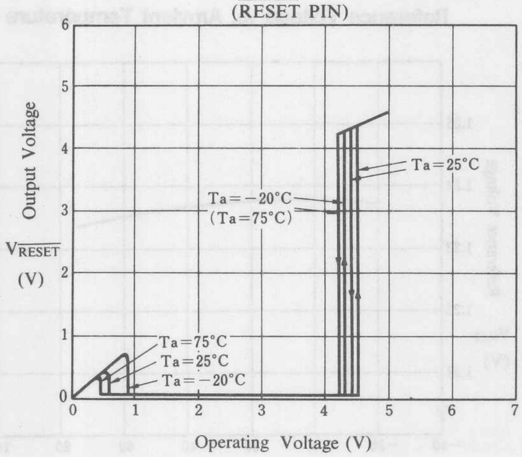
Operating Current vs. Operating Voltage



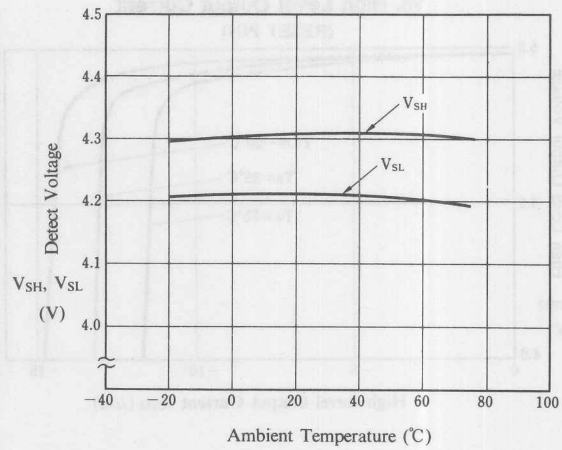
Output Voltage vs. Operating Voltage
(RESET PIN)



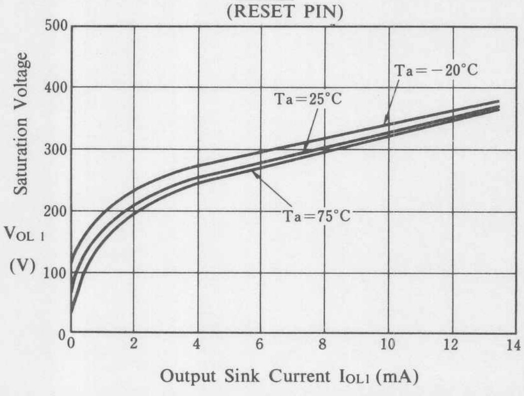
Output Voltage vs. Operating Voltage
($\overline{\text{RESET}}$ PIN)



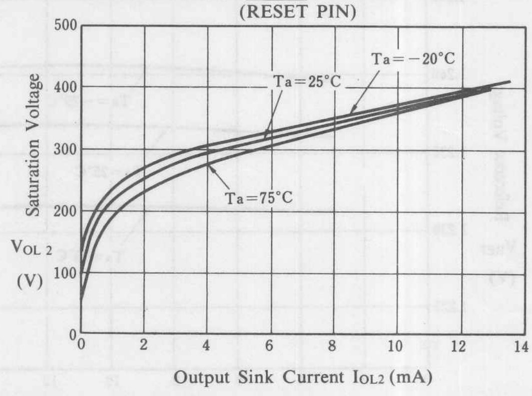
Detect Voltage vs. Ambient Temperature



Saturation Voltage vs. Output Sink Current
($\overline{\text{RESET}}$ PIN)



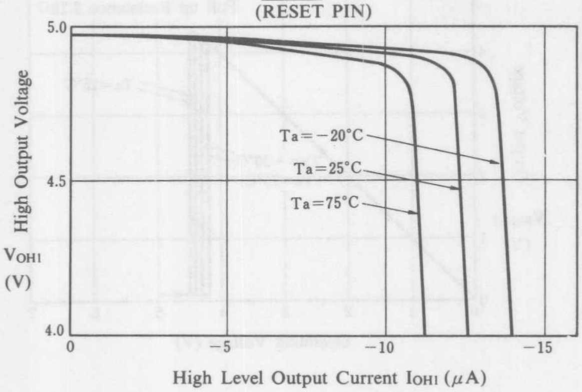
Saturation Voltage vs. Output Sink Current
(RESET PIN)



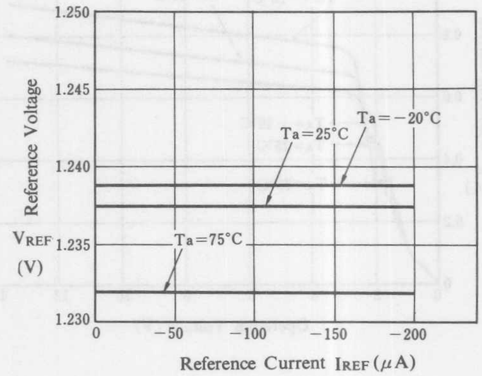
■ TYPICAL CHARACTERISTICS

High Level Output Voltage vs. High Level Output Current

(RESET PIN)

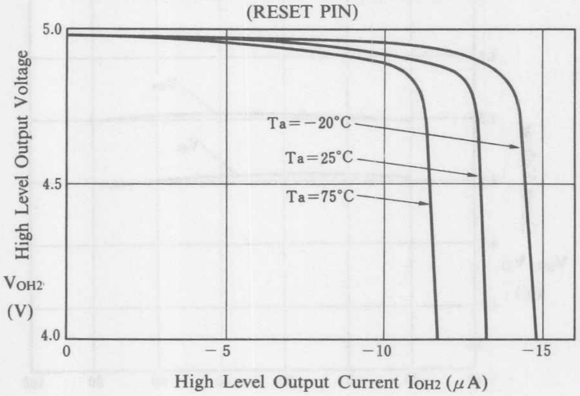


Reference Voltage vs. Reference Current

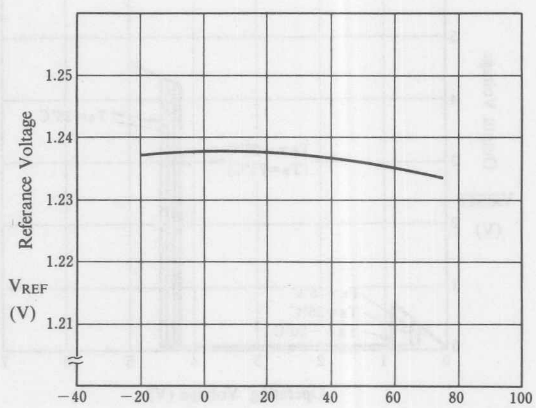


High Output Voltage vs. High Level Output Current

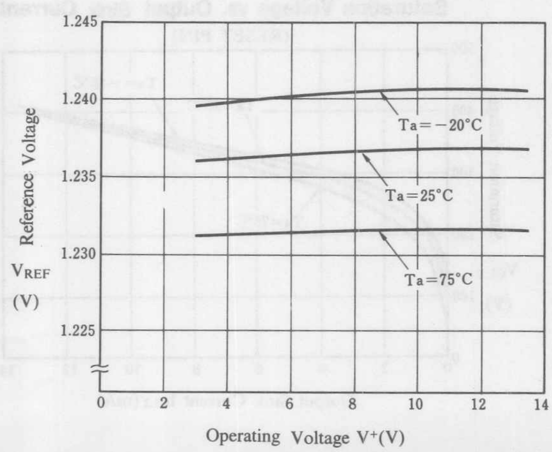
(RESET PIN)



Reference Voltage vs. Amvient Temperature

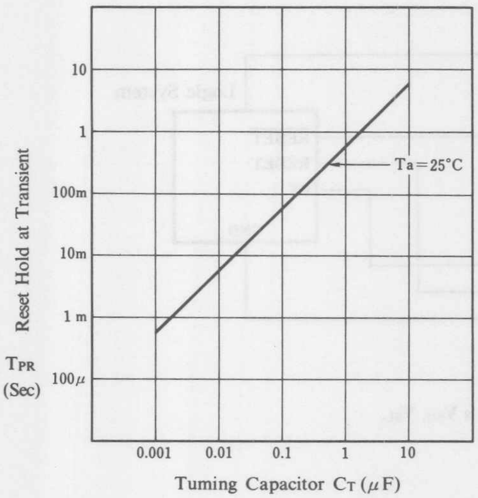


Reference Voltage vs. Operating Voltage

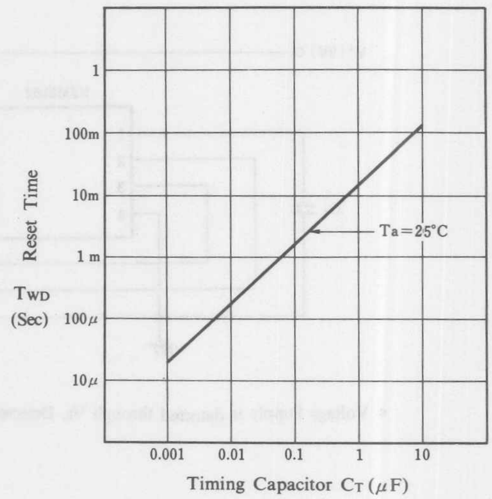


■ TYPICAL CHARACTERISTICS

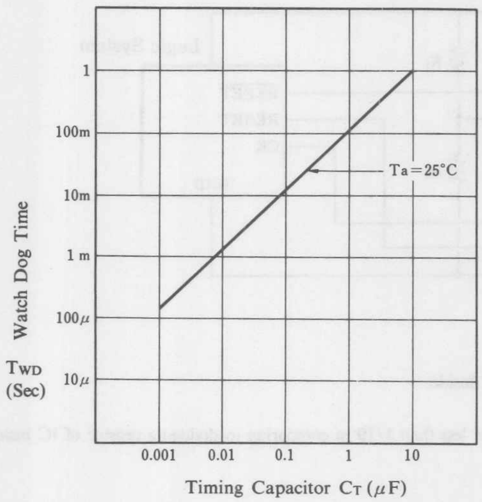
Reset Hold Time at Transient



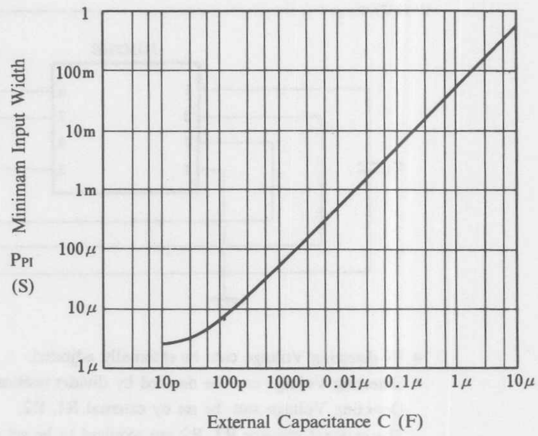
Reset Time



Watch Dog Timer observation time

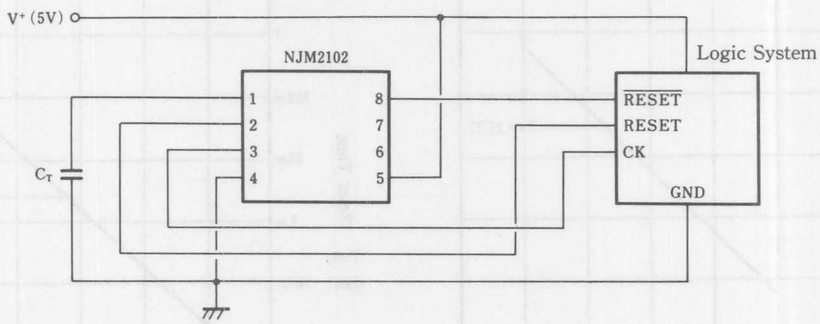


Minimam Input Pulse Width vs. CT



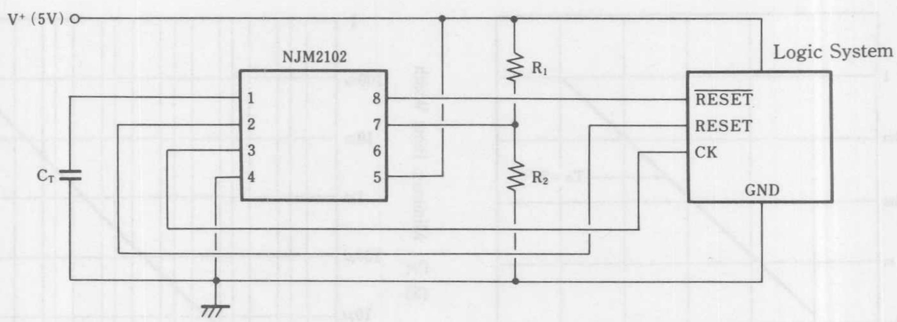
■ APPLICATION CIRCUIT

1. 5V Supply Voltage Supervisory and Watch-dog-timer



- Voltage Supply is detected through Vs. Detected Voltage is V_{SH}, V_{SL}.

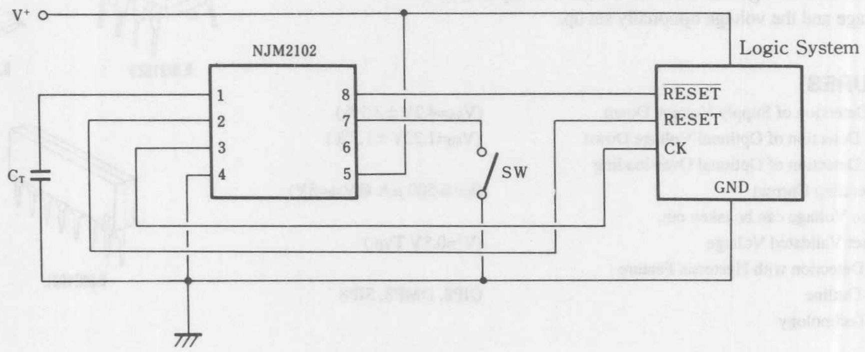
2. 5V Supply Voltage Supervisiory (Externally fine tunning type)



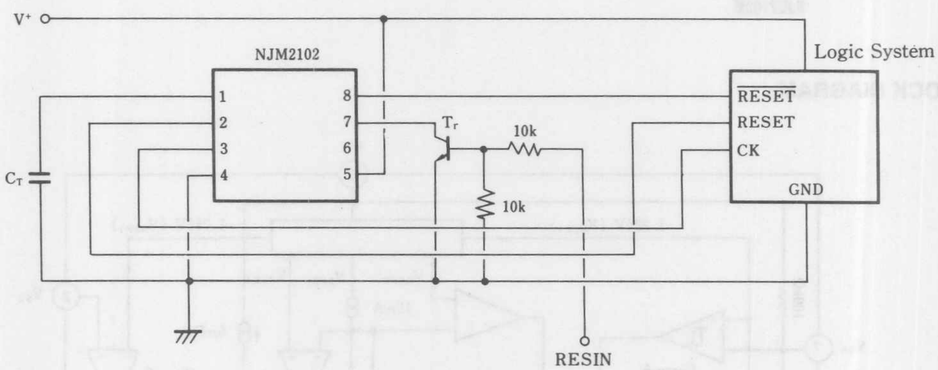
- Vs detecting Voltage can be externally adjusted.
- Detecting Voltage can be decided by divider resistor of IC inside.
  Detecting Voltage can be set by external R1, R2.
  The external resisitor R1, R2 are required to be set in value less than 1/10 in comparing to divideing resistor of IC inside.
  Please refere to following Table.

R_1(kΩ)	R_2(kΩ)	Detecting Voltage: V_{SL}(V)	Detecting Voltage: V_{SH}(V)
10	3.9	4.34	4.44
9.1	3.9	4.08	4.18

3. Compulsory Resetting attached (Reset Hold attached)



- *Pin 7 to be grounded when SW. ON. RESET(8pin) become Low: RESET(pin2) become HIGH.



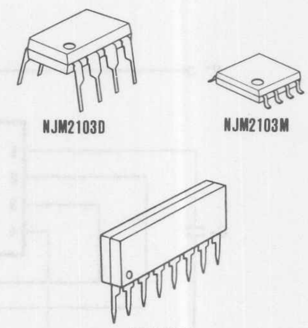
- By putting signal in the RESET pin, and Tr swich ON $\overline{RESET}$ pin become LOW and RESET pin High.

SYSTEM RESET IC

■ GENERAL DESCRIPTION

NJM2103 is supply voltage supervisory IC to detect the abnormal conditions, such as shut down of all supply voltages at once, or sudden voltage down and then generate the reset signal. It supervises both 5V supply voltage and the voltage optionally set up.

■ PACKAGE OUTLINE

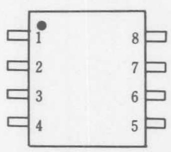


NJM2103D NJM2103M NJM2103L

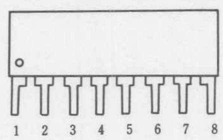
■ FEATURES

- Precise Detection of Supply Voltage Down (V$_{SA}$=4.2V±2.5%)
- Possible Detection of Optional Voltage Down (V$_{SB}$=1.22V±1.5%)
- Possible Detection of Optional Over-loading
- Low Operating Current (I$_{CC}$≦500 μA @V$_{SB}$=5V)
- Reference Voltage can be taken out.
- Low Reset Validated Voltage (V$^+$=0.8V Typ.)
- Voltage Detection with Hysteresis Feature
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

■ PIN CONFIGURATION



NJM2103D
NJM2103M

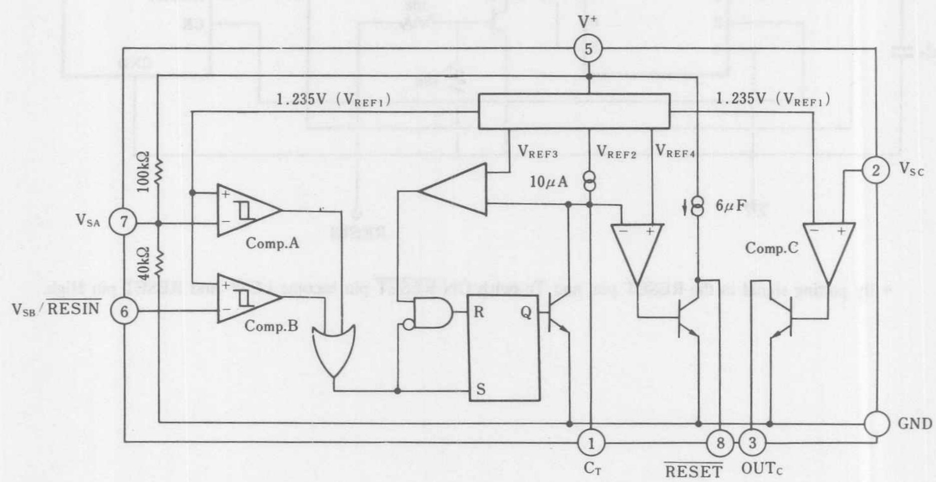


NJM2103L

PIN FUNCTION

1. C$_T$
2. V$_{SC}$
3. OUT$_C$
4. GND
5. V$^+$
6. V$_{SB}$/$\overline{\text{RESIN}}$
7. V$_{SA}$
8. $\overline{\text{RESET}}$

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	20	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DM8) 300	mW
		(SIP8) 800	mW
Input Voltage A	V_{SA}	V^++0.3(<20)	V
Input Voltage B	V_{SB}	20	V
Input Voltage C	V_{SC}	20	V
Operating Temperature Range	T_{opr}	−20~+75	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS

(V^+=5.0Vk V_{SB}=0V, V_{SC}=0V, Ta=25℃)

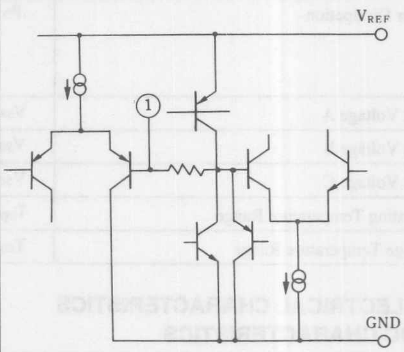
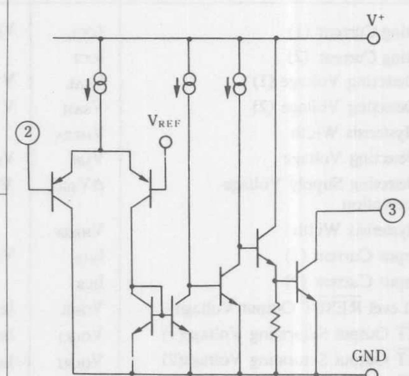
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	I_{CC1}	V_{SB}=5V	—	380	560	μA
Operating Current (2)	I_{CC2}		—	460	700	μA
V_{SA} Detecting Voltage (1)	V_{SAL}	V^+ fall time V_{SB}= V^+	4.10	4.20	4.30	V
V_{SA} Detecting Voltage (2)	V_{SAH}	V^+ rise time V_{SB}= V^+	4.20	4.30	4.40	V
V_{SA} Hysterisis Width	V_{HRSA}		50	100	150	mV
V_{SB} Detecting Voltage	V_{SBL}	V_{SB} fall time	1.202	1.220	1.238	V
V_{SB} Detecting Supply Voltage Fluctuation	ΔV_{SBL}	V^+=3.5~18V	—	3	10	mV
V_{SB} Hysterisis Width	V_{HRSB}		14	28	42	mV
V_{SB} Input Current (1)	I_{IHB}	V_{SB}=5V	—	0	250	nA
V_{SB} Input Current (2)	I_{ILB}		—	20	250	nA
High Level $\overline{\text{RESET}}$ Output Voltage	V_{OHR}	I_{RESET}=−5μA, V_{SB}=5V	4.5	4.9	—	μV
$\overline{\text{RESET}}$ Output Saturating Voltage(1)	V_{OLR1}	I_{RESET}=2mA	—	0.20	0.40	V
$\overline{\text{RESET}}$ Output Saturating Voltage(2)	V_{OLR2}	I_{RESET}=10mA	—	0.30	0.50	V
$\overline{\text{RESET}}$ Output Sink Current	I_{RESET}	V_{OLR}=1.0V	20	80	—	mA
C_T Charge Current	I_{CT}	V_{SB}=5V, VCT=0.5V	6.0	9.5	13.0	μA
V_{SC} Input Current (1)	I_{IHC}	V_{SC}=5V	—	0	500	nA
V_{SC} Input Current (2)	I_{ILC}		—	50	500	nA
V_{SC} Detecting Voltage	V_{SC}		1.215	1.235	1.255	V
V_{SC} Detecting Supply Voltage Fluctuation	ΔV_{SC}	V^+=3.5~13.5V	—	3	10	mV
OUT_C Output Leak Current	I_{OHC}	V_{OHC}=13.5V	—	0	1	μA
OUT_C Output Saturation Voltage	V_{OLC}	I_{OUT}=4mA, V_{SC}=5V	—	0.10	0.40	V
OUT_C Output Sink Current	I_{OUTC}	V_{OLC}=1.0V, V_{SC}=5V	6	20	—	mA
RESET Guarantee Minimum Supply Voltage	V^+_L	V_{OLR}=0.4V, I_{RESET}=200μA	—	0.8	1.2	V

● AC CHARACTERISTICS

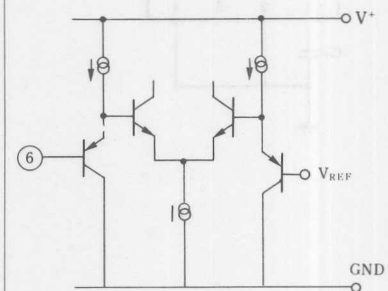
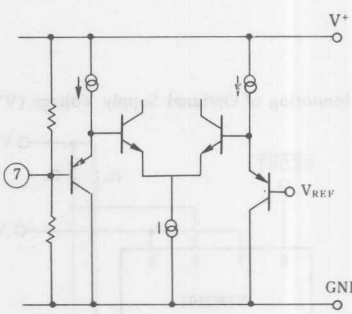
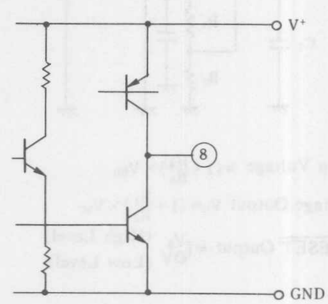
(V^+=5.0V V_{SB}=5.0V, V_{SC}=0V, CT=0.01 μF, Ta=25℃)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{SA} Input Pulse Width	t_{PIA}		—	3.0	—	μs
V_{SB} Input Pulse Width	t_{PIB}		—	1.5	—	μs
$\overline{\text{RESET}}$ Output Pulse Width	t_{PO}	V_{SB}=V^+	—	1.5	—	ms
$\overline{\text{RESET}}$ Rise Time	t_r	V_{SB}=V^+, R_L=2.2kΩ, C_l=100pF	—	1.0	—	μs
$\overline{\text{RESET}}$ Fall Time	t_f	V_{SB}=V^+, R_L=2.2kΩ, C_L=100pF	—	0.1	—	μs
Output Delay Time	t_{PD}	V_{SB} fall time	—	2	—	μs
Output Delay Time	t_{PHL}	V_{SC} rise time, R_L=2.2kΩ, C_L=100pF	—	0.5	—	μs
Output Delay Time	t_{PLH}	V_{SC} fall time, R_L=2.2kΩ, C_L=100pF	—	1.0	—	μs

■ TERMINAL FUNCTION

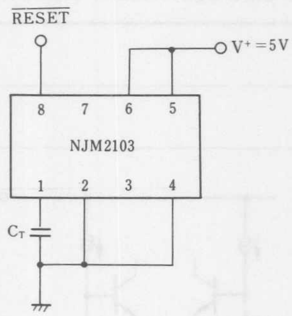
PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	C_T	Pin Connection to Capacitor, Set the reset holding time.	
2	V_{SC}	Comparator Input	
3	OUT_C	Open Collector Output of Comparator C.	

■ TERMINAL FUNCTION

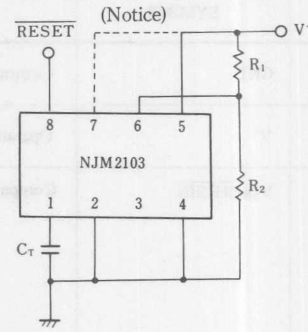
PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
4	GND	Ground	
5	V^+	Operating Voltage	
6	$V_{SB}/\overline{RESIN}$	Comparator B Input	
7	V_{SA}	Comparator A Input	
8	$\overline{RESET}$	Reset Output Internalizing pull up resistor	

■ APPLICATION CIRCUIT

1) 5V Supply Voltage Monitor



2) Monitoring of Optional Supply Voltage ($V^+ \leqq 13.5V$)

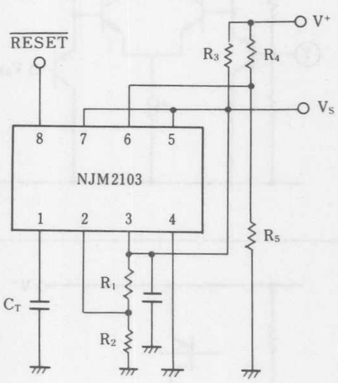


Detecting Voltage $\fallingdotseq (1+\frac{R_1}{R_2}) \times V_{SB}$

(Notice)

If it were that V^+ indicates under 4.50V, Connect 7 pin to V^+

3) Monitoring of Optional Supply Voltage ($V^+ > 13.5V$)

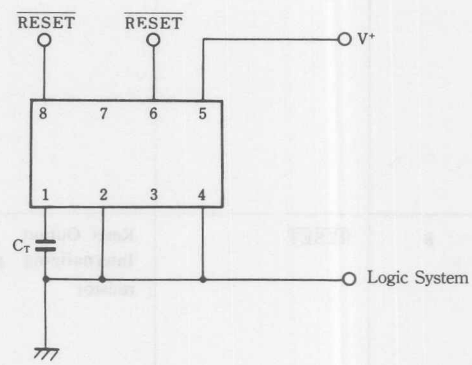


Detecting Voltage $\fallingdotseq (1+\frac{R_4}{R_5}) \times V_{SB}$

Constant Voltage Output $V_S \fallingdotseq (1+\frac{R_1}{R_2}) \times V_{SC}$

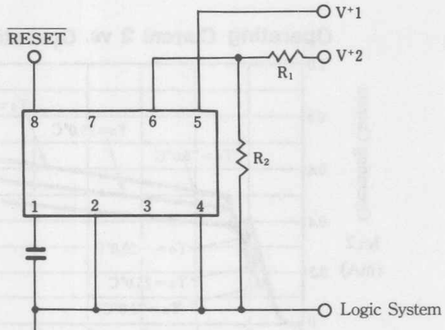
$\overline{\text{RESET}}$ Output $\fallingdotseq \{ \begin{matrix} V_S & \text{(High Level)} \\ 0V & \text{(Low Level)} \end{matrix}$

4) Compulsry Reset



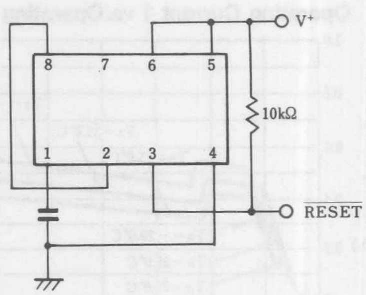
Input Reset signal TTL level to V_{SB}-terminal

5) 5V,V_{CC}<12V Supply Voltage Monttor

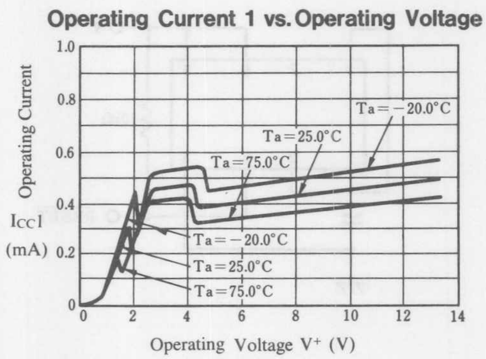


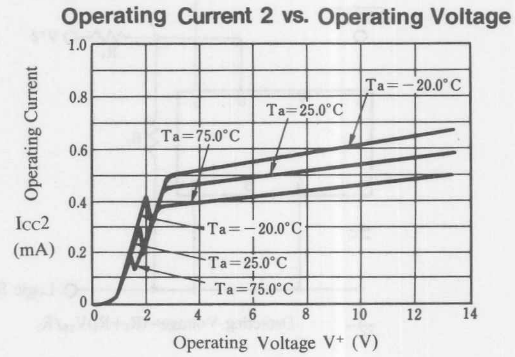
Detecting Voltage=$(R_1+R_2)V_{SB}/R_2$

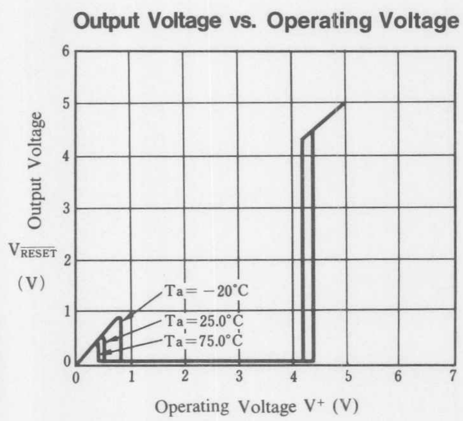
6) Non-Inverting Reset

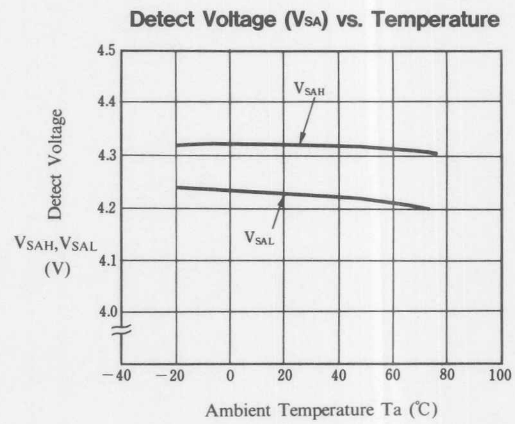


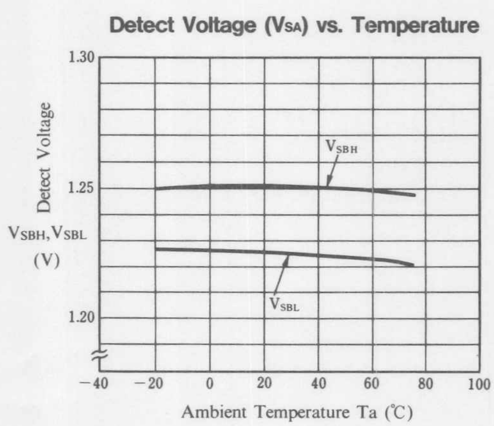
■ TYPICAL CHARACTERISTICS

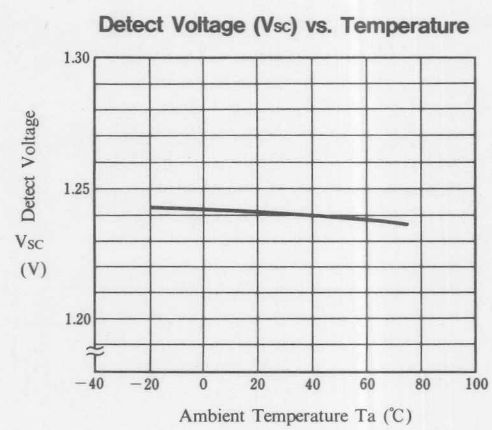






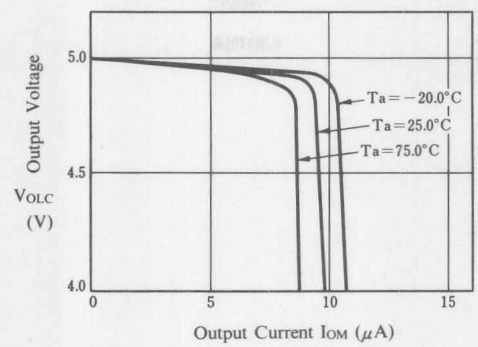




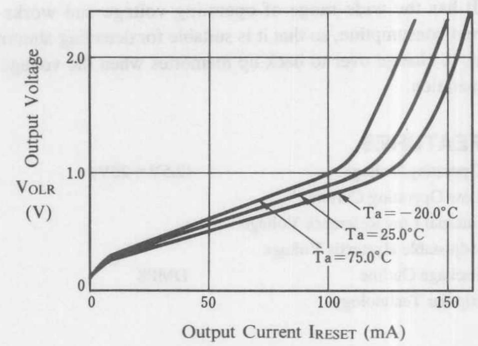


■ TYPICAL CHARACTERISTICS

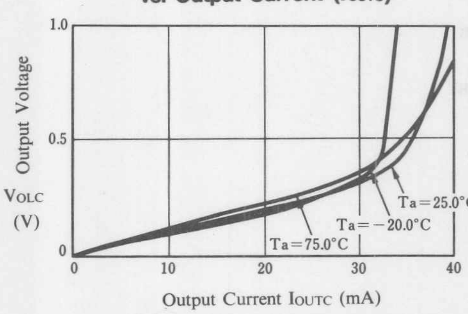
Output Voltage vs. Output Current



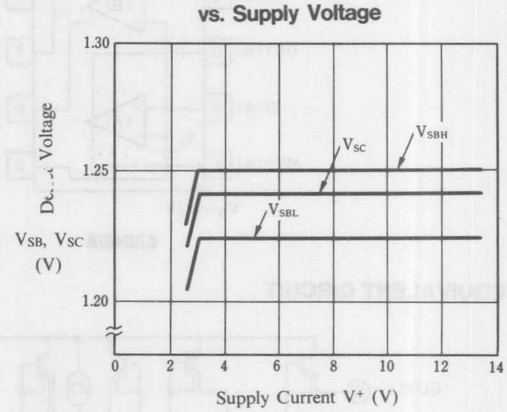
Output Voltage vs. Output Current



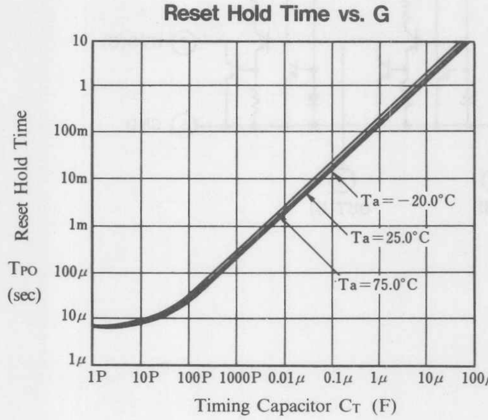
Output Voltage (OUTc) vs. Output Current (IOUTC)



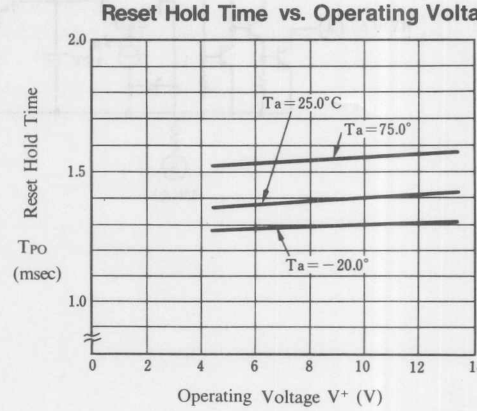
Detect Voltage (VSB, VSC) vs. Supply Voltage



Reset Hold Time vs. G



Reset Hold Time vs. Operating Voltage



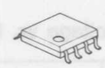
VOLTAGE DETECTOR

■ GENERAL DESCRIPTION

NJM2405 is a dual comparator, including the high precision reference voltage circuit. Both channels have hystersis pins, so it could provide the hysteretic function for systems.

It has the wide range of operating voltage and works with less current consumption, so that it is suitable for detecting abnormal conditions, to change over to back up memories when the voltage drops off in operation.

■ PACKAGE OUTLINE

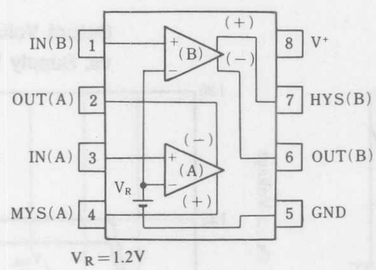


NJM2405M

■ FEATURES

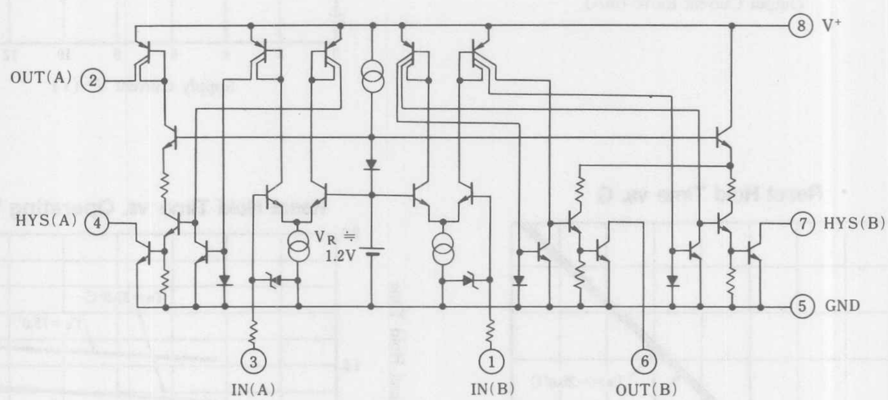
- Operating Voltage (2.5V～20V)
- Low Operating Current
- Internal Low Reference Voltage
- Adjustable Hystersis Voltage
- Package Outline DMP8
- Bipolar Technology

■ PIN CONFIGURATION



NJM2405M

■ EQUIVALENT CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

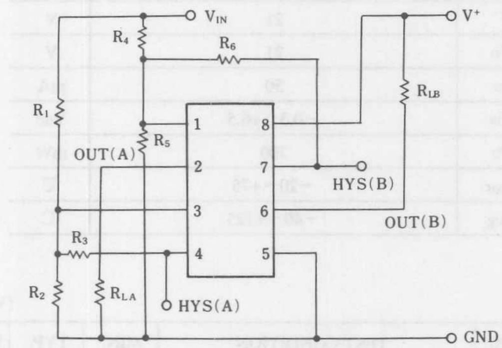
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	21	V
Output Voltage	V_O	21	V
Output Current	I_O	50	mA
Input Voltage	V_{IN}	−0.3～+6.5	Vdc
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

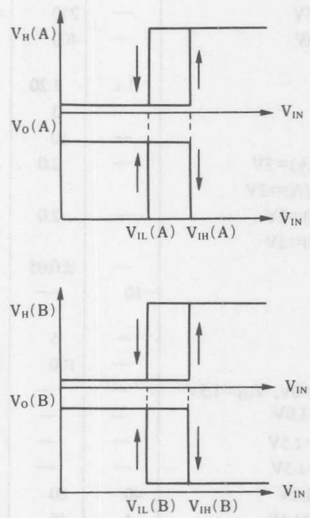
■ ELECTRICAL CHARACTERISTICS

(V^+=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CCH}	V^+ =20V, V_{IH}=1.5V	—	250	400	μA
	I_{CCL}	V^+ =20V, V_{IL}=1.0V	—	400	600	μA
Threshold Voltage	V_{TH}	I_O=2mA, V_O=1V	1.1.	1.20	1.25	V
Threshold Voltage Deviation vs Supply Voltage	ΔV_{TH1}	2.5V≦V^+≦5.5V	—	3	12	mV
	ΔV_{TH2}	4.5V≦V^+≦40V	—	10	40	mV
Offset Voltage between Normal Output and Hysteresis Output		I_O(A)=20μA, V_O(A)=3V I_H(A)=4.5mA, V_H(A)=2V	—	2.0	—	mV
		I_O(B)=3mA, V_O(B)=2V I_H(B)=3mA, V_H(B)=2V	—	2.0	—	mV
Threshold Voltage Temperature Coefficient		−20℃≦T_a≦70℃	—	±0.05	—	mV/℃
Threshold Voltage Difference Between Channels			−10	—	10	mV
Input Current	I_{IL}	I_{IL}=1.0V	—	5	—	nA
	I_{IH}	V_{IH}=1.5V	—	100	500	nA
Output Leak Current	I_{OH}(A)	V^+=20V, V_O(A)=0V, V_{IH}=1.5V	—	—	0.1	μA
	I_{OH}(B)	V_O(B)=20V, V_{IL}=1.0V	—	—	1	μA
Hysteresis Output leak Current	I_{HH}(A)	V_H(A)=20V, V_{IH}=1.5V	—	—	1	μA
	I_{HH}(B)	V_H(B)=20V, V_{IH}=1.5V	—	—	1	μA
Output Source Current	I_{OL}(A)	V_O(A)=0V, V_{IL}=1.0V	40	80	—	μA
Output Sink Current	I_{OL}(B)	V_O(B)=1.0V, V_{IH}=1.5V	4	10	—	mA
Hysteresis Current	I_{HL}(A)	V_H(A)=1.0V, V_{IL}=1.0V	6	12	—	mA
	I_{HL}(B)	V_H(B)=1.0V, V_{IL}=1.0V	4	10	—	mA
Output Saturation Voltage	V_{OL}(A)	I_O(A)=20μA, V_{IL}=1.0V	—	50	200	mV
	V_{OL}(B)	I_O(B)=3.0mA, V_{IH}=1.5V	—	120	400	mV
Hysteresis Output Saturation Voltage	V_{HL}(A)	I_H(A)=4.5mA. V_{IL}=1.0V	—	120	400	mV
	V_{HL}(B)	I_H(B)=3.0mA, V_{IL}=1.0V	—	120	400	mV
Delay Time	t_{PHL}	RL=5kΩ	—	2	—	μs
	t_{PLH}	RL=5kΩ	—	3	—	μs

■ GENERAL OPERATING INFORMATION (Operation Principle)





Relational Function (Attention)

$$V_{IH}(A) = \left(1 + \frac{R_1}{R_2 /\!/ R_3}\right) V_R$$

$$V_{IL}(A) = \left(1 + \frac{R_1}{R_2}\right) V_R$$

$$V_{IH}(B) = \left(1 + \frac{R_4}{R_5 /\!/ R_6}\right) V_R$$

$$V_{IL}(B) = \left(1 + \frac{R_4}{R_5}\right) V_R$$

(note) $V_R \doteqdot V_{TH}\ (\doteqdot 1.20V)$

$$R_2 /\!/ R_3 = \frac{R_2 R_3}{R_2 + R_3}$$

$$R_5 /\!/ R_6 = \frac{R_5 R_6}{R_5 + R_6}$$

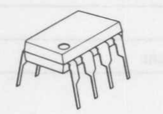
NJM2606/2606A

LOW VOLTAGE DC MOTOR CONTROLLER

■ GENERAL DESCRIPTION

The NJM2606A is integrated circuit with wide operating supply voltage range for DC motor speed control. Especially, the NJM2606A is suited for 3V or 6V DC motor control.

■ PACKAGE OUTLINE



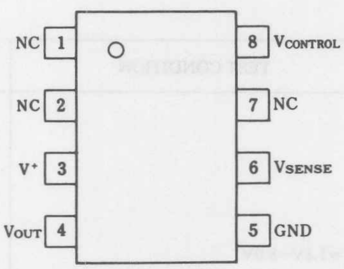
NJM2606D
NJM2606AD

NJM2606AM

■ FEATURES

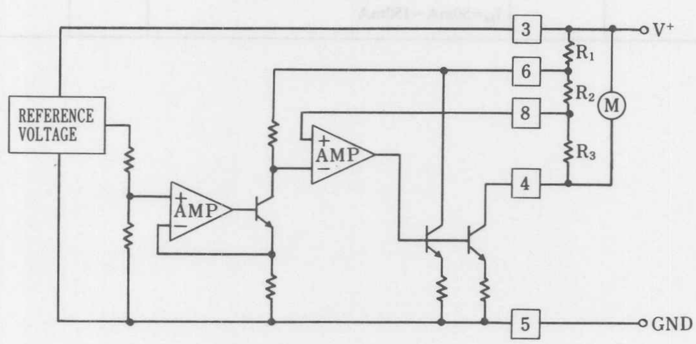
- Operating Voltage (1.8V ~ 8V)
- Internal Low Saturation Voltage Output Transistor
- Package Outline DIP8, DMP8
- Bipolar Technology

■ PIN CONFIGURATION



NJM2606D
NJM2606AD
NJM2606AM

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	10	V
Peak-to-peak Output Current	I_{OP}	700	mA
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
Operating Temperature Range	T_{opr}	−20～75	℃
Storage Temperature Range	T_{stg}	−40～125	℃

(note) At SW ON. (3 sec. at motor locked or 100msec at duty factor less than 0.1%)

■ ELECTRICAL CHARACTERISTICS

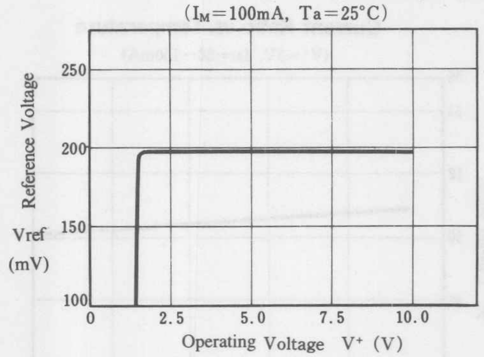
(Ta=25℃, V^+=3V, I_M=100mA)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}		—	2.4	6.0	mA
Output Saturation Voltage						
NJM2606	V_{OSAT}		—	0.18	0.3	V
NJM2606A	V_{OSAT}		—	0.13	0.18	V
Reference Voltage	V_{REF}		0.18	0.20	0.22	V
vs. Operating Voltage	ΔV_{RSV}	V^+=1.8V～8.0V	—	0.7	8.0	mV
vs. Output Current	ΔV_{ROC}	I_M=20mA～200mA	—	2.7	9.0	mV
vs. Ambient Temperature	ΔV_{RT}	Ta=−20°C～+75°C	—	0.04	—	mV/°C
Current Ratio	K	I_M=50mA～150mA	45	50	55	
vs. Operating Voltage	ΔK_{SV}	V^+=1.8V～8.0V I_M=50mA～150mA	—	0.6	3.0	
vs. Output Current	ΔK_{OC}	I_M=(20～50)～(170～200)mA	—	1.0	4.0	
vs. Ambient Temperature	ΔK_{TC}	Ta=−20°C～+75°C I_M=50mA～150mA	—	1.0	—	1/°C

■ TYPICAL CHARACTERISTICS

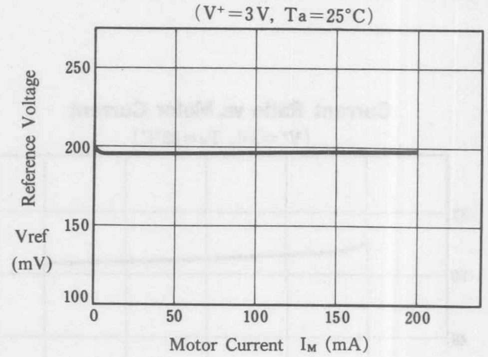
Reference Voltage vs. Operating Voltage

(I_M=100mA, Ta=25°C)



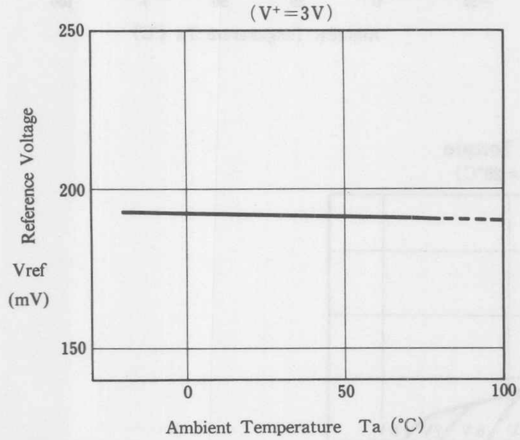
Reference Voltage vs. Motor Current

(V^+=3V, Ta=25°C)



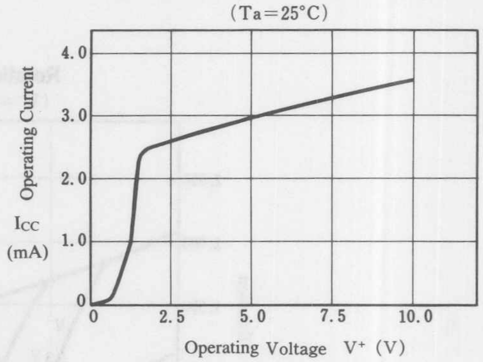
Reference Voltage vs. Temperature

(V^+=3V)



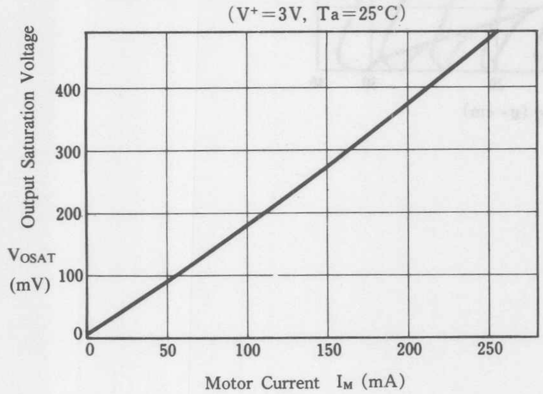
Operating Current vs. Operating Voltage

(Ta=25°C)



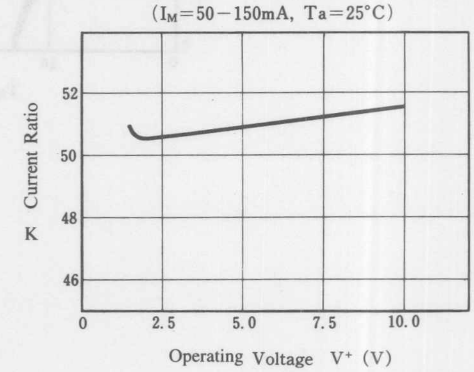
Output Staturation Voltage vs. Motor Current

(V^+=3V, Ta=25°C)



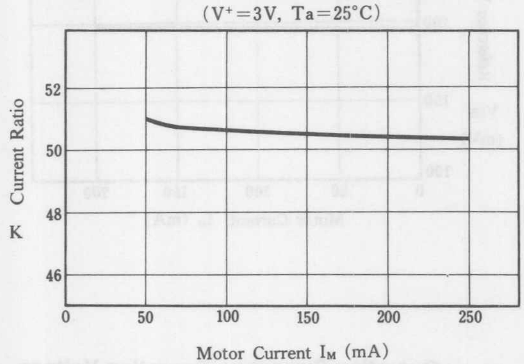
Current Ratio vs. Operating Voltage

(I_M=50−150mA, Ta=25°C)

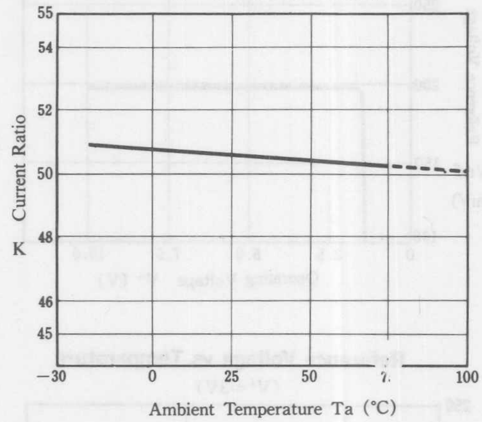


■ TYPICAL CHARACTERISTICS

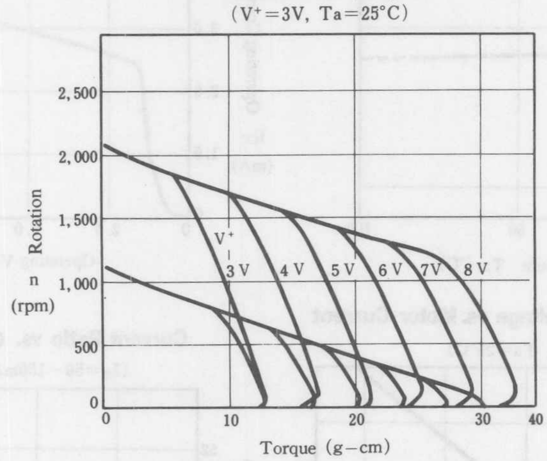
Current Ratio vs. Motor Current
($V^+=3V$, $Ta=25°C$)



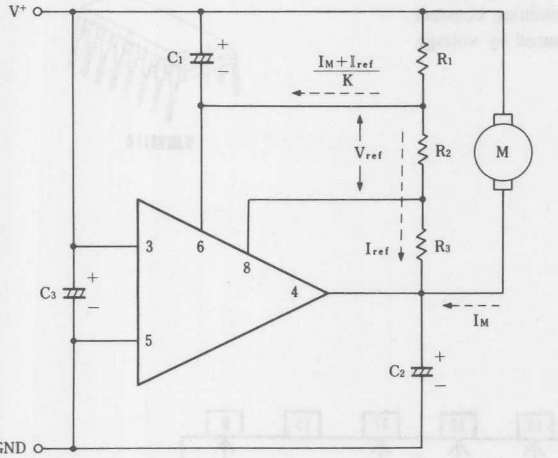
Current Ratio vs. Temperature
($V^+=3V$, $I_M=50\sim150mA$)



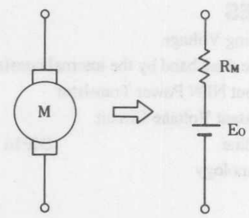
Rotation vs. Torque
($V^+=3V$, $Ta=25°C$)



■ TYPICAL APPLICATION



Select C_1, C_2, C_3 for each motor type.



V_{ref} : Reference Voltage
K : Current Ratio
I_M : Motor Current
R_M : Internal Resistance of Motor
E_O :Motor Counter Electromotive Voltage

The voltage applied at the motor is set as V_M, which brings the following formula.

$$V_M=(R_1+R_2+R_3)I_{ref}+R_1\cdot\frac{I_M+I_{ref}}{K}$$

Now that, $I_{ref}=V_{ref}/R_2$ so that, ($I_{ref}\fallingdotseq 100\mu A$ setting is appropriate)

$$V_M=\frac{V_{ref}}{R_2}(R_1+\frac{R_1}{K}+R_2+R_3)+\frac{R_1}{K}I_M \cdots\cdots(1)$$

On the other hand, the voltage applied at the motor itself will be as in the following.

$$V_M=E_O+R_M\cdot I_M \quad \cdots\cdots(2)$$

Through (1), (2), and then leading to stabilize the control system.

$$R_M\cdot I_M>\frac{R_1}{K}\cdot I_M$$

$$\therefore R_1<K\cdot R_M \cdots\cdots(3)$$

Taking in consideration of deviatons , $R_{1(MAX)}<K_{(MIN)}\cdot R_{M(MIN)}$ with the condition.

Items required checking in regard to the temperature coefficient

IC items

1. Reference voltage: Temperature coefficient of V_{ref}.
2. Current Ratio: Temperature coefficient of K

※1 External component items

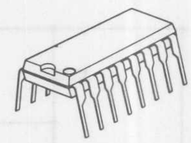
3. Temperature coefficient of R_1, R_2 and R_3
   The relation among these 3 parts takes the very important roll.
4. Temperature coefficient of motor internal resistance
5. Temperature coefficient of motor generative voltage
6. Temperature coefficient ratio of R_1 and R_M
   Count up from 3. 4.

SERVO MOTOR CONTROLLER

■ GENERAL DESCRIPTION

The NJM2611 is an integrated circuit to be applied on servo motor of radio controlled operation. Wide range of operating voltage, and the NJM2611 has the feature of internal circuit of maintaining constant voltage which helps stabilizing from fluctuation caused by voltage source and the ambient temperature.

■ PACKAGE OUTLINE

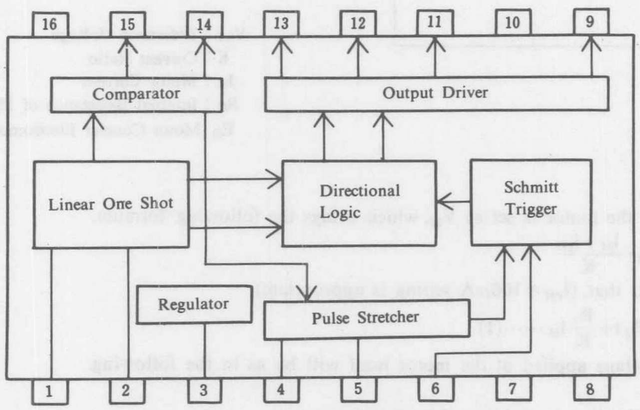


NJM2611D

■ FEATURES

- Wide Operating Voltage
- Setting up the dead band by the internal constant
- Internal Output NPN Power Transistor
- Internal Constant Voltahe Circuit
- Package Outline DIP16
- Bipolar Technology

■ BLOCK DIAGRAM



NJM2611D

■ ABSOLUTE MAXIMUM RATINGS

(V^+=6V, Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	10.0	V
Power Dissipation	P_D	700	mW
Output Sink Current	I_{sink}	600(note)	mA
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

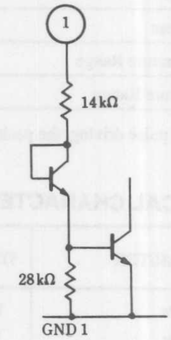
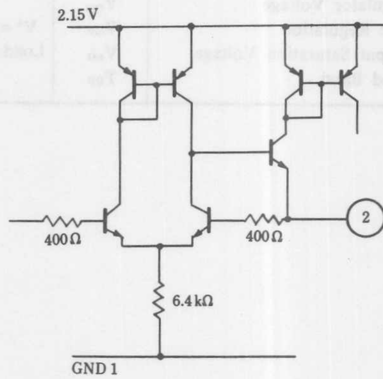
(note) Due to the pulse driving, the peak current must be maintained within the range of the maximum ratings.

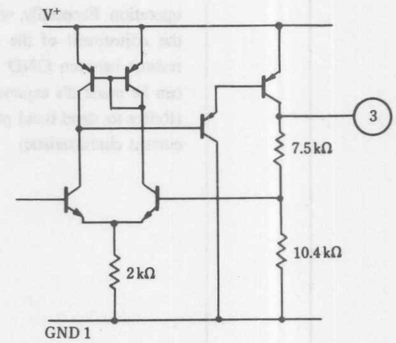
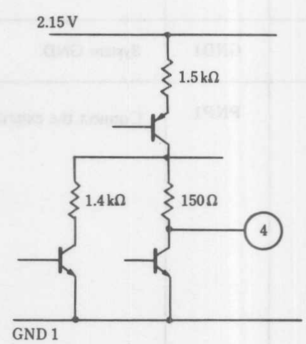
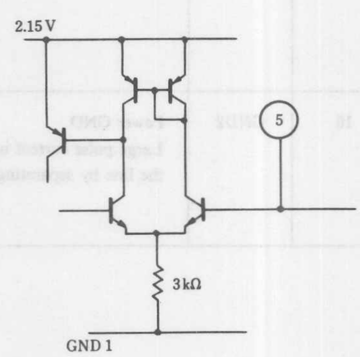
■ ELECTRICAL CHARACTERISTICS

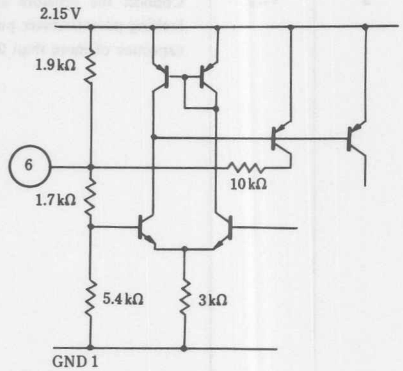
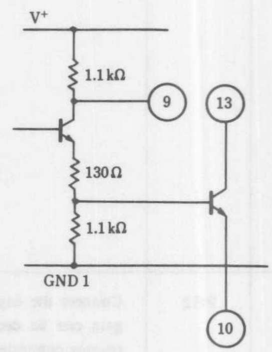
(V^+=6V, Ta=25℃)

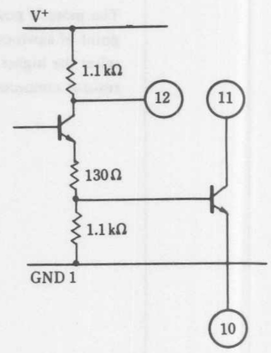
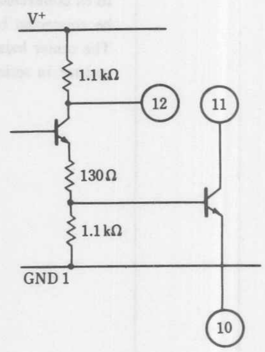
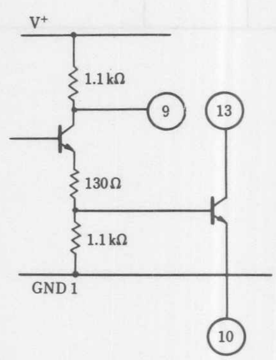
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		2.5	—	7.5	V
Operating Current	I_{CC}		—	7.5	10.0	mA
Minimum Input Pulse Voltage Range	V_{IN}	At the balanced output	1.85	—	—	V
Regulator Voltage	V_{reg}		2.0	2.15	2.3	V
Line Regulation	V_{lin}	V^+=2.5～8.5V	—	—	30	mV
Output Saturation Voltage	V_{sat}	Load 12Ω	—	—	0.5	V
Dead Band	T_{DB}		—	4.0	—	μs

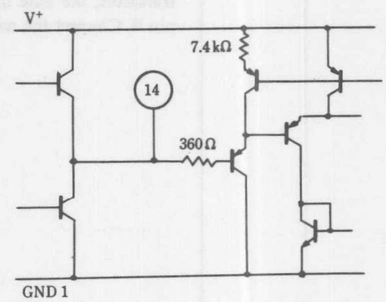
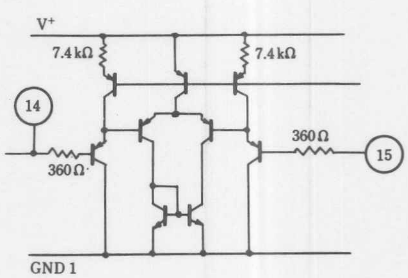
■ PIN DISCRIPTION

PIN NO.	PIN FUNCTION	DESCRIPTION	INSIDE EQUIVAALEUT CIRCUIT
1	V_{IN}	Input the positive pulse of more than 1.85V.	
2	R_{REF}	Constant output voltoge of 1.25V (typical). Through the resistor which is connected to this pin, and setting up the constant current to make the saw tooth sweep at pin 14. Connect the capacitor of approximately 1000 pF with the resistor on parallel.	

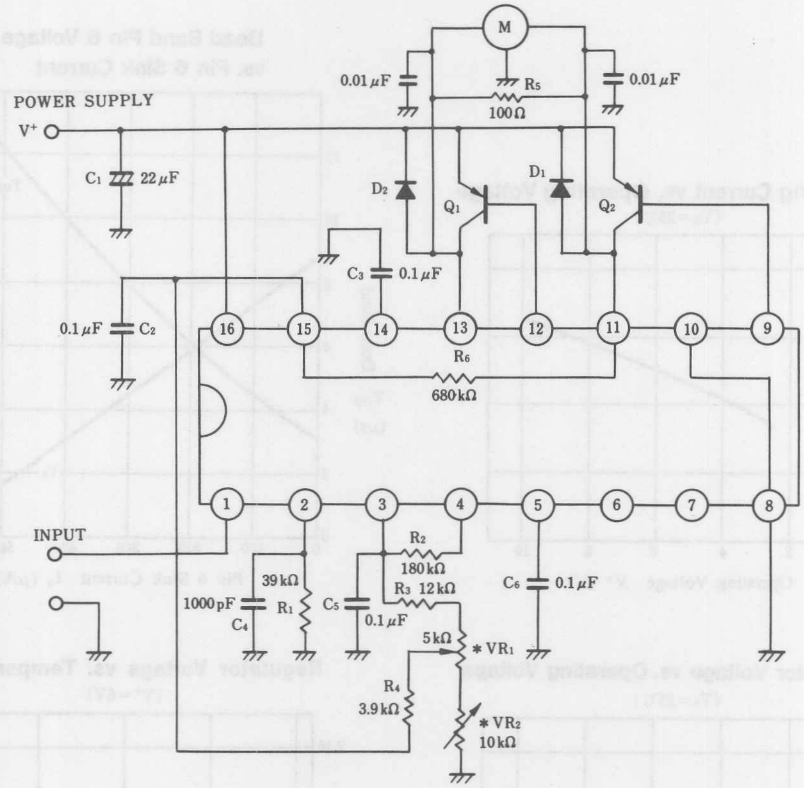
PIN NO.	PIN FUNCTION	DESCRIPTION	INSIDE EQUIVAALEUT CIRCUIT
3	V_{reg}	Connect the resistors along to the motor interlocking potentiometer pulse stretcher. Connect the capacitor of more than $0.1\mu F$.	
4	PS1	Connect the resistor between Vref. The pulse gain can be decided by this resistor and the capacitor connected to pin 5.	
5	PS2	Connect the capacitor between GND. The pulse gain can be decided by this condensor and the resistor connected to pin 4.	

PIN NO.	PIN FUNCTION	DESCRIPTION	INSIDE EQUIVAALEUT CIRCUIT
6	PSV	Nomally, this pin is used on the open state of operation. Especially, when it is reguired to make the adjustment of the dead band, connect the resistor between GND and then the dead band can be made it's expansion. (Refere to, dead band pin 6 voltage vs. pin 6 sink current characteristic)	
7	NC	No connect	
8	GND1	System GND.	
9	PNP1	Connect the external PNP transistor (Q_2) base.	
10	GND2	Power GND Large pulse current is running, therefore, connect the line by separating from the sytem GND.	

PIN NO.	PIN FUNCTION	DESCRIPTION	INSIDE EQUIVAALEUT CIRCUIT
11	OUT1	Connect the collector of the external PNP transistor, the base of which is connected to pin 9. Connect the motor between pin 13.	
12	PNP2	Connect the external PNP transistor (Q_1) base.	
13	OUT2	Connect the collector of the external PNP transistor, the base of which is connected to pin 12. Connect the motor between pin 11.	

PIN NO.	PIN FUNCTION	DESCRIPTION	INSIDE EQUIVAALEUT CIRCUIT
14	C_P	Connect the sawtooth wave generating capacitor. The motor's position shall be decided at the peak point of sawtooth wave, so that it is advisabled to select the higher precision capacitor as well as the resistor connected to pin 2.	
15	COMP	The center part of potentiometer of motor motion is to be connected. The capacitor of about $0.1\mu F$ is to be connected between GND for preventing noise. The center location can be adjusted by putting the resistor in series with the potentiometer.	
16	V+	Power Supply	

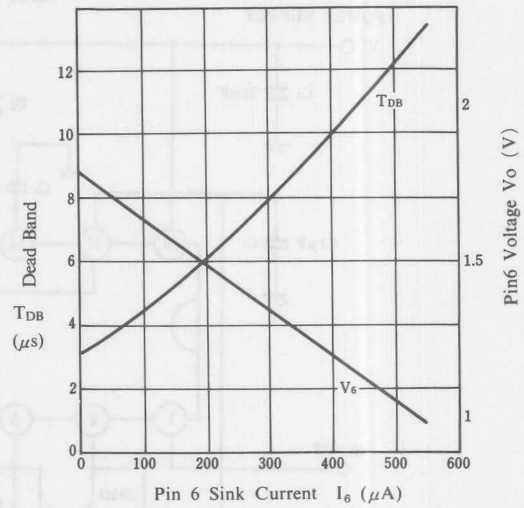
■ TYPICAL APPLICATION



Notes
(1) VR_1 : Potentiometer coupled mechanically to the servo motor
(2) VR_2 : Adjusting the motor center location
(3) Hunching prevention
0.01 μF Capacitor between pin 11 and GND
0.01 μF Capacitor between pin 13 and GND
Diode between pin 11 and power supply
Diode between pin 13 and power supply
100Ω Resistor between pin 11 and pin 13
680kΩ Resistor between pin 11 and GND

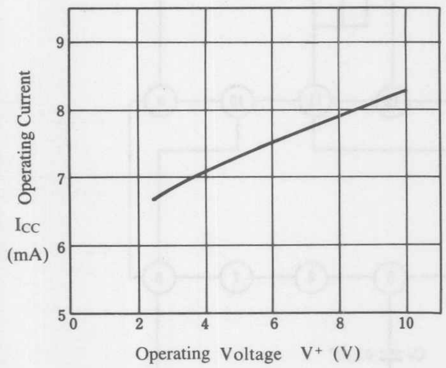
■ TYPICAL CHARACTERISTICS

Dead Band Pin 6 Voltage vs. Pin 6 Sink Current



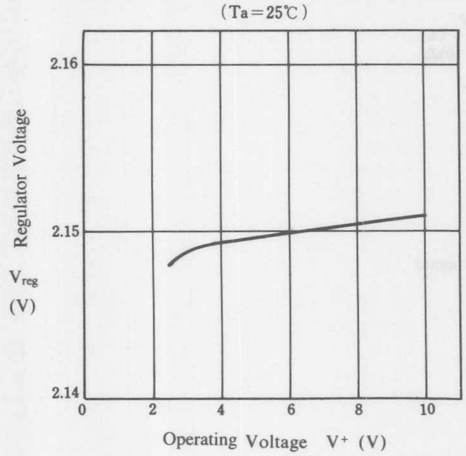
Operating Current vs. Operating Voltage

(Ta=25℃)



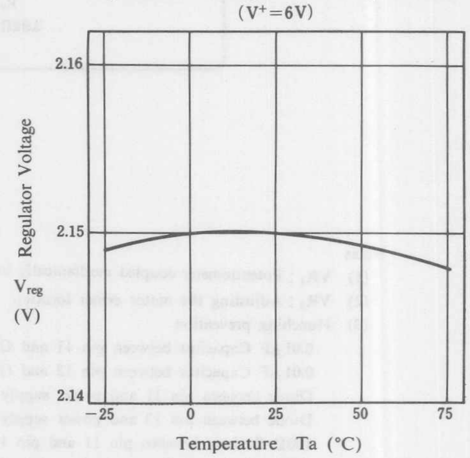
Regulator Voltage vs. Operating Voltage

(Ta=25℃)



Regulator Voltage vs. Temperature

(V^+=6V)



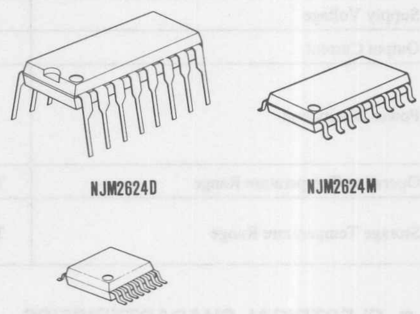
BRUSH LESS DC MOTOR PRE-DRIVER

■ GENERAL DESCRIPTION

The NJM2624 is a 3-phase brushless DC motor pre-driver which requies external power-transistors suited to drive current of the motor.

The Run Enable function is used as PWM control besides of ON/OFF switch function.

■ PACKAGE OUTLINE



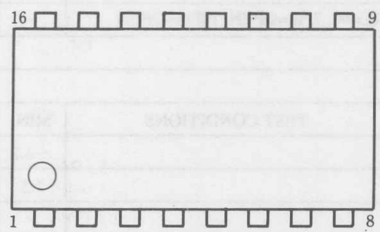
NJM2624D NJM2624M

NJM2624V

■ FEATURES

● Operating Voltage	(+4.5V~+18V)
● Low Operating Current	(10mA max)
● Output Switch Current	(90mA typ.)
● Run Enable	
● Forward or Reverse Direction	
● Bipolar Technology	
● Package Outline	DIP16, DMP16, SSOP16

■ PIN CONFIGURATION

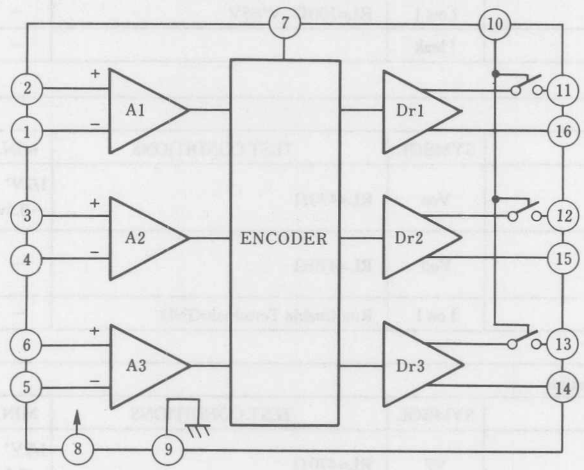


NJM2624D
NJM2624M
NJM2624V

PIN FUNCTION

1 : H1−	9 : GND
2 : H1+	10 : ON/OFF
3 : H2+	11 : OUT1
4 : H2−	12 : OUT3
5 : H3−	13 : OUT5
6 : H3+	14 : OUT6
7 : F/R	15 : OUT4
8 : V⁺	16 : OUT2

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	20	V
Output Current	Io	100	mA
Power Dissipation	P_D	(DMP-16) 700 (DMP-16) 300 (SSOP-16) 300	mW
Operating Temperature Range	T_{opr}	−40〜+85	℃
Storage Temperature Range	T_{stg}	(D, M type-16) −40〜+150	℃
		(V type) −40〜+125	℃

■ ELECTRICAL CHARACTERISTICS

(V^+=12V, Ta=25℃)

Total Device

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+		4.5	−	18	V
Supply Current	Iq	RL=∞, 7Pin=OPEN, 10Pin=OPEN	−	3.7	10	mA

Hole Sensor Section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	Vio		−4.2	−	4.2	mV
Input Common mode Voltage range	Vicm		1.5	−	10.5	V
Input Bias Current	Ib		−	−	600	nA

Output Section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage 1	Vout 1	RL=470Ω, V^+=12V	8.9	9.5	−	V
Output Voltage 2	Vout 2	RL=470Ω, V^+=5V		3.5		V
Maximum Output Current 1	I out 1	RL=100Ω, V^+=12V	50	90	−	mA
Maximum Output Current 2	I out 1	RL=100Ω, V^+=5V	−	30	−	mA
Output Leak Current	I leak		−	−	5	μA

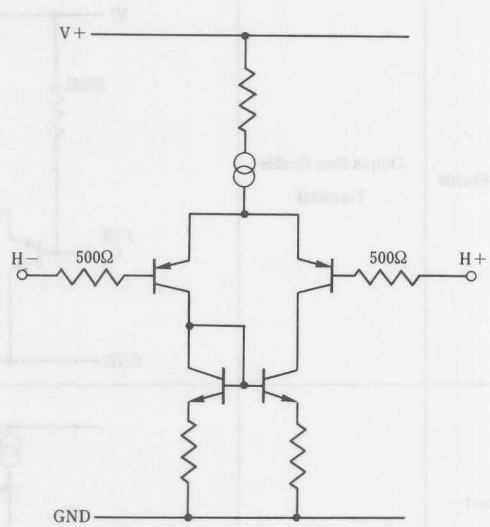
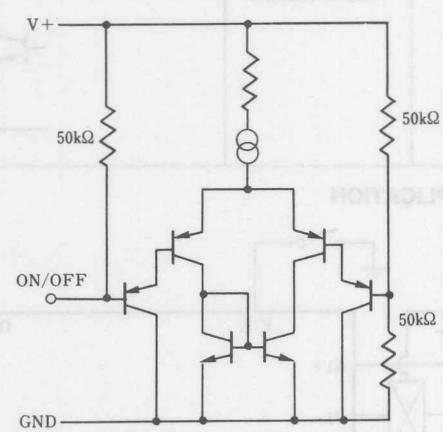
Run Enable Section

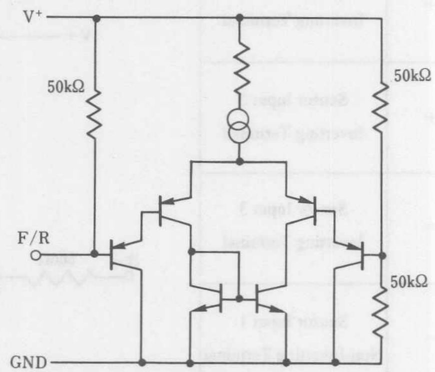
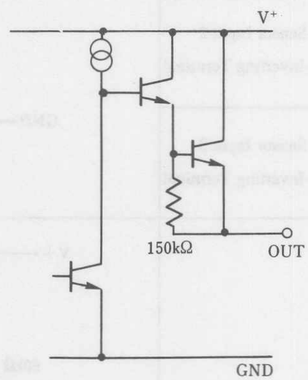
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Run Enable Voltage	Von	RL=470Ω	$1/2V^+$ −0.5v	−	−	V
Run Disable Voltage	Voff	RL=470Ω	−	−	$1/2V^+$ +0.5v	V
Source Current 1	I on 1	Run Enable Terminal=GND	−	250	400	μA

Forward or Reverse Direction Section

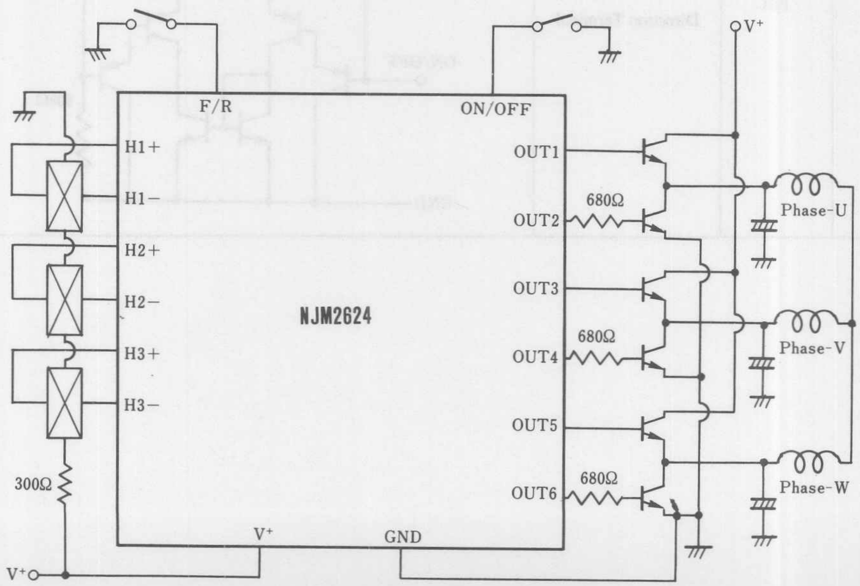
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Forward Direction	VF	RL=470Ω	$1/2V^+$ −0.5v	−	−	V
Reverse Direction	VR	RL=470Ω	−	−	$1/2V^+$ +0.5v	V
Source Current 1	I on 2	Forward or Reverse Direction Terminal=GND	−	250	400	μA

■ TERMINAL DESCRIPTION

PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
2	H1+	Sensor Input 1 Inverting Terminal	
3	H2+	Sensor Input 2 Inverting Terminal	
6	H3+	Sensor Input 3 Inverting Terminal	
1	H1−	Sensor Input 1 Non-Inverting Terminal	
4	H2−	Sensor Input 2 Non-Inverting Terminal	
5	H3−	Sensor Input 3 Non-Inverting Terminal	
7	F/R	Forward or Reverse Direction Terminal	

PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
8	V^+	Power Supply	—
9	GND	Ground	—
10	Run Enable	Output Run Enable Terminal	
11 12 13 14 15 16	Out1 Out3 Out5 Out6 Out4 Out2	Internal Switching Transistor : Emitter Follower	

■ TYPICAL APPLICATION

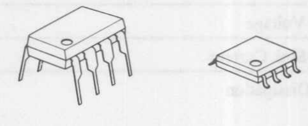


V-F/F-V CONVERTOR

■ GENERAL DESCRIPTION

The NJM4151 provide a simple low-cost method of A/D conversion. They have all the inherent advantages of the voltage-to-frequency conversion technique. The Output of NJM4151 is a series of pulses of constant duration. The frequency of the pulses is proportional to the applied input voltage. These converters are designed for use in a wide range of data conversion and remote sensing applications.

■ PACKAGE OUTLINE

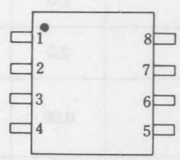


NJM 4151 D　　NJM 4151 M

■ FEATURES

- Operating Voltage (8V ~ 22V)
- Frequency Operation from (1.0Hz to 100kHz)
- Package Outline DIP8, DMP8
- Bipolar Technology

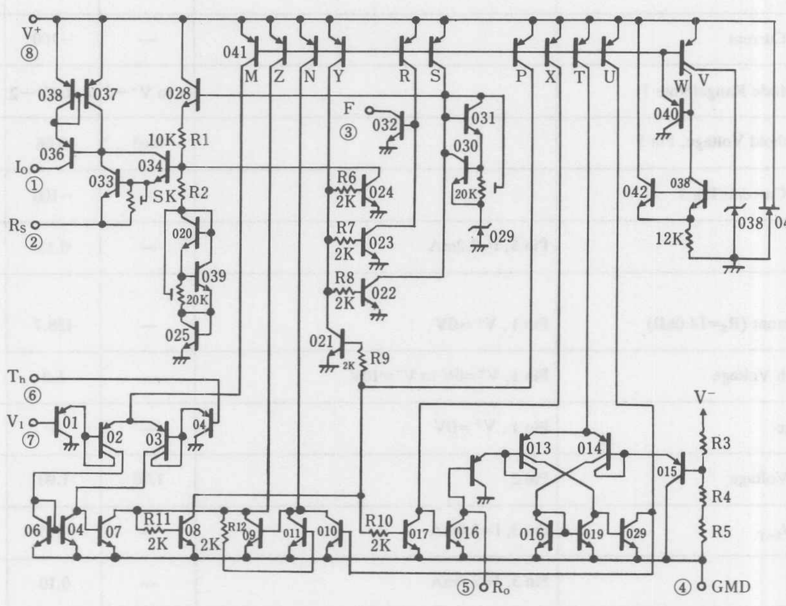
■ PIN CONFIGURATION



NJM4141D
NJM4151M

PIN FUNCTION
1 Current Source
2 Scale Factor
3 Logic Output
4 Ground
5 One-Shot R, C
6 Threshold
7 Input Voltage
8 V^+

■ EQUIVALENT CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8~22	V
Output Sink Current	I_{SINK}	20	mA
Power Dissipation	P_D	(DIP8) 500 (DMP8) 300	mW mW
Input Voltage	V_I	$-0.2\sim V^+$	(V)
Operating Temperature Range	T_{opr}	−20~+75	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

■ ELECTRICAL CHARACTERISTICS

($V^+=+15V$, Ta=+25℃)

PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	$8V<V^+<15V$	2.0	3.5	6.0	mA
	$15V<V^+<22V$	2.0	4.5	7.5	mA
Conversion Accuracy Scale Factor	$V_{IN}=10V$ $R_S=14.0k\Omega$	0.90	1.00	1.10	kHz/V
Drift with Temperature	$V_{IN}=10V$		±100	—	ppM/°C
Drift with V^+	$V_{IN}=1.0V$ $8V<V^+<18V$	—	0.2	1.0	%/V
Input Comparator Offset Voltage		—	5	10	mV
Offset Current		—	±50	±100	nA
Input Bias Current		—	−100	−300	nA
Common Mode Range(Note 1)		0 to V^+-3	0 to V^+-2	—	V
One-Shot Threshold Voltage, Pin 5		0.63	0.66	0.70	$\times V^+$
Input Bias Current, Pin 5		—	−100	−500	nA
Reset V_{SAT}	Pin 5, I=2.2mA	—	0.15	0.50	V
Current Source Output Current ($R_S=14.0k\Omega$)	Pin 1, $V^+=0V$	—	138.7	—	μA
Change with Voltage	Pin 1, $V^+=0V$ to $V^+=10V$	—	1.0	2.5	μA
Off Leakage	Pin 1, $V^+=0V$	—	1	50.0	nA
Reference Voltage	Pin 2	1.70	1.90	2.08	V
Logic Output V_{SAT}	Pin 3, I=3.0mA	—	0.15	0.50	V
V_{SAT}	Pin 3, I=2.0mA	—	0.10	0.30	V
Off Leakage		—	0.1	1.0	μA

Note 1: Input Common Mode Range includes ground.

■ PRINCIPLE OF OPERATION

Single Supply Mode Voltage-to-Frequency Conversion

In this application the NJM4151 functions as a stand-alone voltage to frequency converter operating on a single positive power supply. Refer to Figure 1, the simplified block diagram. The NJM4151 contains a voltage comparator, a one-shot, and a precision switched current source. The voltage comparator compares a positive input voltage applied at pin 7 to the voltage at pin 6. If the input voltage is higher, the comparator will fire the one-shot. The output of the one-shot is connected to both the logic output and the precision switched current source. During the one-shot period, T, the logic output will go low and the current source will turn on with current I.

At the end of the one-shot period the logic output will go high and the current source will shut off. At this time the current source has injected an amount of charge $Q=I_OT$ into the network R_B-C_B. If this charge has not increased the voltage V_B such that $V_B>V_I$, the comparator again fires the one-shot and the current source injects another lump of charge, Q, into the R_B-C_B network. This process continues until $V_B>V_I$.

When this condition is achieved the current source remains off and the voltage V_B decays until V_B is again equal to V_I. This completes one cycle. The VFC will now run in a steady state mode. The current source dumps lumps of charge into the capacitor C_B at rate fast enough to keep $V_B \geqq V_I$. Since the discharge rate of capacitor C_B is proportional to V_B/R_B, the frequency at which the system runs will be proportional to the input voltage.

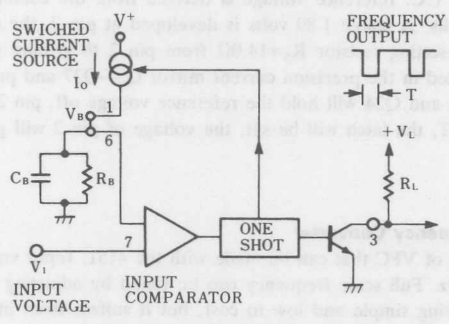


Figure 1. Simplified Block Diagram, Single Supply Mode

The 4151 VFC is easy to use and apply if you understand the operation of it through the block diagram, Figure 1. Many users, though, have expressed the desire to understand the workings of the internal circuitry. The circuit can be divided into five sections: the internal biasing network, input comparator, one-shot, voltage reference, and the output current source.

The internal biasing network is composed of Q39-Q43. The N-channel FET Q43 supplies the initial current for zener diode Q39. The NPN transistor Q38 senses the zener voltage to derive the current reference for the multiple collector current source Q41. This special PNP transistor provides active pull-up for all of the other sections of the 4151.

The input comparator section is composed of Q1-Q7. Lateral PNP transistors Q1-Q4 form the special ground-sensing input which is necessary for VFC operation at low input voltages. NPN transistors Q5 and Q6 convert the differential signal to drive the second gain stage Q7. If the voltage on input pin 7 is less than that on threshold pin 6, the comparator will be off and the collector of Q7 will be in the high state. As soon as the voltage on pin 7 exceeds the voltage on pin 6, the collector of Q7 will go low and trigger the one-shot.

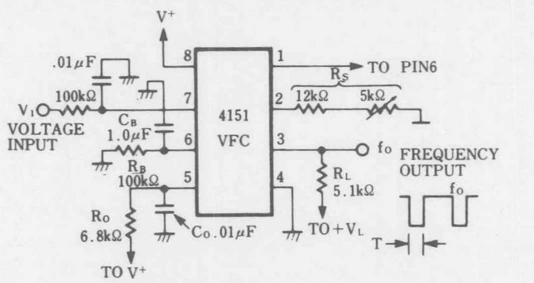
The one-shot is made from a voltage comparator and an R-S latch. Transistors Q12-Q15 and Q18-Q20 form the comparator, while Q8-Q11 and Q16-Q17 make up the R-S latch. One latch output, open-collector reset transistor Q16, is connected to a comparator input and to the terminal, pin 5. Timing resistor R_O is tied externally from pin 5 to V^+ and timing capacitor C_O is tied from pin 5 to ground. The other comparator input is tied to a voltage divider R_3-R_5 which sets the comparator threshold voltage at 0.667 V^+. One-shot operation is initiated when the collector of Q7 goes low and sets the latch. This causes Q16 to turn off, releasing the voltage at pin 5 to charge exponentially towards V^+ through R_O. As soon as this voltage reaches 0.667 V^+, comparator output Q20 will go high causing Q10 to reset the latch. When the latch is reset, Q16 will discharge C_O to ground. The one-shot has now completed its function of creating a pulse of period $T=1.1\ R_OC_O$ at the latch output, Q21. This pulse is buffered through Q23 to drive the open-collector logic circuit transistor Q32. During the one-shot period the logic output will be in the low state. The one-shot output is also used to switch the reference voltage by Q22 and Q24. The low T.C. reference voltage is derived from the combination of a 5.5V zener diode with resistor and diode level shift networks. A stable 1.89 volts is developed at pin 2, the emitter of Q33.

Connecting the external current-setting resistor $R_S=14.0\Omega$ from pin 2 to ground gives $135\mu A$ from the collectors of Q33 and Q34. This current is reflected in the precision current mirror Q35-Q37 and produces the output current I_O at pin 1. When the R-S latch is reset, Q22 and Q24 will hold the reference voltage off, pin 2 will be at 0V, and the current will be off. During the one-shot period T, the latch will be set, the voltage of pin 2 will go to 1.89V, and the output current will be switched on.

■ TYPICAL APPLICATION

1. Single supply Voltage-to-Frequency Converter

Figure 2 shows the simplest type of VFC that can be made with the 4151. Input voltage range is from 0 to +10V, and output frequency is from 0 to 10kHz. Full scale frequency can be tuned by adjusting R_S, the output current set resistor. This circuit has the advantage of being simple and low in cost, but it suffers from inaccuracy due to a number of error sources. Linearity error is typically 1%. A frequency offset will also be introduced by the input comparator offset voltage. Also, response time for this circuit is limited by the passive integration network R_BC_B. For the component values shown in Figure 2, response time for a step change input from 0 to +10V will be 135msec. For applications which require fast response time and high accuracy, use the circuits of Figure 3 and 4.



DESIGN EQUATIONS

$$f_O=KV_I \quad \text{Where } K=0.486\frac{R_S}{R_BR_OC_O}\ \frac{Hz}{V}$$

$$T=1.1R_OC_O$$

Figure 2. Single Supply Voltage-to-Frequency Converter

2. Precision VFC with Single Supply Voltage

For applications which require a VFC which will operate from a single positive supply with positive input voltage, the circuit of Figure 3 will give greatly improved linearity, frequency offset, and response time. Here, an active integrator using one section of the NJM3403A quad ground-sensing op-amp has replaced the R_B-C_B network in Figure 2. Linearity error for this circuit is due only to the 4151 current source output conductance. Frequency offset is due only to the op-amp input offset and can be nulled to zero by adjusting R_B. This technique uses the op-amp bias current to develop the null voltage, so an op-amp with stable bias current, like the NJM3403A, is required.

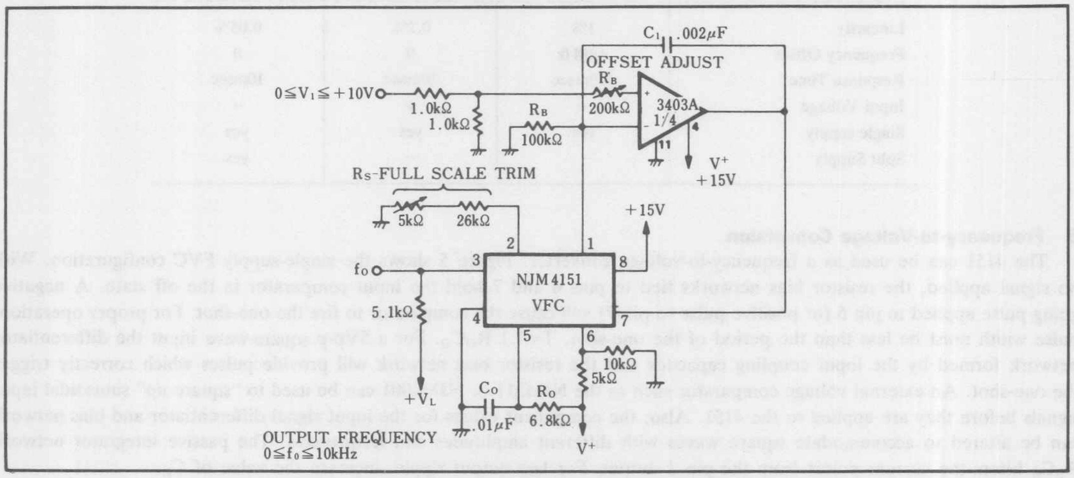


Figure 3. Precision Voltage-to-Frequency Converter Single Supply

3. Precision Voltage-to-Frequency Converter

In this application (Figure 4) the 4151 VFC is used with an operational amplifier integrator to provide typical linearity of 0.05% over the range of 0 to −10V. Offset is adjustable to zero. Unlike many VFC designs which lose linearity below 10mV, this circuit retains linearity over the full range of input voltage, all the way to 0V.

Trim the full scale adjust pot at $V_I = -10V$ for an output frequency of 10kHz. The offset adjust pot should be set for 10Hz with an input voltage of −10mV.

The 4131 operational amplifier integrator improves linearity of this circuit over that of Figure 2 by holding the output of the source, Pin 1, at a constant 0V. Therefore linearity error due to the current source output conductance is eliminated. The diode connected around the op-amp prevents the voltage at 4151 pin 7 from going below 0. Use a low-leakage diode here, since any leakage will degrade the accuracy. This circuit can be operated from a single positive supply if an NJM3403A ground-sensing op-amp is used for the integrator. In this case, the diode can be left out. Note that even though the circuit itself will operate from a single supply, the input voltage is necessarily negative. For operation above 10kHz, bypass 4151 pin 6 with 0.01µF.

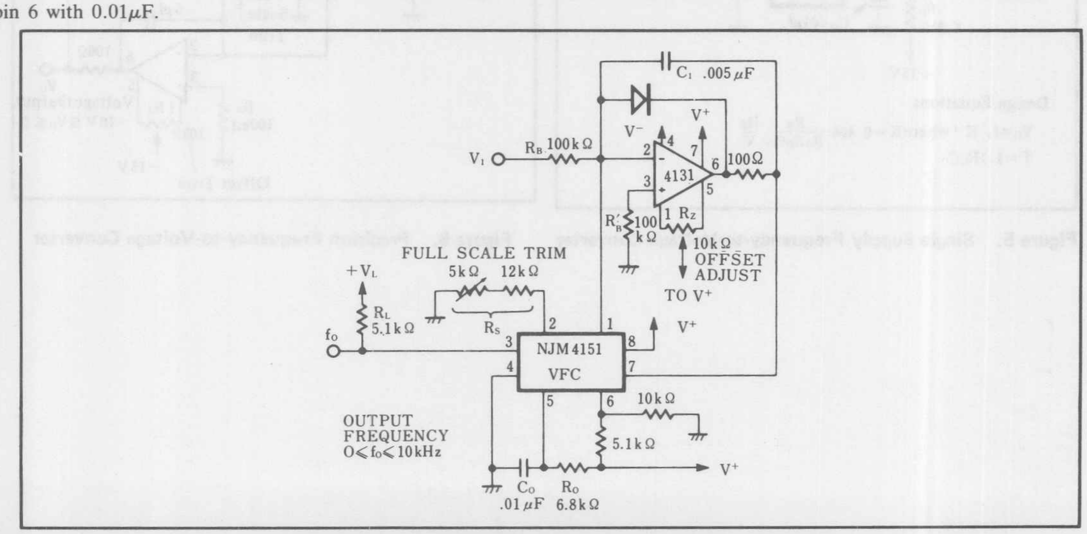


Figure 4. Precision Voltage-to-Frequency Converter

4. Comparison of Voltage-to-Frequency Application Circuits

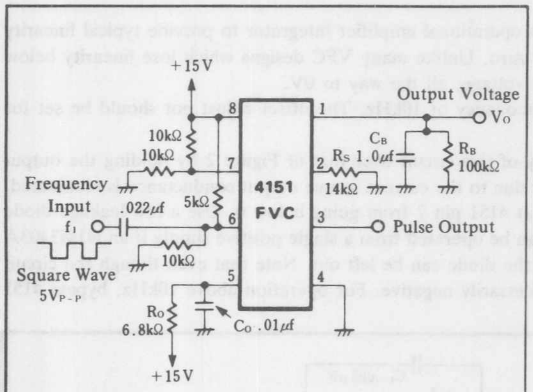
Table 1 compares the VFC applications circuits for typical linearity, frequency offset, response time for a step input from 0 to 10 volts, sign of input voltage, and whether the circuit will operate from a single positive supply or split supplies.

Table 1

	Figure 2	Figure 3	Figure 4
Linearity	1%	0.2%	0.05%
Frequency Offset	+10Hz	0	0
Response Time	135msec	10msec	10msec
Input Voltage	+	+	−
Single supply	yes	yes	yes
Split Supply	−	−	yes

5. Frequency-to-Voltage Conversion

The 4151 can be used as a frequency-to-voltage converter. Figure 5 shows the single-supply FVC configuration. With no signal applied, the resistor bias networks tied to pins 6 and 7 hold the input comparator in the off state. A negative going pulse applied to pin 6 (or positive pulse to pin 7) will cause the comparator to fire the one-shot. For proper operation, pulse width must be less than the period of the one-shot, $T=1.1\ R_OC_O$. For a 5Vp-p square-wave input the differentiator network formed by the input coupling capacitor and the resistor bias network will provide pulses which correctly trigger the one-shot. An external voltage comparator such as the NJM311 or NJM2901 can be used to "square-up" sinusoidal input signals before they are applied to the 4151. Also, the component values for the input signal differentiator and bias network can be altered to accommodate square waves with different amplitudes and frequencies. The passive integrator network R_BC_B filters the current pulses from the pin 1 output. For less output ripple, increase the value of C_B.



Design Equations

$V_O = f_I \cdot K^{-1}$ where $K = 0.486\ \frac{R_S}{R_BR_OC_O}\ \frac{Hz}{V}$

$T = 1.1R_OC_O$

Figure 5. Single Supply Frequency-to-Voltage Converter

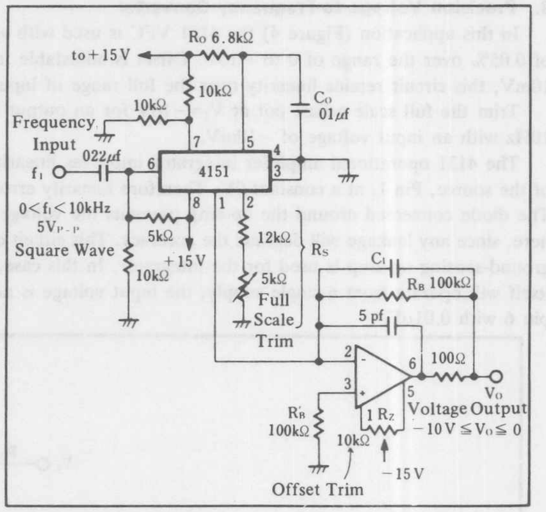


Figure 6. Precision Frequency-to-Voltage Converter

6. Precision Frequency-to-Voltage Converter

For increased accuracy and linearity, use an operational amplifier integrator as shown in Figure 6, the precision FVC configuration. Trim the offset to give −10mV out with 10Hz in and trim the full scale adjust for −10V out with 10kHz in. Input signal conditioning for this circuit is necessary just as for the single supply mode, and scale factor can be programmed by the choice of component values. A tradeoff exists between output ripple and response time, through the choice of integration capacitor C_1. If $C_1=0.1\mu F$ the ripple will be about 100mV. Response time constant $\tau_R=R_B \cdot C_1$. For $R_B=100k\Omega$ and $C_1=0.1\mu F$, $\tau_R=10ms$

■ PRECAUTIONS

1. The voltage applied to comparator input pins 6 and 7 should not be allowed to go below ground by more than 0.3 volt.

2. Pins 3 and 5 are open-collector outputs. Shorts between these pins and V^+ can cause overheating and eventual destruction.

3. Reference voltage terminal pin 2 is connected to the emitter of an NPN transistor and is held at approximately 1.9 volts. This terminal should be protected from accidental shorts to ground or supply voltages. Permanent damage may occur if current in pin 2 exceeds 5mA.

4. Avoid stray coupling between 4151 pins 5 and 7, which could cause false triggering. For the circuit of Figure 2, bypass pin 7 to ground with at least $0.01\mu F$. If false triggering is experienced with the precision mode circuits, bypass pin 6 to ground with at least $0.01\mu F$. This is necessary for operation above 10kHz.

■ PROGRMMING THE 4151

The 4151 can be programmed to operate with a full scale frequency anywhere from 1.0Hz to 100kHz. In the case of the VFC configuration, nearly any full scale input voltage from 1.0V and up can be tolerated if proper scaling is employed. Here is how to determine component values for any desired full scale frequency.

1. Set $Rs=14k\Omega$ or use a $12k\Omega$ resistor and $5k\Omega$ pot as shown in the figures. (The only exception to this is Figure 4.)

2 Set $T=1.1R_0C_0=0.75[1/f_0]$ where f_0 is the desired full scale frequency. For optimum performance make $6.8k\Omega<R_0<680k\Omega$ and $0.001\mu F<C_0<1.0\mu F$

3. a) For the circuit of Figure 2 make $C_B=10^{-2}$ $[1/f_0]$ Farads.
   Smaller values of C_B will give faster response time, but will also increase frequency offset and nonlinearity.
   b) For the active integrator circuits make $C_1=5\times10^{-5}[1/f_0]$ Farads. The op-amp integrator must have a slew rate of at least $135\times10^{-6}[1/C_1]$ volts per second where the value of C_1 is again give in Frads.

4. a) For the circuits of Figure 2 and 3 keep the values of R_B and R_B' as shown and use an input attenuator to give the desired full scale input voltage.
   b) For the precision mode circuit of Figure 4, set $R_B=V_{10}/100\mu A$ where V_{10} is the full scale input voltage. Alternately the op-amp inverting input (summing node) can be used as a current input with full scale input current $I_{10}= -100\mu A$.

5. For the FVCs, pick the value of C_B or C_1 to give the optimum tradeoff between response time and output ripple for the particular application.

■ DESIGN EXAMPLE

I. Design a precision VFC (from Figure 4) with $f_0=100kHz$ and $V_{10}=-10V$.
   1. Set $Rs=14.0k\Omega$.
   2. $T=0.75\ (1/10^5)=7.5\mu sec$ Let $R_0=6.8k\Omega$ and $C_0=0.001\mu F$
   3. $C_1=5\times1^{-5}(1/10^5)=500pF$ Op-amp slew rate must be at lease $SR=135\times10^{-6}(1/500pF)=0.27V/\mu sec$
   4. $R_B=10V/100\mu A=100k\Omega$

II. Design a precision VFC with $f_0=1Hz$ and $V_{10}=-10V$,
   1. Let $Rs=14.0k\Omega$.
   2. $T=0.75(1/1)=0.75sec$ Let $R_0=680k\Omega$ and $C_0=1.0\mu F$
   3. $C_1=5\times10^{-5}(1/1)\ F=50\mu F$
   4. $R_B=100k\Omega$

III. Design a single supply FVC to operate with a supply voltage of 8V and full scale input frequency f_0=83.3Hz. The output voltage must reach at least 0.63 of its final value in 200msec. Determine the output ripple.

1. Set Rs=14.0kΩ.
2. T=0.75(1/83.3)=9msec Let R_0=82kΩ and C_0=0.1μF
3. Since this FVC must operate from 8.0V, we shall make the full scale output voltage at pin 6 equal to 5.0V.
4. R_B=5V/100μA=50kΩ
5. Output response time constant is $\tau_R \leq$20msec Therefore $C_B \leq \tau_R/R_B = 200\times10^{-3}/50\times10^{3}$=4μF Worst case ripple voltage is: V_R=9mS×135μA/4μF=304mV

IV. Design an opto-isolated V_{FC} with high linearity which accepts a full scale input voltage of +10V. See Figure 7 for the final disign. This circuit uses the precision mode VFC configuration for maximum linearity. The NJM3403A quad op-amp provides the functions of inverter, integrator, regulator, and LED driver.

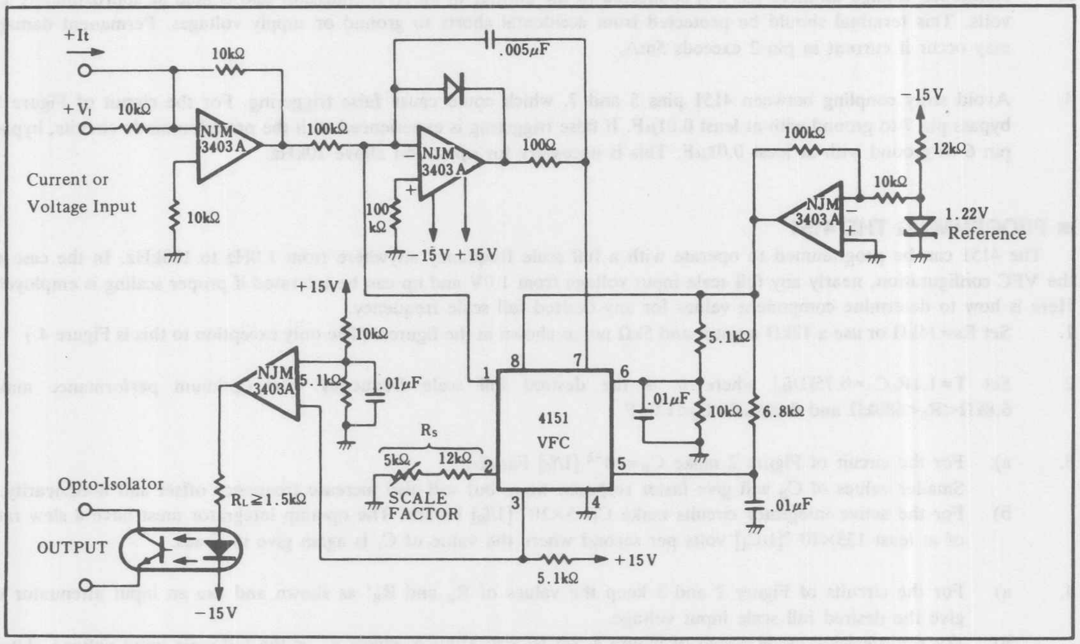
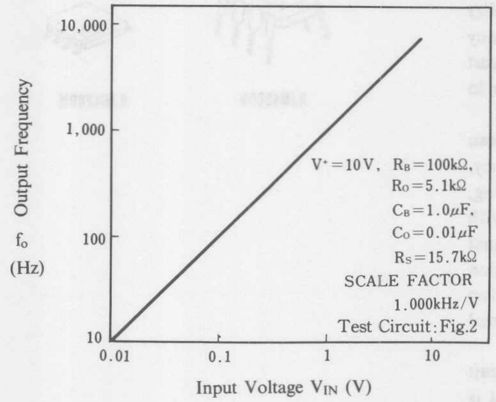


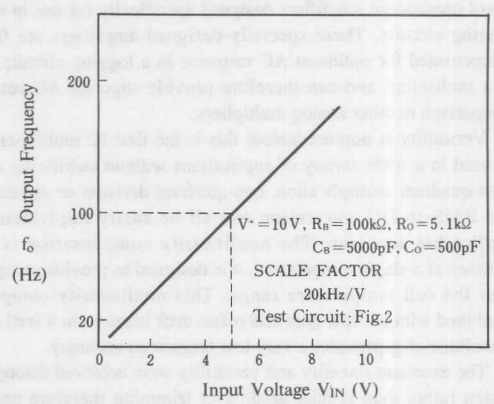
Figure 7. Opto-Isolated VFC

■ TYPICAL CHARACTERISTICS

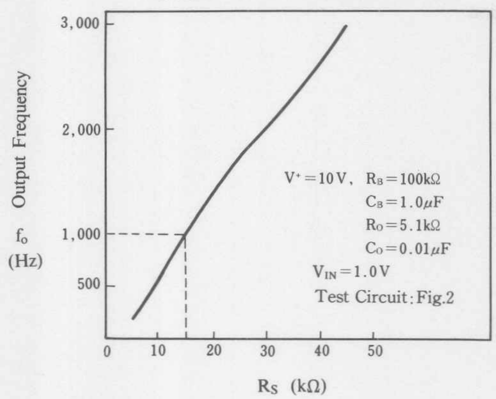
V_{IN}-fo Characteristics (VFC)



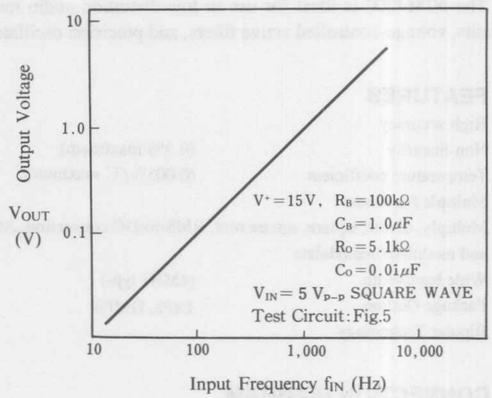
V_{IN}-fo Characteristics (VFC)



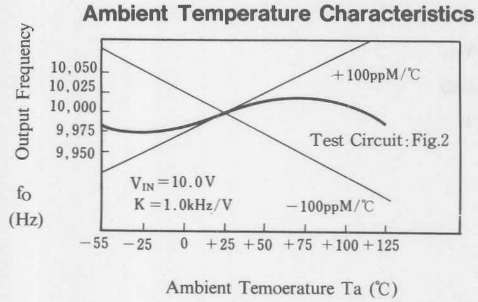
Scale Factor Characteristics



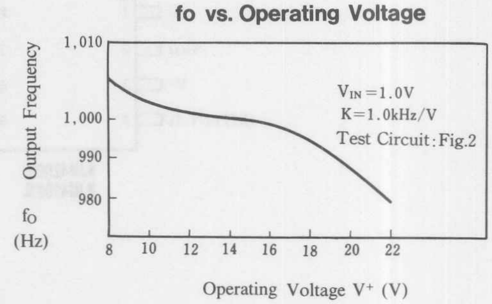
Input Frequency vs. Output Voltage (FVC)



Ambient Temperature Characteristics



fo vs. Operating Voltage



ANALOG MULTIPLIER

■ GENERAL DESCRIPTION

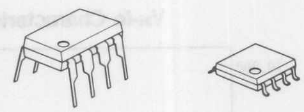
The NJM4200 is the industry's first integrated circuit multiplier to have complete compensation for nonlinearity, the primary source of error and distortion. This is also the first IC mustiplier to have three on-board operational amplifiers designed specifically for use in multiplier logging circuits. These specially-designed amplifiers are frequency compensated for optimum AC response in a logging circuit; the heart of a multiplier, and can therefore provide superior AC response in comparison to other analog multipliers.

Versatility is unprecedented; this is the first IC multiplier that can be used in a wide variety of applications without sacrificing accuracy. Four-quadrant multiplication, one-quadrant division or square-rooting, and RMS-to-DC conversion can all be easily implemented with predictable accuracy. The nonlinearity compensation is not just trimmed at a single temperature, it is designed to provide compensation over the full temperature range. This nonlinearity compensation combined with the low gain and offset drift inherent in a well-designed monolithic chip provides a very low tempco on accuracy.

The excellent linearity and versatility were achieved through circuit design rather than special grading or trimming therefore unit cost is very low. Analog multipliers can now be used in application where price was previously an inhibiting factor.

The NJM4200 is ideal for use in low-distortion audio modulation circuits, voltage-controlled active filters, and precision oscillators.

■ PACKAGE OUTLINE

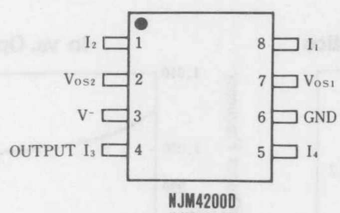


NJM4200D NJM4200M

■ FEATURES

- High accuracy
  - Non-linearity (0.3% maximum)
  - Temperature coefficient (0.005%/℃ maximum)
- Multiple functions
  - Multiply, divide, square, square root, RMS-to-DC conversion, AGC, and modulate/demodulate
- Wide bandwidth (4MHz typ-)
- Package Outline DIP8, DMP8
- Bipolar Technology

■ CONNECTION DIAGRAM



NJM4200D
NJM4200M

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^-	−22	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
Input Current	I_{IN}	−5	mA
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

($Ta=25℃, V^-=-15V$)

PARAMETER	SYMBOL	TEST CONDITION	NJM4200			UNIT
			MIN.	TYP.	MAX.	
Input range(I_1,I_2 and I_4)	I_{IN}		1.0	—	1000	μA
Total error as multiplier						
Untrimmed	—		—	—	±3.0	%
With external trim	—		—	—	±0.5	%
Versus temperature	—	Operational Temperature Range	—	±0.005	—	%/°C
Versus Supply	—	$V^-=-9V\sim-18V$	—	±0.1	—	%/V
Nonlinearity	—	$50\mu A<I<250\mu A$	—	—	±0.3	%
Input offset voltage	V_{IO}	$I_1=I_2=I_4=150\mu A$	—	—	±10	mV
Input bias current	I_B	$I_1=I_2=I_4=150\mu A$	—	—	500	nA
Average temperature coefficient of input offset voltage	—	$I_1=I_2=I_4=150\mu A$	—	—	±100	μV/°C
Output current range(I_3)	I_O	(Note 1)	1.0	—	1000	μA
Frequency response, −3 dB	f_R		—	4	—	MHz
Operating voltage	V^-		−9	−15	−18	V
Operating Current	I_{CC}	$I_1=I_2=I_4=150\mu A$, Ta=25℃	—	—	4	mA

Note 1: These specifications apply with output (I_3) connected to an op amp summing junction. If desired, the output (I_3) at pin (4) can be used to drive a resistive load directly. The resistive load should be less than 700 ohms and must be pulled up to a positive supply such that the voltage on pin (3) stays within a range of 0 to +5V.

■ FUNCTION DESCRIPTION

The NJM4200 multiplier is designed to multiply two input currents (I_1 and I_2) and to divide by a third input current (I_4). The output is also in the form of a current (I_3). A simplified circuit diagram is shown in Figure 1. The nominal relationship between the three inputs and the output is:

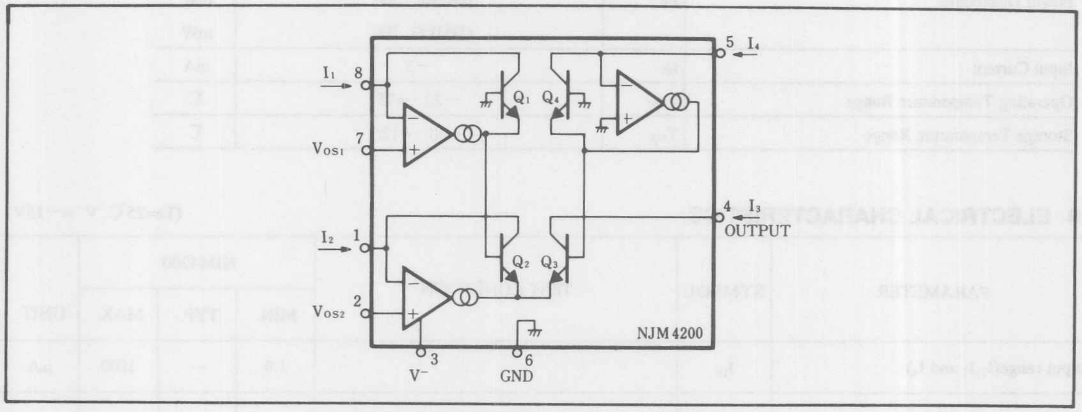


Figure 1. 4200 Multiplier Functional Diagram

$$I_3=\frac{I_1\ I_2}{I_4} \qquad (1)$$

All four currents must be positive and restricted to a range of $1\mu A$ to 1mA. The three input currents go into the multiplier chip at op-amp summing junctions which are nominally at zero volts. Therefore, an input voltage can be easily converted to an input current by a series resistor. Any number of currents may be summed at the inputs. Depending on the application, the output current can be converted to a voltage by an external op-amp or used directly. This capability of combining input currents and voltages in various combinations provides great versatility in application.

Inside the multiplier chip, the three op-amps make the collector currents of transistors Q_1, Q_2, and Q_4 equal to their respective input currents (I_1, I_2, and I_4). These op-amps are designed with current-source outputs and are phase-compensated for optimum frequency response as a multiplier. Power drain of the op-amps was minimized to prevent the introduction of undesired thermal gradients on the chip. The three op-amps operate on a single-supply voltage (nominally −15V) and total quiescent current drain is less than 4mA. These special op-amps provide significantly improved performance in comparison to 741-type op-amps.

The actual multiplication is done within the log-antilog configuration of the Q_1-Q_4 transistor array. These four transistors, with associated proprietary circuitry, were specially designed to precisely implement the relationship.

$$V_{BEN}=\frac{kT}{q}\ 1n\ \frac{I_{CN}}{I_{SN}} \qquad (2)$$

Previous multiplier designs have suffered from an additional undesired linear term in the above quation; the collector current times the emitter resistance. This $I_C r_E$ term can cause significant linearity error. In four-quadrant multiplier circuits, this added $I_C r_E$ term introduces a parabolic nonlinearity even with matched transistors. New JRC has developed a unique and proprietary means of inherently compensating for this undesired $I_C r_E$ term. Furthermore, this New JRC-developed circuit technique compensates linearity error over temperature changes. The nonlinearity-versus-temperature is significantly improved over earlier designs.

From equation (2) and by assuming equal transistor junction temperatures, summing base-to-emitter voltage drops around the transistor array yields:

$$\frac{kT}{q}[1n\frac{I_1}{I_{S1}}+1n\frac{I_2}{I_{S2}}-1n\frac{I_3}{I_{S3}}-1n\frac{I_4}{I_{S4}}]=0 \qquad (3)$$

The equation reduces to: $\frac{I_1\ I_2}{I_3\ I_4}=\frac{I_{S1}\ I_{S2}}{I_{S3}\ I_{S4}}$ (4)

The ratio of reverse saturation currents, $I_{S1}I_{S2}/I_{S3}I_{S4}$ depends on the transistor matching. In a monolithic multiplier this matching is easily achieved and the ratio is very close to unity, typically 1.0±1%. The final result is the desired relationship:

$$I_3=\frac{I_1\ I_2}{I_4} \qquad (5)$$

The inherent linearity and gain stability combined with low cost and versatility makes this new circuit ideal for a wide range of nonlinear functions.

Applications

Four-Quadrant, General-Purpose Multiplier

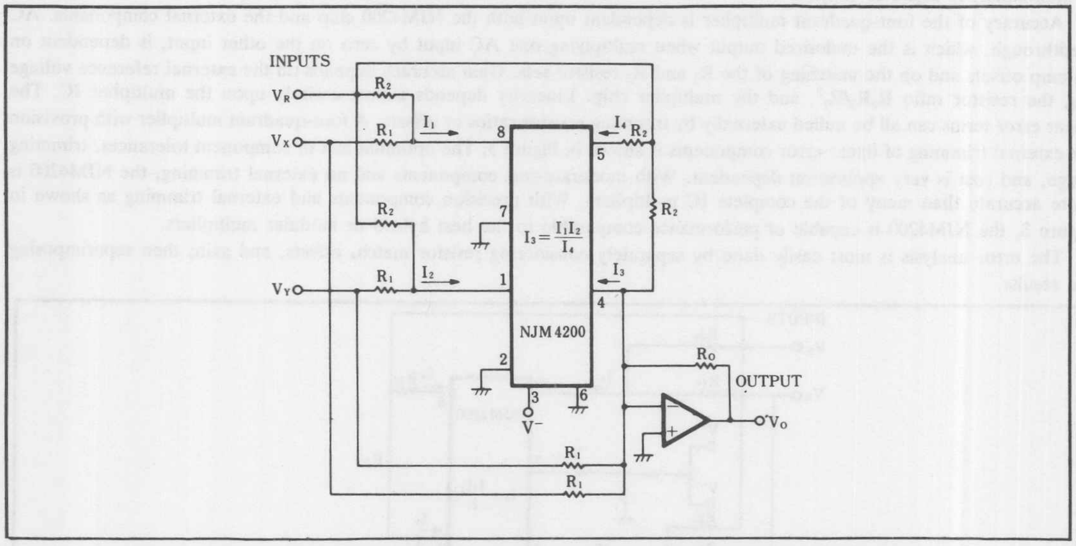


Figure 2. Four-Quadrant General Purpose Multiplier Using the NJM4200

The general schematic for a four-quadrant multiplier using the NJM4200 IC is shown in Figure 2. A positive reference voltage, V_R, is used to offset the multiplier chip. To stay within the most linear operating range, it is necessary that V_R/R_2 plus V_X/R_1 be limited to a range of $50\mu A$ to $250\mu A$. Within the operating range, input and output currents are given by the following equations:

$$I_1=\frac{V_X}{R_1}+\frac{V_R}{R_2} \qquad I_2=\frac{V_Y}{R_1}+\frac{V_R}{R_2} \qquad I_3=\frac{V_X}{R_1}+\frac{V_Y}{R_1}+\frac{V_R}{R_2}+\frac{V_0}{R_0} \qquad I_4=\frac{V_R}{R_2}$$

Combining these relationships through the equation $I_3=I_1I_2/I_4$ yields:

$$V_0=\frac{R_0R_2}{R_1^2}\frac{V_XV_Y}{V_R}$$

The reference voltage V_R must be positive, but V_X and V_Y can be AC voltages. The positive supply voltage can be used as the reference in many applications where a well-regulated +15V is available. Some typical values for a multiplier scaled at $V_XV_Y/10$ are calculated below:

Given: V_X and V_Y have range of −10V to +10V
Desired scaling is $V_0=V_XV_Y/10$
Reference voltage V_R is +15V

Calculation:

(1) Choose $R_1=100k\Omega$

From requirement of $+50\mu A$ minimum

$$\frac{-10V}{100K}+\frac{15V}{R_2}50\mu A$$

Thus, R_2 would also need to be $100k\Omega$

(2) Calculate R_0 from $\frac{R_0R_2}{R_1^2}\frac{1}{V_R}=\frac{1}{10}$

$$R_0=\frac{R_1^2}{R_2^2}\frac{V_R}{10}$$

$$R_0=(100k\Omega)15/10$$

$$R_0=150k\Omega$$

Results:

$$V_0=\frac{V_XV_Y}{10}\text{with } V_R=+15V$$

$R_1, R_2=100k\Omega$

$R_0=150k\Omega$

These values cause a range on I_1 and I_2 of $50\mu A$ to $250\mu A$ to for V_X and V_Y of $-10V$ to $+10V$.

While the choice of values for R_1, R_2 and R_0 are arbitrary, best results are obtained by operating I_1 and I_2 over a range of approximately $50\mu A$ to $250\mu A$.

Accuracy of the four-quadrant multiplier is dependent upon both the NJM4200 chip and the external components. AC feedthrough, which is the undesired output when multiplying one AC input by zero on the other input, is dependent on op amp offsets and on the matching of the R_1 and R_2 resistor sets. Gain accuracy depends on the external reference voltage V_R, the resistor ratio R_0R_2/R_1^2, and the multiplier chip. Linearity depends almost entirely upon the multiplier IC. The linear error terms can all be nulled externally by trimming resistor ratios or offsets. A four-quadrant multiplier with provision for external trimming of linear error components is shown in Figure 3. The optimum mix of component tolerances, trimming range, and cost is very application dependent. With moderate-cost components and no external trimming, the NJM4200 is more accurate than many of the complete IC multipliers. With precision components and external trimming as shown in Figure 3, the NJM4200 is capable of performance comparable to the best hybrid or modular multipliers.

The error analysis is most easily done by separately considering resistor match, offsets, and gain; then superimposing the results.

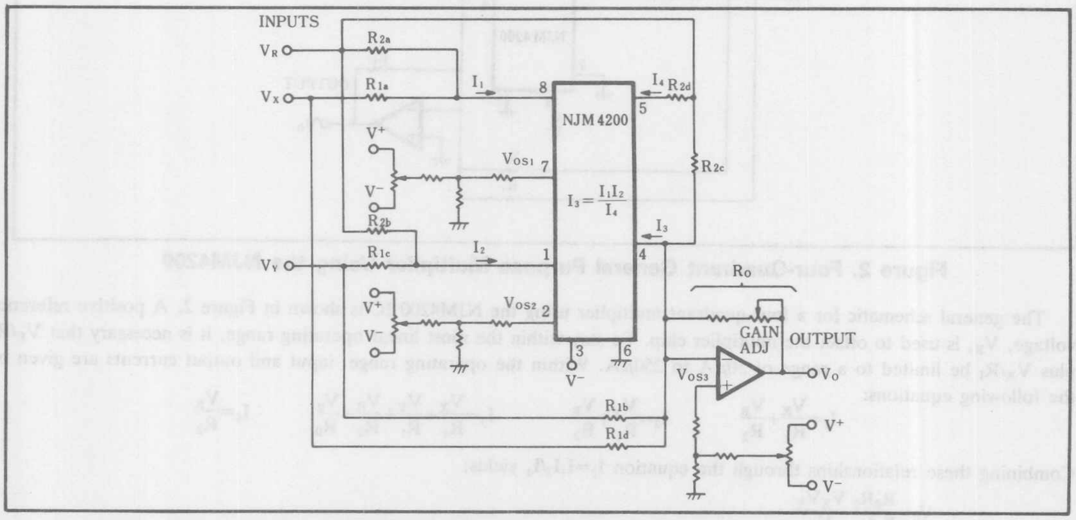


Figure 3. Four-Quadrant, General-Purpose Multiplier with Offset Adjustments

Resistor Matching

Assuming no op amp offsets and no error due to the multiplier chip, then the output would be the sum of the items given below:

$$\text{Desired Output} = \frac{R_0 R_{2d}}{R_{1a}R_{1c}} \frac{V_X V_Y}{V_R} \qquad V_Y \text{ Feedthrough} = \frac{R_0}{R_{1c}}\left(\frac{R_{2d}}{R_{2a}} - \frac{R_{1c}}{R_{1b}}\right)V_Y$$

$$V_X \text{ Feedthrough} = \frac{R_0}{R_{1a}}\left(\frac{R_{2d}}{R_{2b}} - \frac{R_{1a}}{R_{1d}}\right)V_X \qquad \text{Output Offset} = \frac{R_0}{R_{2a}}\left(\frac{R_{2d}}{R_{2b}} - \frac{R_{2a}}{R_{2c}}\right)V_R^2$$

The AC feedthrough is directly proportional to the matching of the R_2 resistor set and the R_1 resistor set. AC feedthrough on the X or Y input is related to resistor tolerance as:

AC Feedthrough$\sim R_0/R_1 \times 2 \times$Res. Tol.$\times V_{IN}$

For example, if R_0/R_1 were 1.5 as in the example given previously and the resistors were matched to within 1%, then the maximum AC feedthrough due to resistor mismatch would be 3% of the V_X or V_Y input voltage. This AC feedthrough can be nulled directly by trimming the resistor sets or indirectly by trimming offsets.

Effect of Op Amp Offsets

In a multiplier, the offsets are cross multiplied and can thus cause AC feedthrough. When one input is zero and the other is a large AC signal, then the output will be the offset of the "zero" input times the AC signal. To quantify this effect, consider the circuit as shown in Figure 3. The offsets of each amplifier are due to both input offset voltage for the op amp and the input offset current times the source resistance.

These offsets can be lumped together into a single V_{OS} term. For this analysis, assume that the external resistors are perfectly matched (R_1's and R_2's all matched). The set of equations below must be combined to see their interaction:

$$I_1=\frac{V_X-V_{OS1}}{R_1}+\frac{V_R-V_{OS1}}{R_2}$$

$$I_2=\frac{V_Y-V_{OS2}}{R_1}+\frac{V_R-V_{OS2}}{R_2}$$

$$I_3=\frac{V_X-V_{OS3}}{R_1}+\frac{V_Y-V_{OS3}}{R_1}+\frac{V_R-V_{OS3}}{R_2}+\frac{V_O-V_{OS3}}{R_0}$$

$$I_4=\frac{V_R-V_{OS4}}{R_2} \qquad I_3=\frac{I_1 I_2}{I_4}$$

$$\text{Desired Output}=\frac{R_0 R_2}{R_1{}^2}\ \frac{V_X V_Y}{V_R}$$

$$V_Y\ \text{Feedthrough}=\frac{R_0}{R_1}\frac{1}{V_R}\left[V_{OS4}-\left(\frac{R_2}{R_1}+1\right)V_{OS1}\right]V_Y$$

$$V_X\ \text{Feedthrough}=\frac{R_0}{R_1}\frac{1}{V_R}\left[V_{OS4}-\left(\frac{R_2}{R_1}+1\right)V_{OS2}\right]V_X$$

$$\text{Output Offset}=\left(\frac{2R_0}{R_1}+\frac{R_0}{R_2}+1\right)V_{OS3}-\left(\frac{R_0}{R_1}+\frac{R_0}{R_2}\right)(V_{OS1}+V_{OS2})$$

For simplicity, $V_{OS}{}^2$ terms and gain-error factors on error terms can be dropped. The output voltage would then be the sum of the terms given above:

To estimate magnitudes, consider the previous example where $R_0=150k\Omega$,R_1 and R_2 were $100k\Omega$, and $V_R=15V$. Then,

V_Y Feedthrough$=1/10(V_{OS4}-2V_{OS1})V_Y$

V_X Feedthrough $=1/10(V_{OS4}-2V_{OS2})V_X$

Output Offset$=5.5V_{OS3}-3(V_{OS1}+V_{OS2})$

To carry this example further, let each V_{OS} term have a maximum value of $\pm10mV$. The worst-case combination would then be a feedthrough of $0.003V_Y$ and $0.003V_X$. Output offset could be as high as 115mV, but would generally be less.

The trimming procedure is straight-forward when done in the following recommended sequence.

1. Apply a full-scale AC voltage To V_Y and make V_X zero. Trim V_{OS1} for output null ($V_O=0$).
2. Apply the same full scale AC voltage to V_X and V_Y zero. Trim V_{OS2} for output null ($V_O=0$).
3. Apply zero to both inputs($V_X=0$ and $V_Y=0$). Trim V_{OS3} for output null ($V_O=0$).
4. Adjust scale factor with R_0. Always adjust the input offsets before setting the scale factor.

In most application, the offset adjustments are used to compensate for the R_1 and R_2 resistor network mismatch as well as the op amp offsets. Thus, the range of offset adjustment is usually chosen to encompass both error terms. For example, the V_Y feedthrough is:

$$\left\{\frac{R_0}{R_1}\left(\frac{R_{2a}}{R_{2b}}-\frac{R_{1a}}{R_{1b}}\right)+\frac{R_0}{R_1}\frac{1}{V_R}\left[V_{OS4}-\left(\frac{R_2}{R_1}+1\right)V_{OS1}\right]\right\}V_Y$$

Varying V_{OS1} over sufficient range can compensate for both offset and resistor mismatch.

One Quadrant Divider

Division is very easily implemented with the NJM4200 multiplier when the inputs are all positive. The circuit for one-quant division is shown in Figure 4. The inputs V_X, V_Z, and V_R must be positive and the input currents I_1, I_2 and I_4 must be restricted in range. Within the rated range, I_1 I_2 will equal I_3 I_4 and therefore:

$$\left(\frac{V_X}{R_1}\right)\times\left(\frac{V_R}{R_2}\right)=\left(\frac{V_0}{R_0}\right)\times\left(\frac{V_Z}{R_4}\right)$$

$$V_0=\frac{R_0 R_4}{R_1 R_2}V_R\frac{V_X}{V_Z}$$

The reference input V_R is generally fixed and the ratio of R_0R_4/R_1R_2 is usually chosen to make $V_O=10V$ at the maximum value of V_X/V_Z. For example, if $V_R=6.2V$ and V_X/V_Z maximum is one, then choose R_0R_4/R_1R_2 of 10/6.2 which is 1.613. The output would then be:

$$V_0=10\frac{V_X}{V_Z},\quad \text{where}\ \frac{V_X}{V_Z}\leqq 1$$

As with the four-quadrant multiplier circuit, op amp offsets cross-multiply with the inputs.

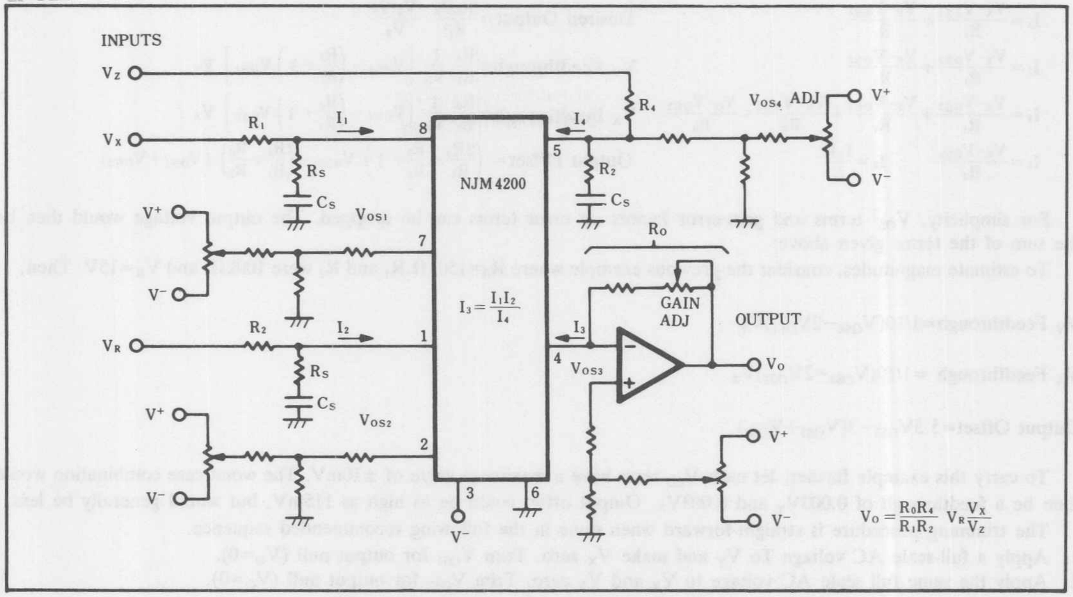


Figure 4. One-Quadrant Divider

These offsets should be nulled to obtain best accuracy. The output voltage with offsets considered, but neglecting V_{OS}^2 terms, is given by:

$$V_0 = \overbrace{\frac{R_4 R_0}{R_1 R_2} V_R \frac{V_X}{V_Z}}^{\text{Ideal}} + \overbrace{\frac{R_4 R_0}{R_1 R_2}\left[\frac{V_R V_X}{V_Z^2}V_{OS4} - \frac{V_X}{V_Z}V_{OS2} - \frac{V_R}{V_Z}V_{OS1}\right]}^{\text{Error Terms}} + V_{OS3}$$

Because the offsets and signals are interactive, the recommended procedure for adjustment is the following:

1. Monitor the offsets at pins (8) and (1) directly and adjust V_{OS1}, V_{OS2} to null them. This removes the V_{OS1} and V_{OS2} error terms.
2. Make $V_X = V_Z$ and sweep over their full dynamic range. The output should be constant; vary the V_{OS4} ADJ pot for a constant output of $R_4 R_0 V_R / R_1 R_2$ plus V_{OS3}.
3. Apply the minimum value of V_X/V_Z and adjust V_{OS3} to obtain the proper V_0.
4. Apply the maximum value of V_X/V_Z and adjust R_0 for proper V_0.

The accuracy will be limited only by the nonlinearity, which for the NJM4200 is very small.

Square-Rooting

The circuit for implementing the square-rooting function is shown in Figure 5. An input voltage V_X multiplied by a reference voltage V_R is made equal to the square of the output voltage. The relationship $I_1 I_2 = I_3 I_4$ becomes:

$$\frac{V_X V_R}{R_1 R_2} = \frac{V_0^2}{R_0 R_4}$$

The input voltage must be positive. Scaling is determined by the external resistor network and reference voltage V_R. The output voltage is given by:

$$V_0 = \sqrt{\frac{R_0 R_4}{R_1 R_2} V_R V_X}$$

In most applications, the resistors should be comparable in value and V_R should be in the range of 5V to 15V. A scale factor of 10 is very convenient and provides an output range of 0.3V to 10V for an input range of 10mV to 10V. In equation form:

$$V_0 = \sqrt{10 V_X}, \quad 10\text{mV} < V_X < 10\text{V}$$

The offsets can be externally trimmed as needed. The nonlinear nature of the square-rooting function makes the error due to offsets very small for large inputs and very large at low input levels. With offsets included, the output voltage is:

$$V_0 = \left[\frac{R_0 R_4}{R_1 R_2} V_R \left(1 - \frac{V_{OS2}}{V_R}\right) V_X - \frac{R_0 R_4}{R_1 R_2} V_R V_{OS1} + V_0 (V_{OS3} + V_{OS4})\right]^{1/2}$$

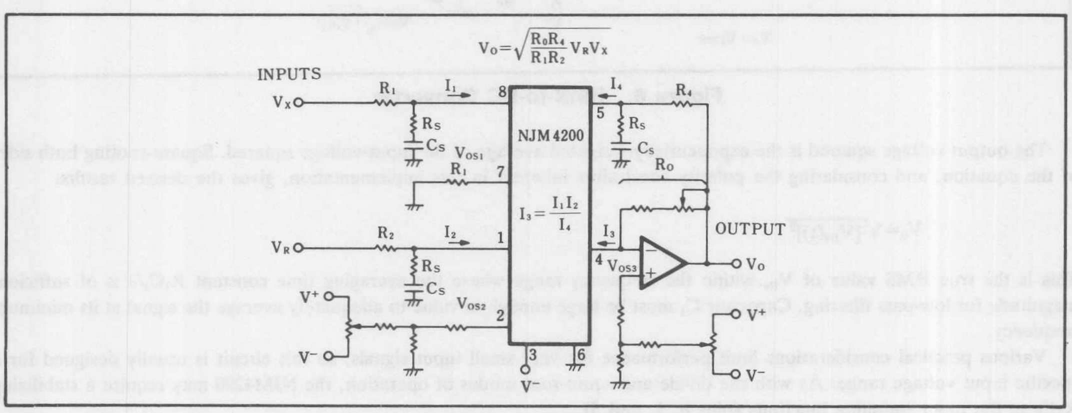


Figure 5. Square-Rooting Circuit

The term V_{OS2}/V_R affects gain only and is constant, therefore varying R_O can compensate for the V_{OS2} error term. The effect of V_{OS3} and V_{OS4} is additive and only one of these offsets are advisable to be adjusted. The V_{OS1} term should be trimmed to zero. The recommended trimming sequence is as follows:

1. Adjust V_{OS3} to zero directly by monitoring pin(4).
2. Apply minimum value of V_X and adjust V_{OS1} for correct V_0.
3. Apply maximum value of V_X and adjust R_0 for correct V_0.

The square-rooting circuit can easily be designed for overall accuracy of ±0.2% when using the NJM4200 IC multiplier.

RMS-to-DC Converter

The root-mean-square value of a complex waveform can be computed directly by squaring, integrating, and then square rooting. The NJM4200 is idealy suited to this computation and the entire RMS-to-DC conversion can be implemented with a single device.

A functional diagram is shown in Figure 6. An absolute-value circuit, or precision rectifier, first converts the AC input into a rectified positive voltage. Input currents I_1 and I_2 are made equal and will be $|V_{IN}|/R_1$. The remaining input current, I_4, is made equal to V_0/R_0 plus a derivative term, $C_0 dV_0/dt$. Combining these relationships according to $I_1 I_2 = I_3 I_4$,

$$\frac{V_{IN}^2}{R_1^2} = \frac{V_0^2}{R_1^2} + C_1 \frac{dV_0}{dt}\frac{V_0}{R_1}$$

This equation is equivalent to

$$V_0^2 + \frac{R_1 C_1}{2}\frac{d}{dt}\left(V_0^2\right) = V_{IN}^2$$

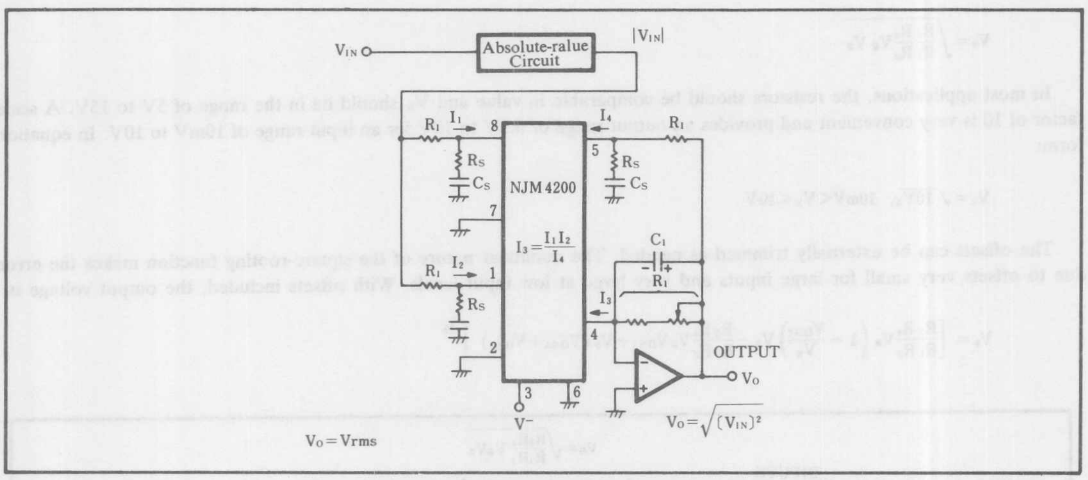


Figure 6. RMS-to-DC Converter

The output voltage squared is the exponentially-weighted average of the input-voltage squared. Square-rooting both sides of the equation, and considering the polarity constraints inherent in this implementation, gives the desired results:

$$V_0 = \sqrt{\overline{[V_{IN}(t)]^2}}$$

This is the true RMS value of V_{IN} within the frequency range where the averaging time constant $R_1C_1/2$ is of sufficient magnitude for low-pass filtering. Capacitor C_1 must be large enough in value to adequately average the signal at its minimum frequency.

Various practical considerations limit performance for very small input signals, so this circuit is usually designed for a specific input voltage range. As with the divide and squre-root modes of operation, the NJM4200 may require a stabilizing $R_S C_S$ at the input summing junctions (pins 8, 1, and 5).

The specific component values and external adjustments needed depends on the particular application.

Design Considerations

Frequency Response and Stability

The op amps within the NJM4200 multiplier are stabilized for optimum performance in the four-quadrant multiplier configuration. At extremes of input current, the stability becomes marginal and external phase compensation may be required. The possibility of undesired oscillations should be considered for input currents of less than 50μA or greater than 500μA. Dividing and square-rooting operations often require a wide dynamic range on the input currents.

Two techniques are very helpful for assuring frequency stability and minimizing noise under a wide range of conditions:

1. Connect a series R_SC_S from input summing junction to ground as shown in Figure 7. This network has the effect of attenuating the feedback at high frequencies and thereby stabilizing the op amp. Loop gain at high frequencies is sacrificed, but this is seldom of concern in dividing or square-rooting applications. Recommended values are 10kΩ for R_S and 0.005μF for C_S
2. The resistor on the noninverting input can be bypassed as shown in Figure 7. This helps to reduce noise.

The need for these frequency compensating techniques will depend on the application, particularly the input current range and input signal characteristics.

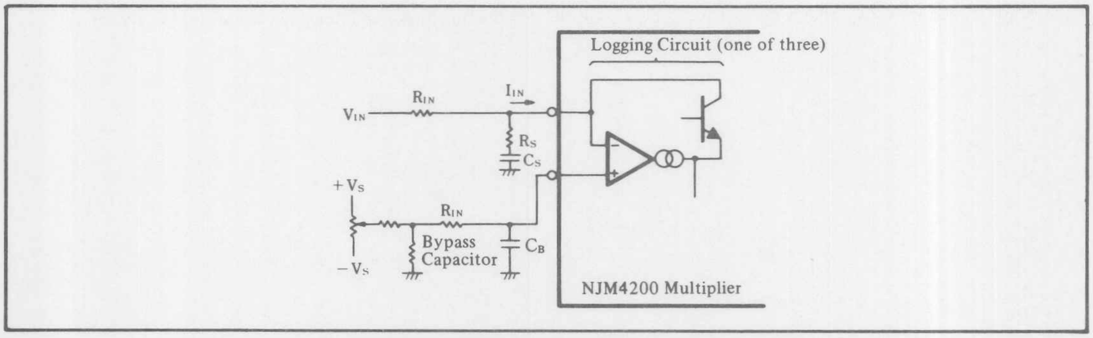


Figure 7. Optional Frequency Stability Components R_S,C_S and C_B

Gain Stability

This type of multiplier is very sensitive to temperature gradients across the transistor quad (Q_1 to Q_4 and Q_2 to Q_3). The ambient temperature tends to affect offsets, but temperature gradients will cause a gain error. Several steps can be taken to minimize this effect:

1. Keep the multiplier physically remote from power dissipating components.
2. When using printed-circuit boards, make pad sizes and layout pattern as symmetrical as possible.
3. Head sinking or epoxy potting can be used if necessary. This will tend to prevent rapid changes in temperature gradient.

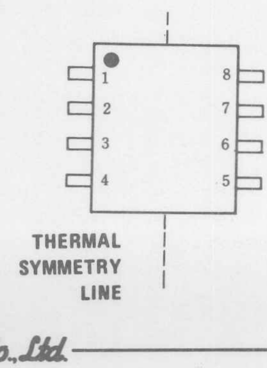
Power drain within the multiplier chip itself is relatively low, therefore the gain stability can be very good if the IC is not exposed to temperature gradients.

Offset Stability

Input offset voltage of the op amps can be easily trimmed if desired. The effects of input bias current drift can be minimized by making the impedance approximately equal on the inverting and noninverting inputs. The equivalent input offset will then depend only on the difference in bias currents rather than the absolute values.

■ THERMAL SYMMETRY

The scale factor is sensitive to temperature gradients across the chip in the lateral direction. Where possible, the package should be oriented such that sources generating temperature gradients are located physically on the line of thermal symmetry. This will minimize scale-factor error due to thermal gradients.



INDEX

INDEX

DISCONTINUED PRODUCTS

■ DISCONTINUED PRODUCTS TABLE

Type No.	FUNCTION
NJM387	Dual Low Noise OP-Amp
NJM2404E	3/4 Wired Remote Controller
NJM2610	Bi-Directional Motor Driver
NJM2066	Dual Head Phone Driver Amplifier
NJM2204B	Log Amplifier
NJM2075A	Dolby B/C Type NR Processor
NJM2175	Dolby Prologic Surround Decoder
NJM2219	RF Modulator
NJM2225A	Video Camera Auto-Iris Function
NJM2259	UHF Band RF Modulator
NJM2270	RF Amplifier
NJM3201	FDD Read/Write Amplifier
NJM2104F	System Reset IC
NJM2620	Motor Driver for VCR
NJM2250	EVF Driver IC
NJM2260	RF Amplifier IC
NJD6505/06	NPN Transistor Array
NJD6511/12/13/14	Ttansistor Array

New Japan Radio Co., Ltd.

HEAD OFFICE

3-10 Yokohama-cho, Nihonbashi, Chuo-ku, Tokyo 103, Japan

Phone: 81-3-5642-8288 FAX: 81-3-5642-8229

U.S. SUBSIDIARY

NJR Corporation 440 East Middlefield Rd., Mountain View, CA 94043, U.S.A.

Phone: 415-961-3901 FAX: 415-969-1409

B497